Phase 1: Datapath components

Registers
Registers must be 32-bits wide with a synchronous load enable signal and a asynchronous clear signal.

Multiplexers
2:1 and 4:1 multiplexers for a 32-bit bus.

Arithmetic Logic Unit (ALU)
This unit takes two 32-bit numbers and a carry bit as its inputs and implements the necessary operations to perform all basic arithmetic and logic instructions. Its outputs are a 32-bit number representing the result of the executed operation and 4 bits representing the condition codes for the operation (N, Z, C, V). The tester module must show correct operation for all basic arithmetic and logic instructions as well those that alter the condition codes.

Register Windows Mechanism
This unit must implement at least four register windows, including the necessary glue logic to allow for overlapping windows. It must have one 32-bit input port that allows writing to a visible register and two 32-bit output ports that allows one visible register to be read. One constraint is that this module cannot be designed as a behavioral model. The tester module must show R/W capabilities for registers on every window. Overlapping registers must preserve their values during a window switch and Round Robin functionality must be present as well. Include a Block Diagram of the design.

Random Access Memory
The memory unit must be at least 512 bytes in size and must be capable of handling bytes (8-bits), halfwords (16-bits), words (32-bits) and double words (64-bits). All necessary handshaking signals must be present including any necessary bus lines. Independent buses for R/W operation may be used. The unit must be preloaded with a textfile containing a test program. This file consists of a series of bytes separated by spaces or new lines. Each group of four bytes correspond to one instruction. The first byte read is the MSB while the fourth byte is the LSB (Big Endian). The tester module must show the unit is capable of performing R/W operations on bytes (8-bits), halfwords (16-bits), words (32-bits) and double words (64-bits), while correctly managing both data and address bus lines.