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Electronics Mini Lab Report Cover Page

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Department: Electrical and Electronic Engineering	**Module Name:** Practical Engineering Design Solutions and Project Development
Module Code: EEEE2046	**Module Convenors:** Dr. Ricardo Correia
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Design calculation

Filter calculation: Speed detection range for the radar was chosen to be from 15 mph to 50 mph (6.7056 m/s to 22.352 m/s), the range of normal vehicle speed on roads.

Filter calculation: Vehicle speed v and Doppler frequency f_D can be linked by equation 1:

$$v = \frac{c \times f_D}{2 \times f_{tx}} \quad (1)$$

Where f_{tx} is the transmitter frequency; The low cut-off and high cut-off frequency (f_{cl} and f_{ch}) can be calculated by equation 2 and 3 respectively:

$$f_{cl} = \frac{2 \cdot V_{min} \cdot f_{tx}}{c} = \frac{2 \cdot 6.7056 \cdot 10.587 \times 10^9}{3 \times 10^8} Hz = 473.3\ Hz \quad (2)$$

$$f_{ch} = \frac{2 \cdot V_{max} \cdot f_{tx}}{c} = \frac{2 \cdot 22.352 \cdot 10.587 \times 10^9}{3 \times 10^8} Hz = 1577.6\ Hz \quad (3)$$

The resistors' value R_1 and R_2 for the filter was set to be 10 $K\Omega$. Based on high cut-off frequency and low cut-off frequency, capacitor value C_1 and C_2 can be calculated by equation 5 and 7:

$$f_{cl} = \frac{1}{2\pi R_1 C_1} \quad (4) \qquad f_{ch} = \frac{1}{2\pi R_2 C_2} \quad (6)$$

$$C_1 = \frac{1}{2\pi R_1 f_{cl}} = \frac{1}{2\pi \times 10K\Omega \times 473.3\ Hz} = 20.17\ nF \approx 22\ nF \quad (5)$$

$$C_2 = \frac{1}{2\pi R_2 f_{ch}} = \frac{1}{2\pi \times 10K\Omega \times 1577.6\ Hz} = 10.08\ nF \approx 10\ nF \quad (7)$$

Amplifier calculation: Based on filter simulation output, input for the amplifier is expected to be in range from 1.62 V to 1.67 V and based on ADC and comparator input range for STM32, the output of amplifier is set to be 0 V to 3.3 V. Calculations for ADC and comparator amplifier are shown below:

ADC Amplifier:

Set $V_{out} = mV_{in} + b$, Substitute V_{out} and V_{in} with their respective maximum and minimum values:

$$\begin{cases} 3.3 = 1.67m + b \\ 0 = 1.62m + b \end{cases}, \begin{cases} m = 66 \\ b = -106.92 \end{cases}$$

$$m = \frac{R_F + R_G + R_1||R_2}{R_G + R_1||R_2}, |b| = V_{ref} \cdot \left(\frac{R_2}{R_1 + R_2}\right) \cdot \left(\frac{R_F}{R_G + R_1||R_2}\right)$$

set R_G = 6.8 KΩ, $V_{ref} = 3.3\ V$:

R_1 was calculated to be 2.2 KΩ and R_2 to be 2.2 KΩ, R_F = 470 KΩ.

Comparator Amplifier:

To obtain square wave, V_{out} needs to have large swing. Any value greater than 3.3 V and below 0 V will be cut off by the op-amp to obtain square wave.

$$\begin{cases} 30 = 1.67m + b \\ -30 = 1.62m + b' \end{cases}, \begin{cases} m = 1200 \\ b = -1974 \end{cases}$$

$$m = \frac{R_F + R_G + R_1||R_2}{R_G + R_1||R_2}, |b| = V_{ref} \cdot \left(\frac{R_2}{R_1 + R_2}\right) \cdot \left(\frac{R_F}{R_G + R_1||R_2}\right)$$

set R_G = 6.8 KΩ, $V_{ref} = 3.3\ V$:

R_1 was calculated to be 2.2 KΩ and R_2 to be 2.2 KΩ, R_F to be 2.2 MΩ.

*Because $R_G >> R_1||R_2$, $R_1||R_2$ was neglected during the calculation.

*Because $m > 0, b < 0$ for both ADC and comparator amplifier, their circuit configuration was chosen to be case 3 according to the handout.

Design and simulation model

LTspice models for both ADC and comparator input are shown in figure 1 and 2 respectively. Since the selected speed range for both inputs are the same, the filter for both will be of same specification. The input for the filter is set to be a sine wave with frequency of 470 Hz and amplitude of 50 mV to simulate the waveform from Doppler radar near a tuning fork. The amplifier for ADC and comparator is different due to

different gain requirement. As discussed in amplifier calculation section, the output of ADC amplifier needs to span ideally from 0 V to 3.3 V, while the gain for comparator needs to be large to produce square wave. Therefore R_F for comparator input circuit is significantly larger.

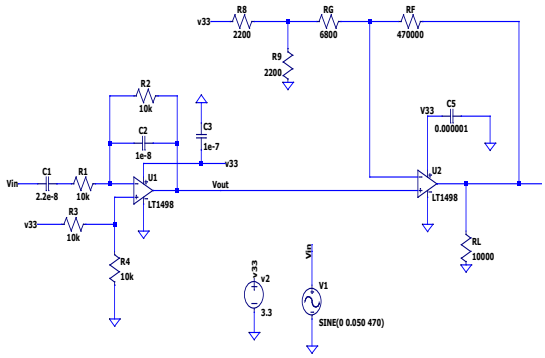

Fig1. Filter and amplifier circuit for ADC input.

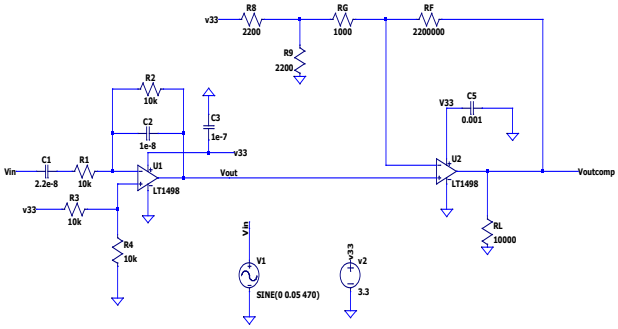

Fig2. Filter and amplifier circuit for Comparator input.

The simulation results for filter circuit input and output waveform and AC analysis are shown in figure 3 and 4 below respectively:

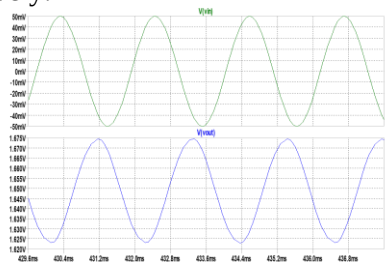

Fig 3: Filter input and output for both ADC and Comparator Circuit

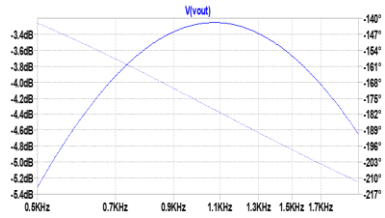

Fig 4: Filter circuit AC analysis output

The input and output waveform for ADC and comparator amplifier are shown in figure 5 and figure 6 respectively.

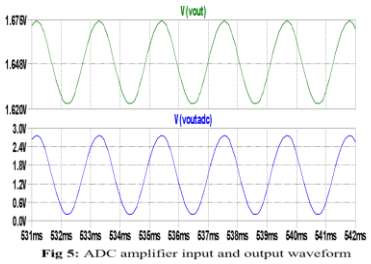

Fig 5: ADC amplifier input and output waveform

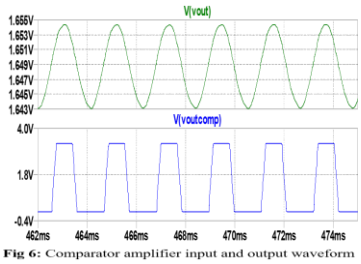

Fig 6: Comparator amplifier input and output waveform

Physical Construction

Physical construction was taken place by submitting schematics and remotely soldered by technicians. The schematics can be referred to the appendix.

Explanation of testing process

Sine waves of different frequency and amplitude were generated by the function generator and applied to the ADC and comparator circuit. Outputs from ADC and comparator circuits were collected from the oscilloscope and plotted on excel graphs.

Test result

Sampled waveform data for both input and output signal for ADC filter and amplifier circuit:

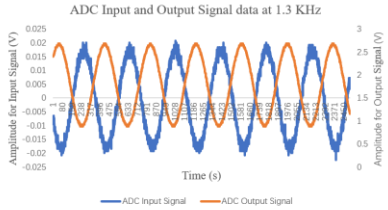

Fig 7: ADC input and output data at 1.3 KHz

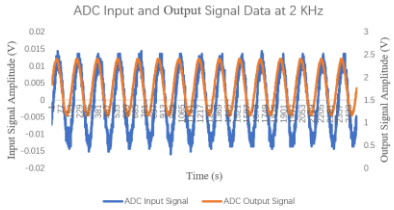

Fig 8: ADC input and output data at 2 KHz

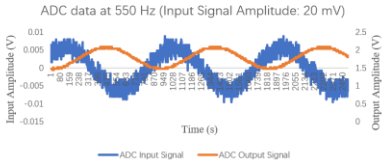

Fig 9: ADC waveforms at 2 KHz with input amplitude 20 mV

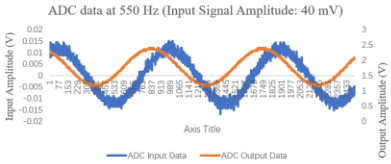

Fig 10: ADC waveforms at 2 KHz with input amplitude 40 mV

Sampled waveform data for both input and output signal for comparator filter and amplifier circuit:

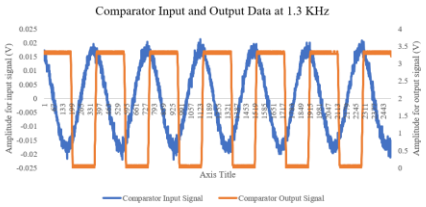

Fig 11: Comparator input and output data at 1.3 KHz

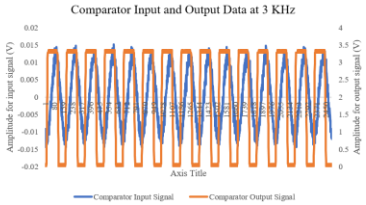

Fig 12: Comparator input and output data at 3 KHz

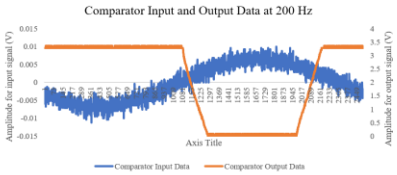

Fig 13: Comparator input and output data at 200 Hz

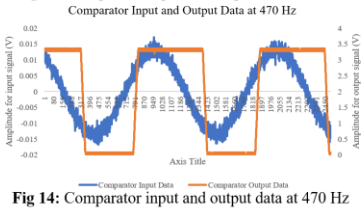

Fig 14: Comparator input and output data at 470 Hz

Discuss of the result:

Simulation results are shown in design and simulation model section. AC analysis for filter shows slow frequency roll-off. The wanted frequency range is from 473.3 Hz to 1577.6 Hz. However, from figure 4, the -3 dB cut-off range is greater than expected which will cause unwanted signal to be selected. This might be due to the characteristics of the filter circuit configuration. Butterworth or Chebyshev filter circuit configuration has fast roll-off and might improve circuit performance. The amplifier simulation for ADC circuit has span from around 0.3 V to 2.7 V, when input from Doppler radar module is expected to have amplitude of around 40 mV. In reality, radar signal might be smaller and ADC circuit output might have smaller span than this, but it is good enough for STM32 algorithms to process. Real circuit test results are shown in figure 11 to 14 in test result section. For both ADC and comparator circuit, filter shows poor frequency selectivity. Input signals at 200 Hz or 3 KHz, which is outside the wanted frequency range, still produce measurable outputs. The attenuation on unwanted frequency range is not obvious for the filter. Amplifier could work as expected for both circuits. Improvements could be done such as changing filter to Chebyshev to increase circuit selectivity and improve overall performance.

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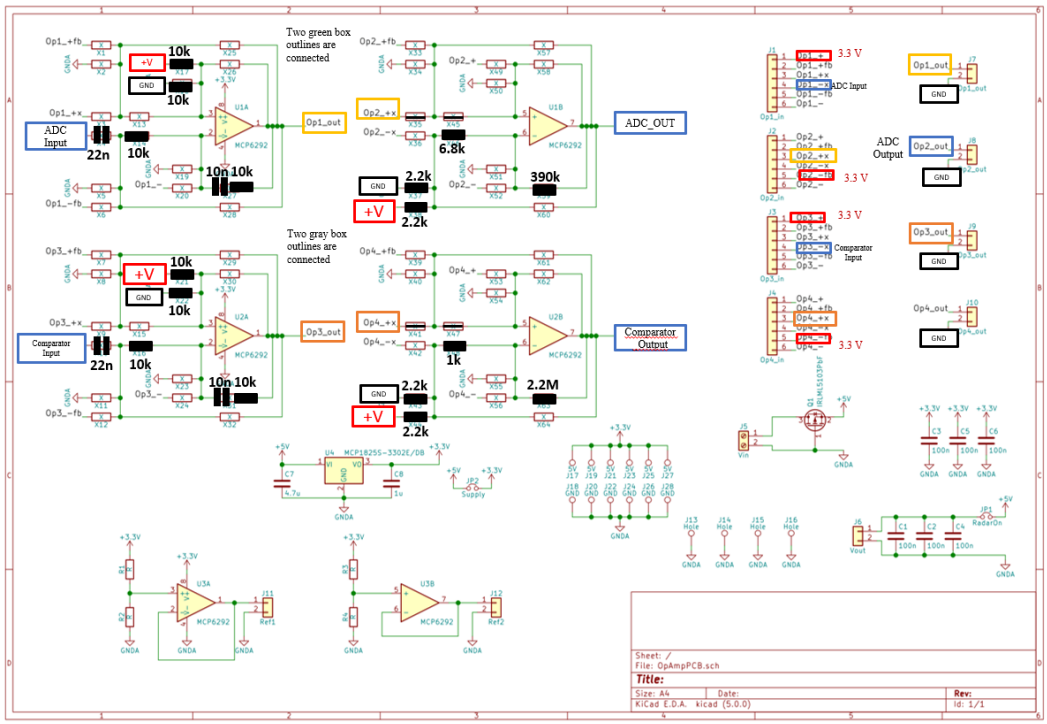
Appendix:

Submitted Circuit Construction Schematics:



Voltage Setting:

3.3V

How to use:

- Modify the voltage text box to select either 5V or 3.3V
- Copy and paste the component markers on to the schematic
- Don't forget to include labels with the values
- Use the box outlines to indicate wire/external connections
- Example on next slide