Analysis of Classic Transimpedance Amplifiers and Design Considerations for Low Shunt Resistance Photodiodes

John Petrilli

Introduction

An abundance of information and resources on transimpedance amplifiers (TIAs) are widely available in books, articles, and application notes. There are three aspects of this app note which provide value beyond what is already available: analysis and equation derivation at every step of the design, design considerations for source inputs with low shunt resistance, and a TIA calculator to quickly visualize the impacts of design choices.

TIA Basic Concept

A transimpedance amplifier converts current at the input to voltage at the output. TIAs are commonly used with photodiodes, however they are effective with most current sources.

The typical design goal is to be shot noise limited[1] with a wide bandwidth. These two parameters will be a trade-off in a classic TIA design, although keep in mind that a custom frontend can help achieve both.

Figure 1 displays the basic design idea behind the TIA.

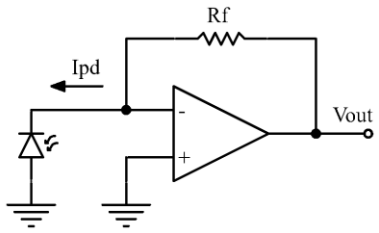

Figure 1. Basic Transimpedance Amplifier Design Concept

It is universally known that an ideal voltage feedback op-amp draws zero current at the inputs. Therefore, all the photodiode current I_P, travels through the feedback resistor R_F resulting in equation (1).

$$\frac{V_{OUT} - V_{IN-}}{R_F} - I_{PD} = 0 \quad (1)$$

$$V_{IN-} = V_{IN+} = 0 \quad (2)$$

Substituting (2) into (1) we get:

$$V_{OUT} = R_F I_{PD} \quad (3)$$

Photodiodes

Photodiodes are PIN or P-N junction semi-conductor devices which convert photons into electrical current through the photoelectric effect. These devices are the most common input source to a transimpedance amplifier.

Equivalent Electrical Model

A photodiode's equivalent circuit ends up being a current source in parallel with a diode, capacitor, and resistor along with a series resistance as seen in figure 2.

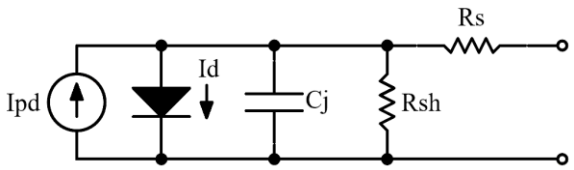

Figure 2. Photodiode Equivalent Electrical Model

I_D is the dark current and it is a noise contributor, however it can be minimized or completely avoided if the photodiode is configured in photovoltaic mode. C_J is the junction capacitance, R_{SH} is the shunt resistance, and R_S is the series resistance. R_S is small and typically ignored in the TIA analysis. Adding R_S into the circuit analysis gives diminishing returns when comparing analysis complexity and useful results.

Frequency Response Considerations

The frequency response and stability of the TIA ends up being dependent on the junction capacitance, C_J. To reduce C_J one can either reverse bias the photodiode, pick a photodiode

[1] Shot noise limited is defined as the noise from the input current source being the dominant contributor among all noise components.

with a smaller active area, or use bootstrapping techniques reduce the effective C_J.

Responsivity
Responsivity of a photodiode is the amount of photocurrent per incident light, given in A/W. Photodiode datasheets will supply a graph of responsivity vs. wavelength similar to figure 3.

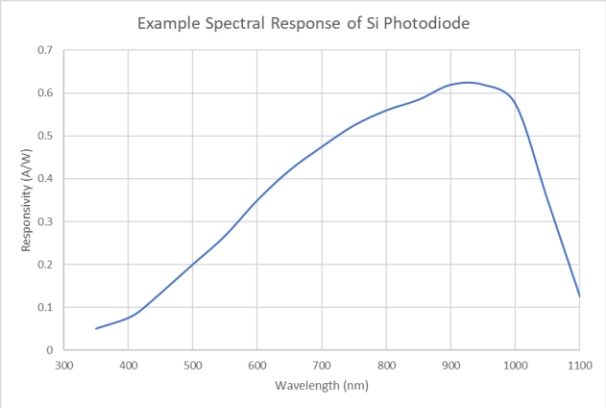

Figure 3. Example Spectral Response of Si Photodiode

As the responsivity increases the required transimpedance gain of the circuit decreases resulting in better noise performance. If possible, it is advantageous to optimize the wavelength of incident light vs. the photodiode's responsivity.

Photodiode Configurations
Photovoltaic mode is the unbiased configuration of the photodiode. This configuration is suggested for low bandwidth (less than a few hundred kHz) and low light applications. An example of photovoltaic mode is shown in figure 4.

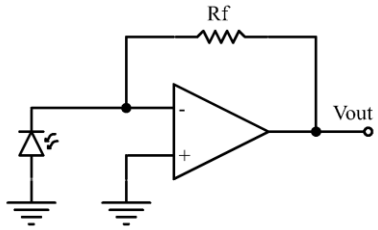

Figure 4. Transimpedance Amplifier with Photovoltaic Configuration

Photoconductive mode is the configuration where the photodiode is subjected to a reverse bias voltage. An example is shown in figure 5.

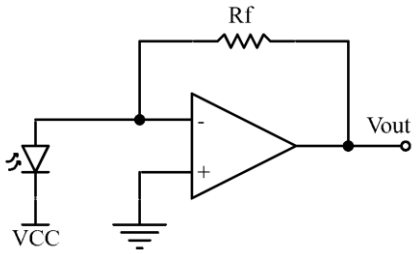

Figure 5. Transimpedance Amplifier with Photoconductive Configuration

This configuration reduces the junction capacitance and in turn will increase the frequency response of the circuit. The drawback here is an increase in dark current which will increase the detectors shot noise.

$$I_{SN} = \sqrt{2 * q * (I_P + I_D)\Delta f} \qquad (4)$$

Equation 4 shows the contribution dark current has on the shot noise. In applications where the photocurrent is an order of magnitude above the dark current, the noise contribution from the dark current will go unnoticed.

Quick Op-Amp Review

Equations for an op-amps open loop response, closed loop response, and feedback factor are used throughout this application, so here is a quick review which will be referenced later.

Open Loop Block Diagram
An operational amplifier operating in open loop can be described by the following block diagram:

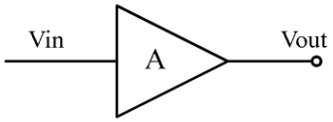

Figure 6. Block Diagram of Open Loop Op-Amp

The open loop equation can be described by equation (5) below. The negative gain is due to the inverting nature of the TIA.

$$V_{OUT} = -AV_{IN} \qquad (5)$$

Closed Loop Block Diagram
Gain of an operational amplifier operating in closed loop can be described by the following block diagram:

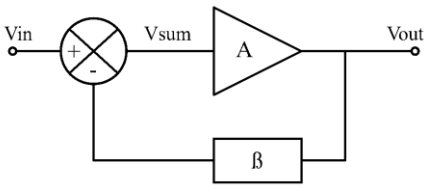

Figure 7. Block Diagram of Closed Loop Op-Amp

Derivation of the amplifiers gain equation:

$$V_{OUT} = AV_{SUM} \tag{6}$$

$$V_{SUM} = V_{IN} - \beta V_{OUT} \tag{7}$$

$$V_{OUT} = A(V_{IN} - \beta V_{OUT}) \tag{8}$$

$$\frac{V_{OUT}}{V_{IN}} = A_{CL} = \frac{A}{1 + A\beta} \tag{9}$$

When the open loop gain A, becomes sufficiently large compared to β, the total gain can be reasonably estimated by the closed loop gain as shown in equation (10).

$$\frac{V_{OUT}}{V_{IN}} = A_{CL} = \frac{1}{\beta}, when\ A \gg\ \beta \tag{10}$$

Note the following:

- Feedback factor = 1/β
- Voltage noise gain is the closed loop gain described by equation (9)

TIA DC Analysis

Input Impedances

TIAs have the best performance when the input current sources are as close to ideal as possible. There are two main reasons for this: First, ideal current sources allow all the current to transfer to the load, second it reduces the noise gain which improves the noise performance.

Ideally, the op-amps equivalent input impedance as seen by the current source will be very low, and the current sources shunt resistance will be very high resulting in all of the input current to travel through the feedback resistor.

Ideal Current Source

An ideal current source as shown in figure 8 is defined as a current source in parallel with infinite resistance. This makes the current source impervious to the load.

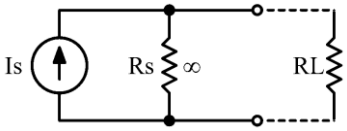

Figure 8. Ideal Current Source

$$I_{RL} = I_S \frac{R_S}{R_S + R_L} \tag{11}$$

From equation (11) we can see that an ideal current source wastes no current through the parallel resistance R_S. As R_S decreases into the realm of practical values, proportionally less current is transferred to the load.

Op-Amp Equivalent Input Impedance

Figure 9 shows the equivalent input impedance of the op-amp as seen by the input current source.

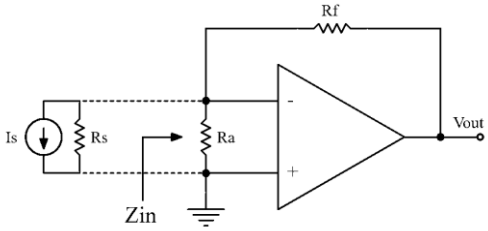

Figure 9. Model for Derivation of Op-Amps Equivalent Input Impedance as seen by the Input Source

Modifying the KCL from equation (1) by adding the op-amps input resistance R_A, we get the following:

$$\frac{V_{IN-}}{R_A} + \frac{V_{OUT} - V_{IN-}}{R_F} - I_{PD} = 0 \tag{12}$$

From equation (5) we know that V_{OUT} can be substituted with $-AV_{IN}$.

$$V_{IN-}\left(\frac{1}{R_A} + \frac{1 + A}{R_F}\right) = I_{PD} \tag{13}$$

$$Z_{IN} = \frac{V_{IN-}}{I_S} = \frac{1}{\left(\frac{1}{R_A} + \frac{1 + A}{R_F}\right)} \tag{14}$$

Plugging in typical values such as R_A=100GΩ, R_F=1MΩ, A=100dB we can see that the input impedance is quite small which is desirable.

$$Z_{IN} = \frac{1}{\left(\frac{1}{100e9} + \frac{1 + 1e5}{1e6}\right)} = 10\Omega \tag{15}$$

Shunt Resistance Effect on TIA Current
The efficiency of current transferred to the feedback resistor is plotted in figure 10 by using the current divider in figure 8. The source resistance is varied while the load impedance Z_{IN} stays static.

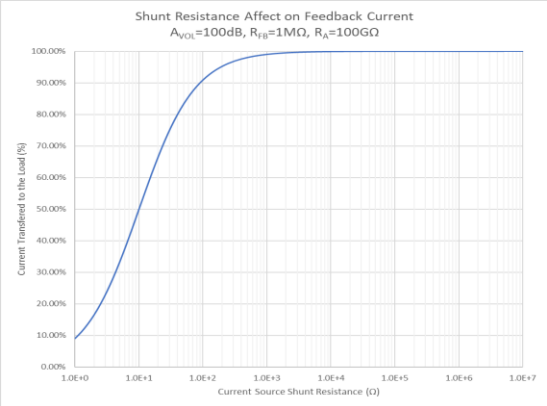

Figure 10. Amount of Photocurrent Transferred to the Feedback Network, Expressed as a Percent.

It can be inferred from figure 10 that current sources with a low shunt resistance will experience non-linear transimpedance gain with the gain being lower than the value of the feedback resistor. The TIA gain will also be slightly unpredictable and vary on a unit-to-unit basis due to manufacturability variations on the amplifiers GBP and open loop gain.

Feedback Factor
In a TIA the feedback factor represents the required closed loop voltage gain to keep the two op-amp inputs at differential zero. This is what makes equation (3) true.

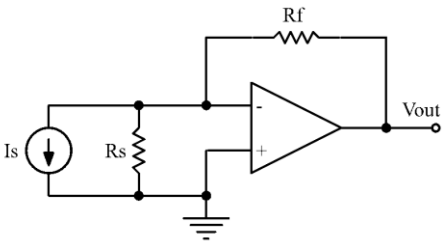

Figure 11. Transimpedance Amplifier with Ideal Input

Ignoring the current I_S, let's see what voltage gain is required of the op-amp by performing a KCL around the inverting input of figure 11.

$$\frac{V_{IN-}}{R_S} + \frac{V_{IN-} - V_{OUT}}{R_F} = 0 \qquad (16)$$

Solving for the transfer function of the circuit we get the following:

$$\frac{V_{OUT}}{V_{IN-}} = \frac{1}{\beta} = \frac{R_S + R_F}{R_S} \qquad (17)$$

TIA AC Analysis

Open Loop Gain

It is imperative to plot the open loop gain of the transimpedance amplifier. This is necessary to understand stability, voltage gain, and the frequency response. When optimizing TIA performance, the A_{OL} can quickly become the limiting factor.

The open loop behavior of an op-amp is the same as a single pole filter. This can be modeled once A_V and GBP are known. First step is to find the amplifiers pole (don't forget to convert A_V from dB to V/V)

$$f_T = \frac{GBP}{A_V} \qquad (18)$$

The transfer function of a single pole filter with a gain of A_V is shown in equation 19 with τ_T being the filters time constant.

$$\frac{V_{OUT}}{V_{IN}}(j\omega) = \frac{A_V}{1 + j2\pi\tau_T} \qquad (19)$$

The inverse of tau results in the cut-off frequency, ω_T.

$$\frac{V_{OUT}}{V_{IN}}(j\omega) = A_{OL}(j\omega) = \frac{A_V}{1 + j\frac{\omega}{\omega_T}} \qquad (20)$$

It is important to note that the load at the amplifiers output can have a significant impact on the open loop response. Read the amplifiers datasheet and perform SPICE simulations to help make that determination on a case-by-case basis. To avoid loading the TIA, the output can be fed into another amplifier.

Feedback Factor, 1/β

1/β allows the designer to better understand noise gain and stability. To properly analyze 1/β the TIA must be accurately modeled as shown in figure 12.

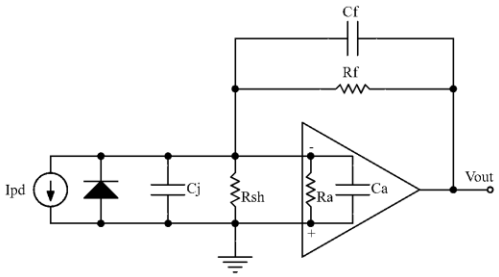

Figure 12. Equivalent Electrical Model of Transimpedance Amplifier

If capacitor C_F is not explicitly placed, it still exists as stray capacitance from the feedback resistor and PCB traces, so it must be modeled.

To simplify the analysis, figure 13 puts the photodiode and amplifier impedances in parallel $R_{IN} = R_{SH} || R_A$ and $C_{IN} = C_J || C_A$.

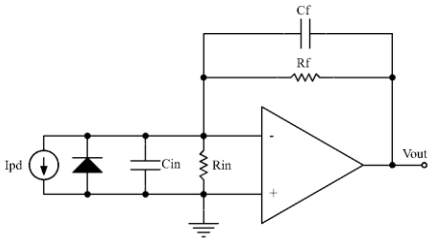

Figure 13. Simplified Equivalent Electrical Model of Transimpedance Amplifier

Taking it one step further, the parallel resistances and capacitances can be modeled as one impedance as shown in figure 14. Remember that the parallel combination of resistors and capacitors must be performed in the frequency (jω) or Laplace (s) domain.

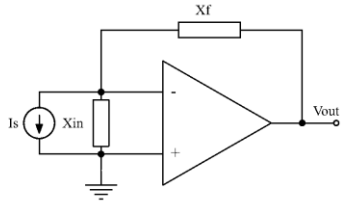

Figure 14. Fully Simplified Electrical Model of Transimpedance Amplifier

Performing a KCL around V_{IN-} in figure 14:

$$\frac{V_{IN-}}{X_{IN}} + \frac{V_{IN-} - V_{OUT}}{X_F} = 0 \qquad (21)$$

$$\frac{V_{OUT}}{V_{IN-}}(j\omega) = \frac{X_{IN} + X_F}{X_{IN}} \qquad (22)$$

$$X_{IN} = R_{IN} || \, C_{IN} = \frac{R_{IN}}{1 + j\omega C_{IN} R_{IN}} \qquad (23)$$

$$X_F = R_F || C_F = \frac{R_F}{1 + j\omega C_F R_F} \qquad (24)$$

Substituting (23) and (24) into (22)

$$\frac{V_{OUT}}{V_{IN-}}(j\omega) = \frac{1}{\beta(j\omega)} = 1 + \frac{R_F + j\omega C_{IN} R_{IN} R_F}{R_{IN} + j\omega C_F R_F R_{IN}} \qquad (25)$$

Equation 25 is the TIA's feedback factor. To analyze individual contributions of the amplifier and photodiode, further expand R_{IN} and C_{IN} per equations 26 and 27.

$$R_{IN} = R_{SH} || R_A = \frac{R_{SH} * R_A}{R_{SH} + R_A} \qquad (26)$$

$$C_{IN} = C_J || C_A = C_J + C_A \qquad (27)$$

Voltage Noise Gain

The voltage noise gain is the total closed loop voltage gain. The amplifiers voltage noise will be multiplied by the voltage noise gain.

$$v_{NG}(j\omega) = \frac{A_{OL}}{1 + A_{OL}\beta} \qquad (28)$$

Figure 14 graphs the open-loop gain, feedback factor, and voltage noise gain vs. frequency. This graph provides a lot of useful information about the design and limitations such as: the DC open loop gain is 100dB, the GBP is 10MHz, the maximum TIA bandwidth is 100kHz, the DC gain is ~0dB and the AC gain is ~25dB, the circuit zero is ~1kHz, the TIA BW is ~16kHz, there will be a noise peak from 1kHz to GBP, and the circuit is stable with a phase margin of 45° < PM < 90°.

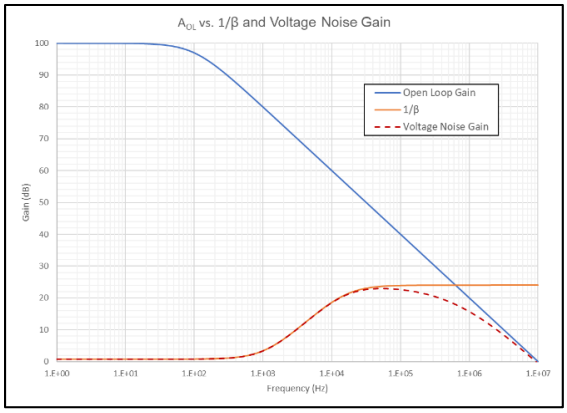

Figure 14. Open Loop Gain Plotted against 1/β and Voltage Noise Gain

Input Impedance

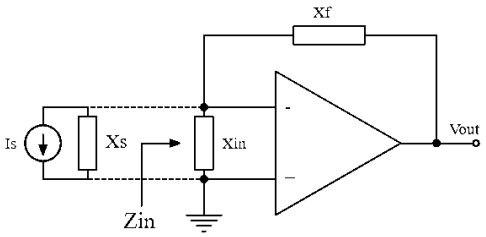

Figure 15. AC Analysis of Op-Amps Equivalent Input Impedance

Expanding on equation (14) from the DC analysis section, the frequency dependent components are added in.

$$Z_{IN}(j\omega) = \frac{V_{IN-}}{I_S} = \frac{1}{\left(\frac{1}{R_A||C_A} + \frac{1+A_{OL}}{R_F||C_F}\right)} \quad (29)$$

$$Z_{IN}(j\omega) = \frac{1}{\frac{1+j\omega R_A C_A}{R_A} + (1+A_{OL})\frac{1+j\omega R_F C_F}{R_F}} \quad (30)$$

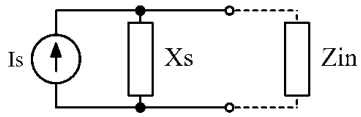

Figure 16. Frequency Dependent Current Divider as Seen by TIA

Figure 17 graphs the input impedance derived in equation (30) alongside the percent of photocurrent transferred to the feedback network as described by figure 16. It can be observed that the input impedance increases with frequency; for lower shunt resistances this introduces a problem of poor efficiency of source current being transferred to the feedback network.

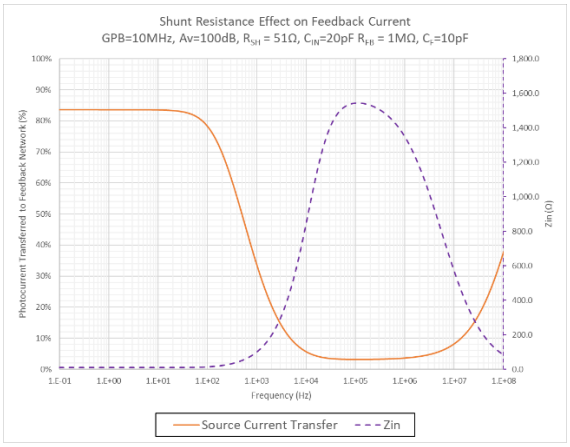

Figure 17. Current Transfer Ratio of Source Current to the Feedback Network with Typical GBP and Gain.

Increasing the gain bandwidth product will keep the current transfer efficiency high over a wider bandwidth and increasing the open loop DC gain will increase the efficiency percent as shown in figure 16.

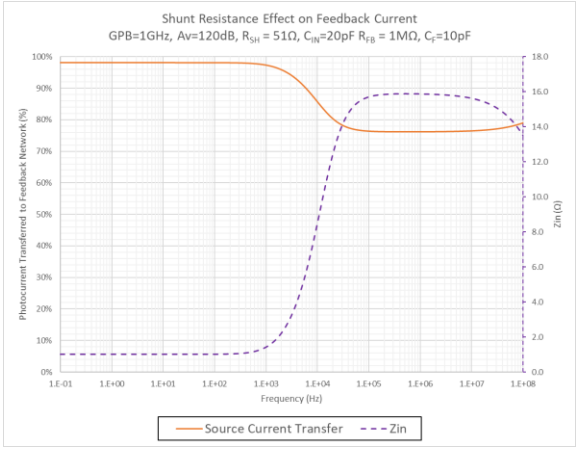

Figure 18. Current Transfer Ratio of Source Current to the Feedback Network with High GBP and Gain.

Transimpedance Frequency Response

The transimpedance gain is expressed in V/A. The closed loop voltage gain's job is to keep the V_{IN+} - V_{IN-} differential voltage at 0V, so the voltage portion of the transimpedance gain will be limited by the open loop gain, not the closed loop gain. The frequency response will also be limited by the open loop bandwidth.

From figure 14 we can KCL around the V_{IN-} node to get equation (31).

$$i_{PD} + \frac{V_{IN-}}{\frac{1}{R_{IN}} + j\omega C_{IN}} + \frac{V_{IN-} - V_{OUT}}{\frac{1}{R_{FB}} + j\omega C_{FB}} = 0 \qquad (31)$$

$$-i_{PD} = (V_{IN-})\frac{1 + j\omega C_{IN}R_{IN}}{R_{IN}} + (V_{IN-} - V_{OUT})\frac{1 + j\omega C_{FB}R_{FB}}{R_{FB}} (32)$$

What we really care about is the transfer function, V_{OUT}/i_{PD}. Equation (32) doesn't inherently allow us to solve for the transfer function. Conveniently, we know the frequency response is limited by the open loop response, so we can sub equation (5) into (32). Remember that A_{OL} is the amplifiers open loop frequency response, not just the DC gain.

$$-i_{PD} = (\frac{V_{OUT}}{-A_{OL}})\frac{1 + j\omega C_{IN}R_{IN}}{R_{IN}} + (\frac{V_{OUT}}{-A_{OL}} - V_{OUT})\frac{1 + j\omega C_{FB}R_{FB}}{R_{FB}} (34)$$

$$\frac{V_{OUT}}{i_{PD}}(j\omega) = \frac{A_{OL}}{\frac{1 + j\omega C_{IN}R_{IN}}{R_{IN}} + (1 + A_{OL})\left(\frac{1 + j\omega C_{FB}R_{FB}}{R_{FB}}\right)} \qquad (35)$$

Figure 19 shows the impact the shunt resistance can have on the transimpedance gain and frequency response.

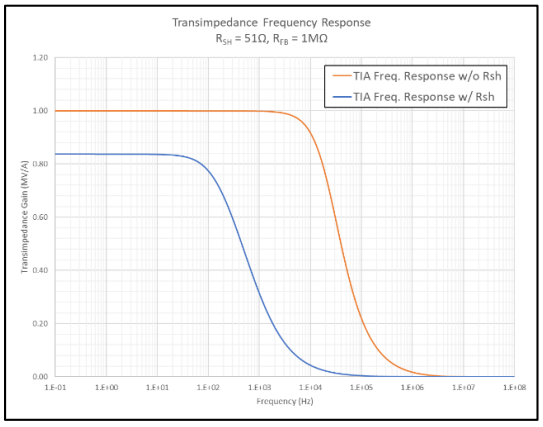

Figure 19. Transimpedance Frequency Response with and without Modeling the Photodiodes Shunt Resistance

The shunt resistance can be ignored when it's very large but must be modeled when it is low as shown in figure 19.

Stability

Rate of Closure

A popular method to determine stability of op amp circuits and transimpedance amplifiers is using rate of closure. The rate of closure method is a way to visually determine the stability of an operational amplifier circuit by examining the intersection of A_{OL} and 1/β.

Rate of Closure (dB/dec)	Phase Margin (°)	Stability
20	45 < PM < 90	Stable
20 < RoC < 40	45	Stable
RoC ≥ 40	0 < PM < 45	Unstable

Table 2. Rate of Closure Stability Criteria

Figure 21 displays various phase margin plots for rate of closure analysis.

Maximum Stable Frequency

It's a good idea to calculate the maximum frequency at which the transimpedance amplifier will still achieve stability. This is done by moving the feedback pole to the intersection of 1/β and the open loop gain then back calculate for the intersection frequency.

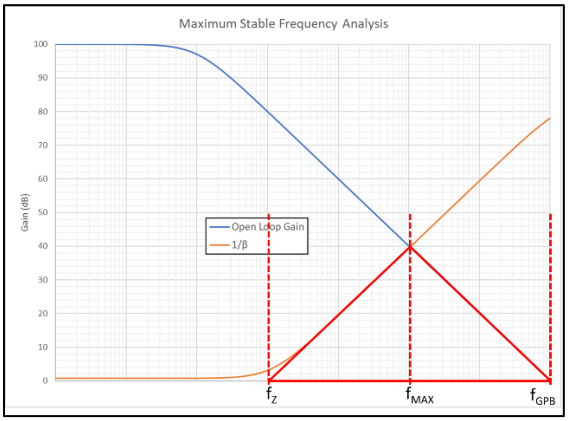

Figure 20. Method to Find the Intersection Frequency Between Open and Closed Loop Gains

The triangle in the bode plot allows the intersection frequency to be solved for.

$$\log(f_{MAX}) = \frac{\log(f_Z) + \log(f_{GBP})}{2} \qquad (36)$$

$$\log(f_{MAX}) = \frac{1}{2} * \log(f_Z * f_{GBP}) \qquad (37)$$

$$\log(f_{MAX}) = \log((f_Z * f_{GBP})^2) \qquad (38)$$

$$f_{MAX} = \sqrt{f_Z * f_{GBP}} \quad (39)$$

f_{GBP}, and f_Z are needed to solve for f_{MAX}. f_{GBP} is known from the amplifier's datasheet f_Z is currently unknown and must be calculated.

$$0 = 1 + \frac{R_F + j\omega C_{IN} R_{IN} R_F}{R_{IN} + j\omega C_F R_F R_{IN}} \quad (40)$$

$$-R_{IN} - j\omega C_F R_F R_{IN} = R_F + j\omega C_{IN} R_{IN} R_F \quad (41)$$

$$f_Z = \frac{R_{IN} + R_F}{2\pi R_{IN} R_F (C_{IN} + C_F)} \quad (42)$$

The f_{MAX} location is the TIA bandwidth.

$$f_{MAX} = \frac{1}{2\pi R_F C_F} \quad (43)$$

Substituting (42) and (43) into (39)

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{(R_{IN} + R_F) * f_{GBP}}{2\pi * R_{IN} R_F (C_{IN} + C_F)}} \quad (44)$$

Equation (44) becomes a second order polynomial with respect to C_F and can be solved with the quadratic formula as seen in equation (45).

$$C_F = \frac{1 + \sqrt{1 + 8\pi f_{GBP} (\frac{R_F^2}{R_{IN}} + R_F) C_{IN}}}{4\pi f_{GBP} (\frac{R_F^2}{R_{IN}} + R_F)} \quad (45)$$

Figure 21 displays the effect the feedback capacitor has on the 1/β term. With C_F not installed, there is insufficient phase margin and the circuit will oscillate. With the minimum C_F installed, the phase margin is 45° and the circuit will be stable. The green plot shows a safer design option with a comfortable amount of phase compensation falling somewhere between 45° and 90°.

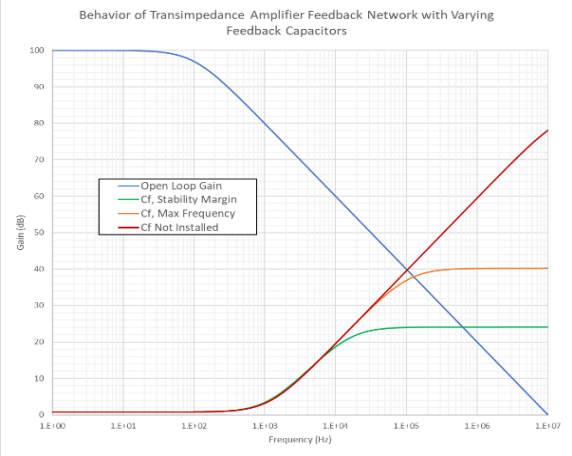

Figure 21. Behavior of Transimpedance Amplifier Feedback Network with Varying Feedback Capacitors

Note that if the DC voltage gain is greater than 0dB ($R_F > R_{SH}$) equation (45) will no longer be valid because the calculated frequency intersection point will have an offset in amplitude. This offset will cause a reduction in maximum calculated bandwidth. Equation (46) is modified to account for this offset by taking the DC gain into account with A_{DC} being in dB.

$$C_F = \frac{1 + \sqrt{1 + 8\pi \frac{f_{GPB}}{10^{A_{DC}/20}} (\frac{R_F^2}{R_{IN}} + R_F) C_{IN}}}{4\pi \frac{f_{GPB}}{10^{A_{DC}/20}} (\frac{R_F^2}{R_{IN}} + R_F)} \quad (46)$$

Also, note that it is possible for the pole to appear before the zero in the bode plot. This situation will occur with low shunt resistor detectors or designs with a very high feedback resistance as seen in figure 22. There isn't a simple approach to solve for the feedback compensation capacitor value from the bode plot. Calculating the phase margin gives better resolution and information pertaining to circuit stability.

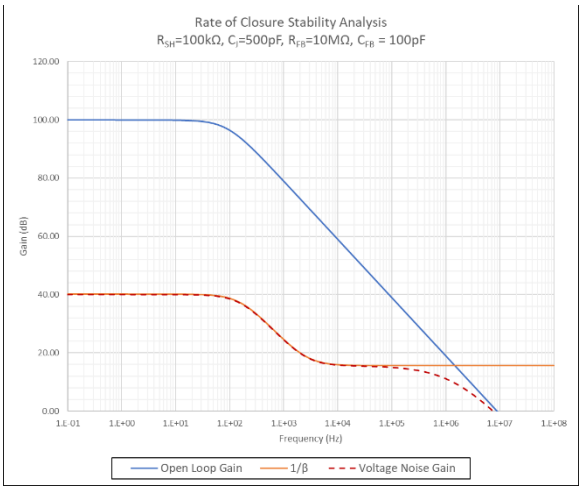

Figure 22. Stability Analysis with the Circuit's Pole Appearing before the Zero

Phase Margin

Rate of closure is useful for quick visual feedback of stability at a single frequency. Calculating the phase margin through the entire bandwidth range will result in a complete picture of the stability. Oscillations will occur if a phase shift of 360° occurs. The phase margin will be the remaining phase angle once the phase of each circuit component is added to 360°. This task seems a bit daunting, but all the hard work of equation derivation is complete, so the phase margin calculation ends up being simple.

The op amp negative feedback accounts for a phase shift of -180°

$$\Phi_{FB} = -180° \tag{47}$$

The amplifiers open loop phase shift will eventually account for -90°. However, we don't want to assume the full phase shift occurs before TIA's zero or pole, so let's mathematically calculate it with respect to frequency.

$$\Phi_A = \frac{180}{\pi}\arctan\left(\frac{\mathbb{I}\{A_{OL}(j\omega)\}}{\mathbb{R}\{A_{OL}(j\omega)\}}\right) \tag{48}$$

The last phase shift component is the feedback factor of the TIA. This can be taken as Φ_β or $-\Phi_{1/\beta}$.

$$\Phi_{\frac{1}{\beta}} = \frac{180}{\pi}\arctan\left(\frac{\mathbb{I}\left\{{}^{1}/_{\beta}\,(j\omega)\right\}}{\mathbb{R}\left\{{}^{1}/_{\beta}\,(j\omega)\right\}}\right) \tag{49}$$

The phase margin becomes:

$$\Phi_{PM} = 360° + \Phi_{FB} + \Phi_A - \Phi_{1/\beta}$$

The rate of closure analysis in figure 23 calculated the minimum stable capacitor to be 0.21pF resulting in a 7.6MHz cut-off frequency and 45° phase margin. The rate of closure phase margin estimate tracks the calculated phase margin at the A_{OL} and 1/β intersection, however, a decade before the intersection the phase margin dipped down to 16°. The circuit will still be stable, but ringing and overshoot will be still present in what was assumed to be a phase compensated design. Reducing the TIA bandwidth an entire order of magnitude will keep the phase margin at a 45° minimum throughout the effective bandwidth.

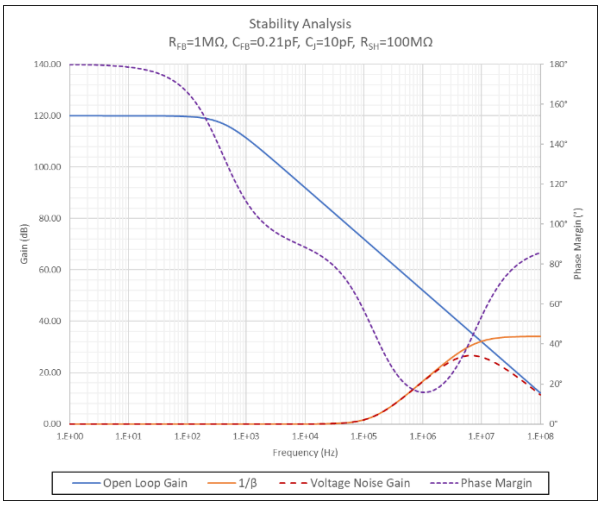

Figure 23. Phase Margin Calculated Over Bandwidth

Maximizing the bandwidth via rate of closure may not always result in an appropriately phase compensated design.

Noise Contributors

There are three main noise contributors in a typical transimpedance amplifier: detector noise, amplifier noise, transimpedance feedback noise. These are all uncorrelated noise sources, so the total noise will be the root-sum-square (RSS) of each noise component.

The purpose of noise modeling is to give insight and some level of confidence as to whether the design will meet the specifications. While it's desirable to be as accurate as possible, remember that it is an estimate and it won't be perfect.

Detector Shot Noise
Shot noise is a statistical noise value related to the fluctuation of photocurrent and dark current. This value is multiplied by the pole of the TIA feedback network to get the frequency response.

$$i_{DSN}(j\omega) = \frac{\sqrt{2 * q * (I_P + I_D)}}{1 + j\omega R_{FB} C_{FB}} \quad (50)$$

Detector Thermal Noise
Like all resistances, the shunt resistance of the photodiode has an associated thermal noise. This value is multiplied by the pole of the feedback network.

$$i_{DTN}(j\omega) = \frac{\sqrt{\frac{4 * k_B * T}{R_{SH}}}}{1 + j\omega R_{FB} C_{FB}} \quad (51)$$

Amplifier Voltage Noise
The amplifiers voltage noise will be multiplied by the total noise gain found in equation (28).

$$e_o(j\omega) = e_n v_{NG} \quad (52)$$

The amplifier's input referred voltage noise contribution in terms of current noise is described in equation (53).

$$i_{AVN}(j\omega) = \frac{e_o}{R_{FB}} \quad (53)$$

Amplifier Current Noise
The amplifier current noise will be the current noise specified in the datasheet multiplied by the pole of the TIA feedback network.

$$i_{ACN}(j\omega) = \frac{i_n}{1 + j\omega R_{FB} C_{FB}} \quad (54)$$

Transimpedance Feedback Noise
The feedback resistor R_F will contribute thermal noise to the circuit. The resistors current noise contribution is multiplied by the pole of the TIA feedback network.

$$i_{FBN}(j\omega) = \frac{\sqrt{\frac{4k_B T}{R_{FB}}}}{1 + j\omega R_{FB} C_{FB}} \quad (55)$$

Total Input Referred Current Noise
The total current noise of the transimpedance amplifier circuit can be found by taking the RSS of each noise contributor.

$$i_{TIA}(j\omega) = \sqrt{i_{DSN}^2 + i_{DTN}^2 + i_{AVN}^2 + i_{ACN}^2 + i_{FBN}^2} \quad (56)$$

Figure 24 is an example current noise graph of TIA that is using a low shunt resistance photodiode. The example design is limited by the amplifier voltage noise.

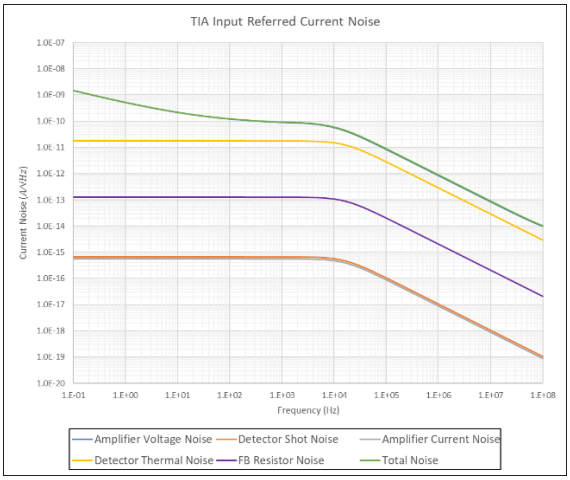

Figure 24. Example of Input Referred Current Noise Graph

Voltage Noise
The total voltage noise can be found by multiplying the total current noise by the feedback resistor R_{FB}

$$v_{TIA} = i_{TIA} R_{FB} \quad (57)$$

Noise Integral
The noise integral is found by taking small bandwidth slices and summing them up. In equation (58) *y* is the total number of bandwidth slices and *Δf* is the size of the bandwidth slice.

$$i_{TOT} = \sum_{x=0}^{y} i_{TIA} \sqrt{\Delta f} \quad (58)$$

Noise Equivalent Power NEP

Noise equivalent power or NEP is defined as the power incident on the detector which results in a signal to noise ratio of 1 in a 1Hz bandwidth. NEP is used to compare noise performance between detectors. For transimpedance amplifiers the NEP is more useful if graphed vs frequency. NEP can be extracted easily at this point in the design as described by equation (59).

$$NEP = \frac{i_{TOT}}{R_\lambda} \qquad (59)$$

Signal-to-Noise Ratio

The signal to noise ratio can be found by dividing the minimum incident power by the NEP at the noise bandwidth of interest. The NEP is power expressed as a SNR of 1, so equation (60) to extracts the SNR.

$$SNR_{NBW} = 10 \log \frac{P_{INCIDENT}}{NEP_{NBW}} \qquad (60)$$

Noise Reduction Techniques

The AC gain of the transimpedance amplifier causes voltage noise peaking from the circuit zero through the gain bandwidth product as observed in figure 14. The voltage noise will usually end up being the dominant noise contributor at frequencies beyond the TIA bandwidth. This results in increased RMS voltage noise at the output. There are a few techniques described in this section to help reduce the noise gain or a portion of the noise bandwidth.

Feedback Capacitor

As we are already well aware, adding a capacitor across the feedback resistor introduces a pole in the circuit response causing the circuit zero to flatten out. Increasing the capacitor, thus decreasing the TIA bandwidth, will reduce the noise by chopping down the AC gain and the voltage noise contribution associated with it.

The takeaway here is that the first step and lowest cost solution to additional phase compensation and noise reduction is to limit the TIA bandwidth as much as the system allows.

Composite Amplifier

The feedback capacitor approach reduces noise due to AC gain (amplitude) and the composite amplifier can be used to reduce noise bandwidth (frequency). Note that this design choice will only provide value if the TIA bandwidth isn't already maximized; there needs to be at least a decade of flat frequency response from the 1/β curve for this method to be effective. The neat thing about this configuration is that the second op-amp isn't required to be an expensive, high-performing, precision device. As long as the first op-amp has the desired performance and available bandwidth, it will compensate for the short-comings of the second op amp such as offset voltage, bias currents, and noise.

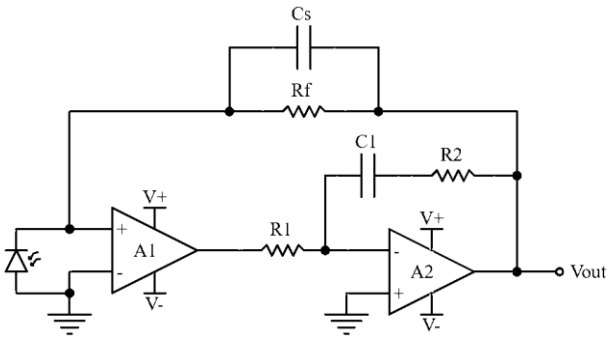

Figure 25. Transimpedance Composite Amplifier Configuration to Shape Open Loop Response for Broadband Noise Reduction

At low frequencies C_1 is open and A_2 operates in open loop. At mid-frequencies A_2 becomes an attenuator as C_1's impedance adds with R_2 for a gain of $-(R_2+X_{C1})/R_1$. R_2 and C_1 also form a zero which shapes the composite amplifiers open loop gain from 40dB/dec back to 20dB/dec for the purposes of stability. At high frequencies C_1 becomes a short making A_2's gain $-R_2/R_1$.

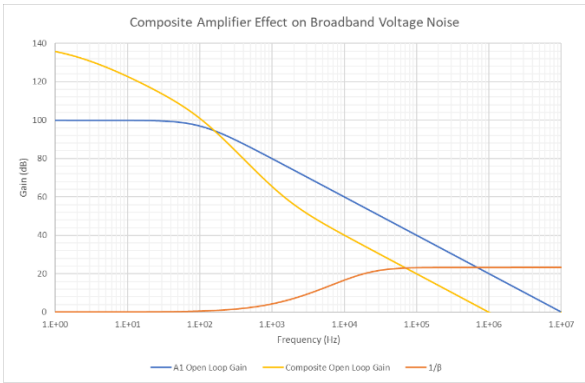

Figure 26. Broadband Voltage Noise Reduction of Composite Amplifier Compared to Classic TIA

The open loop gain of the composite amplifier can be shaped to intersect with the TIA bandwidth which can eliminate a significant amount of broadband noise. In figure 26, the voltage noise will be reduced by the red shaded area. Log charts are deceiving, this will equate to a reduction of $\sqrt{10MHz - 1MHz} = 3000$.

In-Loop Phase Compensation

This is a technique that is more commonly used to drive capacitive loads but is found to be useful for reduction of broadband voltage noise. This circuit is not recommended for use with low shunt resistance photodiodes.

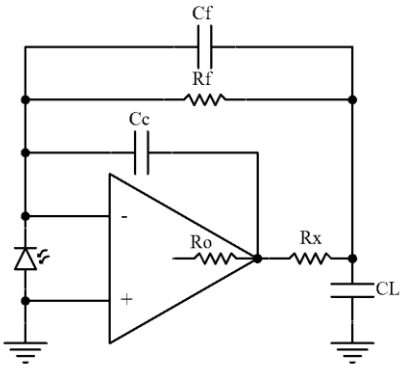

Figure 27. In-Loop Phase Compensation

There are a few design rules to keep in mind: R_X << R_F, R_O << R_{SH}, and R_O = R_X.

This circuit introduces three poles. First is the pole due to the R_F/C_F feedback network.

$$f_{p1} = \frac{1}{2\pi R_F C_F} \quad (61)$$

The next pole is due to the compensation capacitor shorting and taking over the feedback. This adds a second pole in the open-loop gain.

$$f_{p2} = \frac{1}{2\pi (R_O + R_X) C_L} \quad (62)$$

The last pole is introduced under the condition of the load capacitor shorting.

$$f_{p3} = \frac{1}{2\pi [(R_F + R_X) || (R_O + R_{SH})] C_C} \quad (63)$$

The shunt resistance will typically be much larger than the feedback resistance so we can approximate the third pole to be the following:

$$f_{p3} \approx \frac{1}{2\pi (R_F + R_X) C_C} \quad (64)$$

To maintain a sufficient phase margin without sacrificing TIA signal bandwidth all three pole frequencies should be equal.

$$f_{p1} = f_{p2} \rightarrow \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi (R_O + R_X) C_L} \quad (65)$$

$$C_L = \frac{R_F}{R_O + R_X} C_F \quad (66)$$

Setting pole 1 and 3 equal solves for the compensation capacitor C_C.

$$f_{p1} = f_{p3} \rightarrow \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi (R_F + R_X) C_C} \quad (67)$$

$$C_C = \frac{R_F}{R_F + R_X} C_F \approx C_F \quad (68)$$

There is a challenge with this circuit which is empirical tuning of the passive values. Op amp output resistances are usually not well defined in datasheets or accurately modeled in SPICE. All the values in circuit rely on R_O as a starting point for the design. If R_O can't be reasonably estimated, call it 50Ω and be prepared to empirically tune the circuit.

Bootstrapping

Bootstrapping in electronics is the idea to feed the output signal back to the input usually for the purpose of increasing the input impedance. Bootstrapping in a transimpedance amplifier design refers to reducing the effective photodiode capacitance by eliminating voltage swings across the photodiode. A capacitor will significantly lose its effectiveness if its voltage potential is always zero. If the photodiode capacitance is larger than a few tens of pico-farads, this design technique can have positive benefits with respect to reduced noise and increased bandwidth.

JFET Source Follower Bootstrap

For low light applications an effective choice is bootstrapping the photodiode with a JFET. If the correct transistor is chosen, a JFET source follower will have: a gain of nearly unity, very low voltage noise (<2nV/√Hz), low input capacitance (<10pF), and low gate current (<1pA). The single JFET bootstrap configuration can be seen in figure 28.

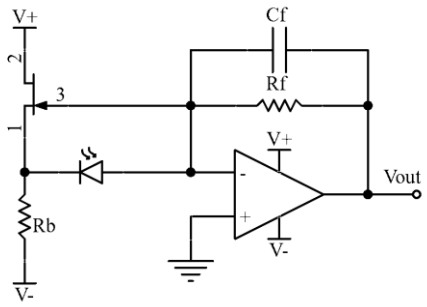

Figure 28. JFET Bootstrap for Low Photocurrent Applications

The signal at V_{IN-} is mirrored to the JFET source due to the nearly-unity gain source follower stage. This will keep the differential voltage across the photodiode constant, thus reducing the effects of the junction capacitance. The feedback network is now looking back into the gate of the JFET instead of directly into the photodiode. The effective input capacitance can be estimated as equation (69) although this estimation will be truer for figure 29. V_{GS} in figure 28 will fluctuate with changes in photocurrent, so a fraction of C_J will also be present. The Art of Electronics Third Edition pp. 547 takes a SWAG that $\frac{1}{10}C_J$ will be still present in the effective input capacitance of figure 28.

$$C_{IN(effective)} = C_A + C_{ISS} \qquad (69)$$

A drawback to figure 28, is that it puts a reverse bias voltage of V_{GS} across the diode. Photodiodes designed to be operated in photovoltaic mode cannot withstand much reverse bias voltage. Reverse voltage can be more effectively nulled out with a matched pair of JFETs as seen in figure 29.

Zero Bias JFET Source Follower Bootstrap

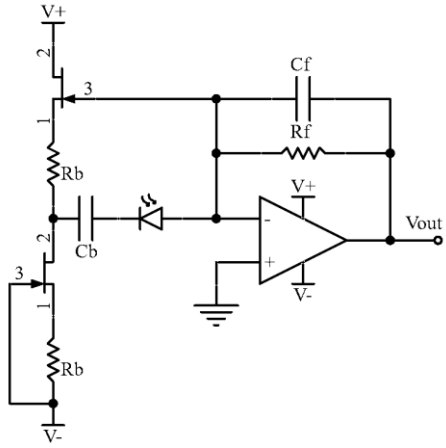

Figure 29. Zero Bias JFET Source Follower Bootstrap

An improvement to the single JFET bootstrap is the Zero Bias JFET Source Follower Bootstrap. The matched JFETs and current setting resistors will split the rail in half at the buffer output resulting in a zero bias across the photodiode, assuming |V+| = |V-|.

Improved Zero Bias JFET Source Follower

The improvement of the circuit in figure 30 comes from the feedback provided by Q1 and J1. When photocurrent flows, the current demand from J2 and R2 changes which causes current through J1 and R1 to change as well. This change is realized at the base of Q1 which modifies the collector current by $\beta_{Q1}*\Delta I_B$. The PNP feedback causes a reduction in the source follower output impedance by a factor of β_{Q1}. This is beneficial because as the output impedance of the source follower decreases, so does the voltage potential across the diode.

When choosing components, J1 and J2 must be matched. R1 and R2 should be closely matched. The PNP transition frequency should be larger than the photodiodes rise/fall times, and ideally have a large β.

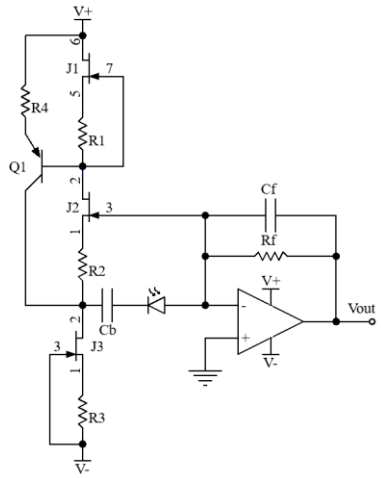

Figure 30. Improved Zero Bias JFET Source Follower Bootstrap. Photodiode Amplifiers Op Amp Solution, by J. Graeme, McGraw Hill,1995, p. 81.

BJT Cascode Bootstrap

Dr. Philip Hobbs designed and popularized a BJT photodiode front end which reduces noise and increases bandwidth when compared with a traditional TIA design. This design does have an issue which is part obsolescence. This design was intended for photocurrent sensitivity down to the 1's of micro-amps range. The datasheets lead me to believe it will still be effective in the nano-amp range, however, proceed with caution or use the JFET approach in the pico-amp range. As it stands, this design assumes a very high shunt resistance; as the shunt resistance decreases the output voltage will experience a DC offset, but this can be easily mitigated. This design will also put a reverse bias voltage of about 9V across the diode, ensure the photodiode can operate in photoconductive mode. Calculate the dark current contribution to shot noise to make sure it won't give you any headaches.

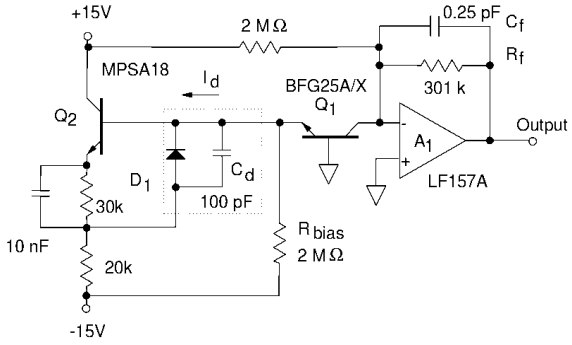

Figure 20. Bootstrapped TIA Design from "Photodiode Front Ends The Real Story" by Dr. Philip B.D. Hobbs

Dr. Hobbs has a few other bootstrap ideas and designs in his book "Building Electro-Optical Systems: Making it all Work". They are not included here as they are similar in spirit to Improved Zero Bias JFET Source Follower.

References

Brisebois, G. (2006). *Low Noise Amplifiers for Small and Large Area Photodiodes.* Retrieved from Design Note 399: https://www.analog.com/media/en/reference-design-documentation/design-notes/dn399f.pdf

Burr-Brown. (1994, February). *Noise Analysis of FET Transimpedance Amplifiers.* Retrieved from https://www.ti.com/lit/an/sboa060/sboa060.pdf

Graeme, J. G. (1991, June). *Feedback Plots Define Op Amp AC Performance.* Retrieved from https://www.ti.com/lit/an/sboa054/sboa054.pdf?ts=1711459510378

Graeme, J. G. (1993, January). *Op Amp Performance Analysis.* Retrieved from https://www.ti.com/lit/an/sboa054/sboa054.pdf?ts=1711459510378

Hobbs, P. C. (2001, April). Photodiode Front Ends The real story. *Optics & Photonics News*.

Horowitz, P., & Hill, W. (1989). *The Art of Electronics (2nd Ed.).* Cambridge University Press.

Horowitz, P., & Winfield, H. (2015). *The Art of Electronics (3rd Ed.).* Cambridge University Press.

Hoyle, C., & Peyton , A. (1998). Bootstrapping Techniques to Improve the Bandwidth of Transimpedance Amplifiers. *IEE Colloquium on Analog Signal Processing (Ref. No. 1998/472).* Oxford: IET.

Kay, A. (2014). *Analysis and Measurement of Intrinsic Noise In Op Amp Circuits Part II: Introduction to Op Amp Noise.* Retrieved from https://www.ti.com/lit/ml/slyy061/slyy061.pdf

Mackowiak, V., Peupelmann, J., Ma, Y., & Gorges, A. (n.d.). *NEP - Noise Equivalent Power.* Retrieved from https://www.thorlabs.com/images/TabImages/Noise_Equivalent_Power_White_Paper.pdf

OSI Optoelectronics. (n.d.). *Photodiode Characteristics and Applications.* Retrieved from https://www.osioptoelectronics.com/media/pages/knowledgebase/b954012b64-1675100541/an-photodiode-parameters-and-characteristics.pdf

Vishay. (1997, March 10). *The FET Constant-Current Source/Limiter.* Retrieved from AN103: https://www.vishay.com/docs/70596/70596.pdf