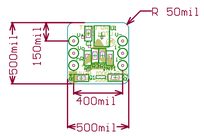
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	TOP SILK				
	TOP SOLDER	Solder Resist	0.40mil	3.5	
1	TOP COPPER	Copper	1.40mil		
	CORE	FR-4	58.00mil	4.8	
2	BOTTOM COPPER	Copper	1.40mil		
	BOTTOM SOLDER	Solder Resist	0.40mil	3.5	
	BOTTOM SILK				

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape
□	6	12.00mil (0.305mm)	PTH	Round	TOP COPPER - BOTTOM COPPER	Via	Rounded
⌖	6	39.00mil (0.991mm)	PTH	Round	TOP COPPER - BOTTOM COPPER	Pad	Rounded
	12 Total						

REVISION RECORD			
REV	DESCRIPTION	APPROVED:	DATE:
1	ZERO DRIFT LATCHING COMPARATOR	JPETRILLI	24.Nov.2020

NOTES:
1. FINAL BOARD THICKNESS TO BE +/-10% OF TOTAL SHOWN IN LAYER STACK UP DETAIL.
2. FABRICATE IN ACCORDANCE WITH IPC-D-610, LATEST REV.
3. SOLDER MASK FOR TOP AND BOTTOM IS BLUE LPI.
4. APPLY SILKSCREEN TO BOTH SIDES USING WHITE EPOXY INK.
5. WARP AND TWIST NOT TO EXCEED .010 PER INCH.
6. ALL DIMENSIONS ARE IN INCHES, HOLES SIZES ARE FINISHED SIZES.
7. THIS IS A 4 LAYER BOARD. REFER TO THE LAYER DETAIL.
8. BOARDS TO BE CLEAN AND FREE OF FOREIGN MATERIAL.
9. BREAK ALL SHARP CORNERS.
10. FINISH TO BE ENIG AND COMPLY WITH IPC-4552 LATEST REV.
11. BOARD MUST BE RoHS/WEEE COMPLIANT.
12. THIS BOARD IS 6/6MIL TRACE/CLEARANCE MINIMUM DESIGN RULES
13. PCB FABRRICATOR TO APPLY UL MARK, 94V-0 AND DATE CODE.
14. TOLERANCES ARE NOT CUMULATIVE
15. PCB OUTLINE SHOWN ON 'Board Outline' or 'Mechanical 2' LAYER AND IS FOR REF. ONLY DO NOT PLACE OUTLINE ON FINAL PCB.
16. BARE PCB CLEANLINES SHOULD BE IN ACCORDANCE WITH IPC-5704
17. REFLOW SOLDERING SPECIFIED BY J-STD-020D. DO NOT EXCEED 250C



COMPANY: ANALOG DESIGN REF.		DIVSION: NEW PRODUCT INTRODUCTION	
TOLERANCES: .XX ±.01 .XXX ±.002 ANGLES ±1 °	DRAWN: JPETRILLI	TITLE: FABRICATION DRAWING, ZERO DRFT LTCH CMP	
	DATED: 24.Nov.2020	CODE:	SIZE: B / DRAWING NO: 40001 / REV: 1
		SCALE:	SHEET: 1 OF 1