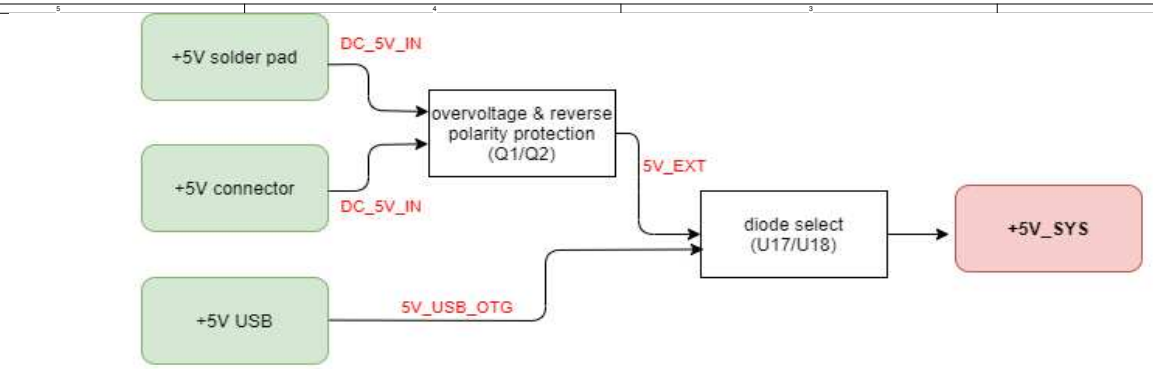
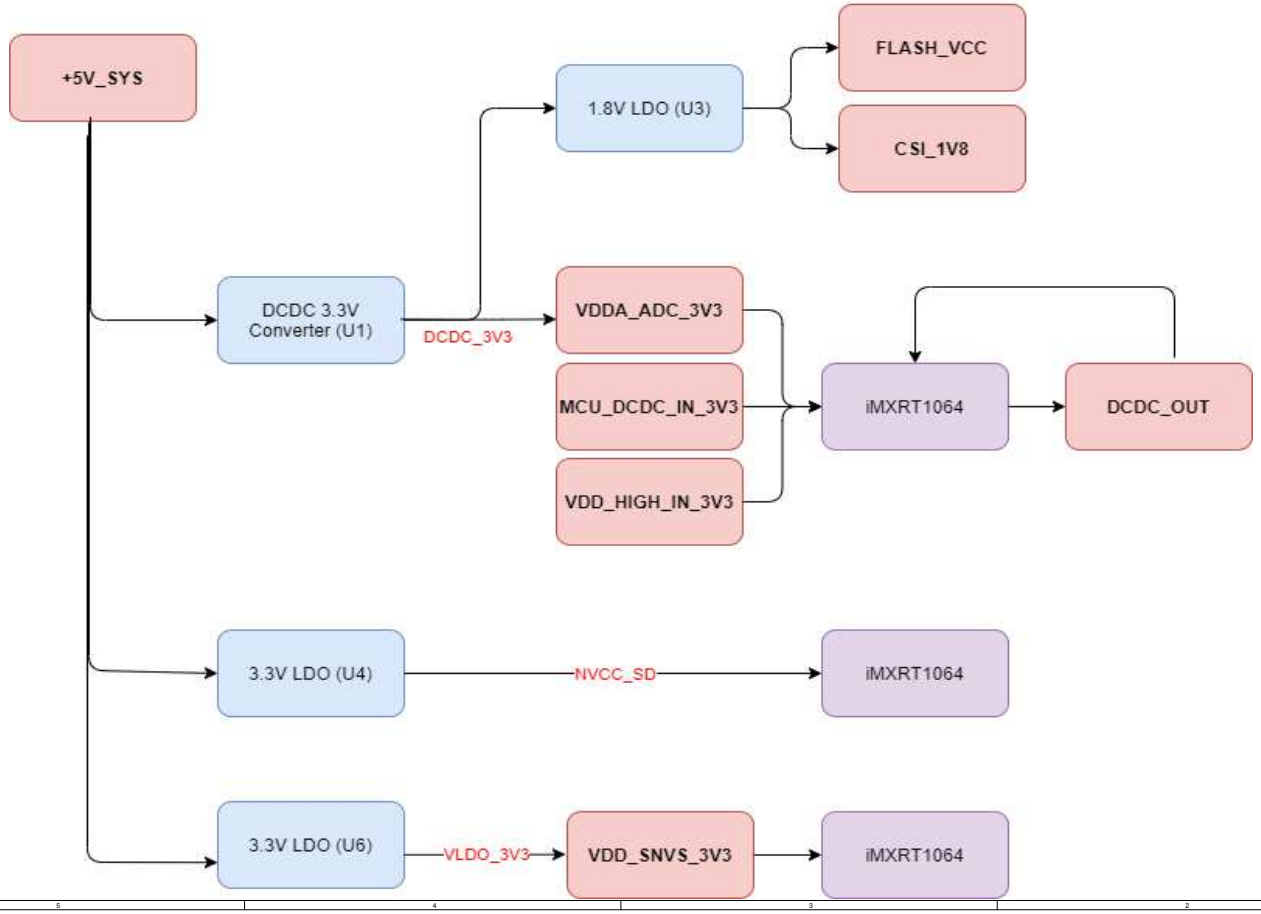
POWER DIAGRAM





Title	POWER DIAGRAM	
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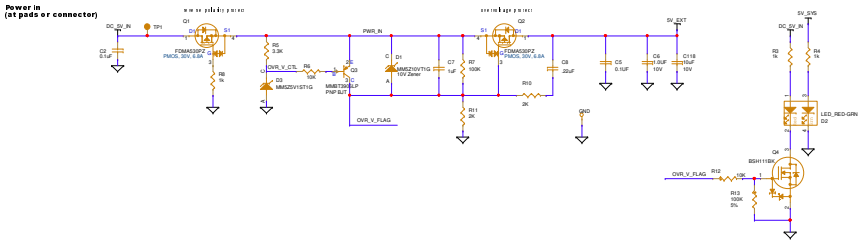
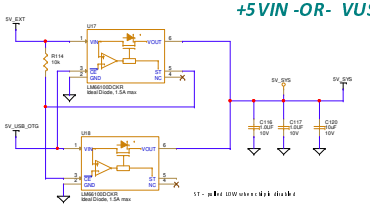
POWER SUPPLIES

+5VIN

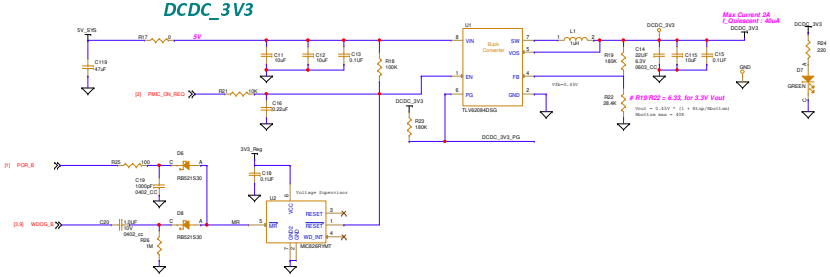


POWER INPUT SELECT:
+5VIN -OR- VUSB

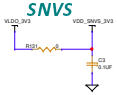


POWER DISTRIBUTION

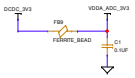
DCDC_3V3



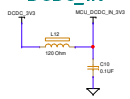
SNVS



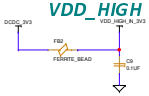
ADC



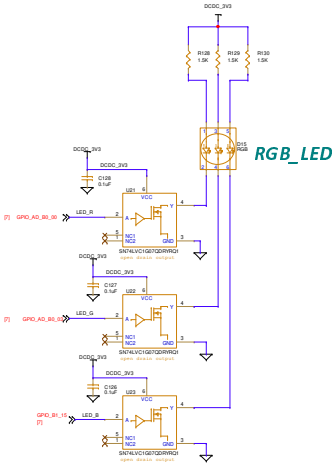
DCDC_IN



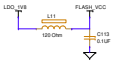
VDD_HIGH



RGB_LED



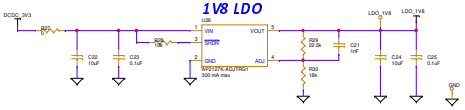
FLASH



USER LED

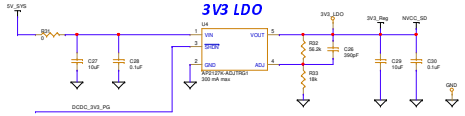
FLASH VCC

1V8 LDO



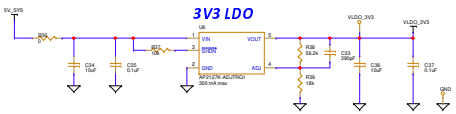
NVCC_SD

3V3 LDO

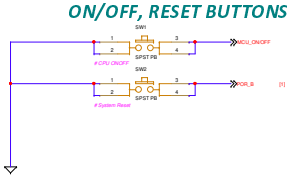


SNVS

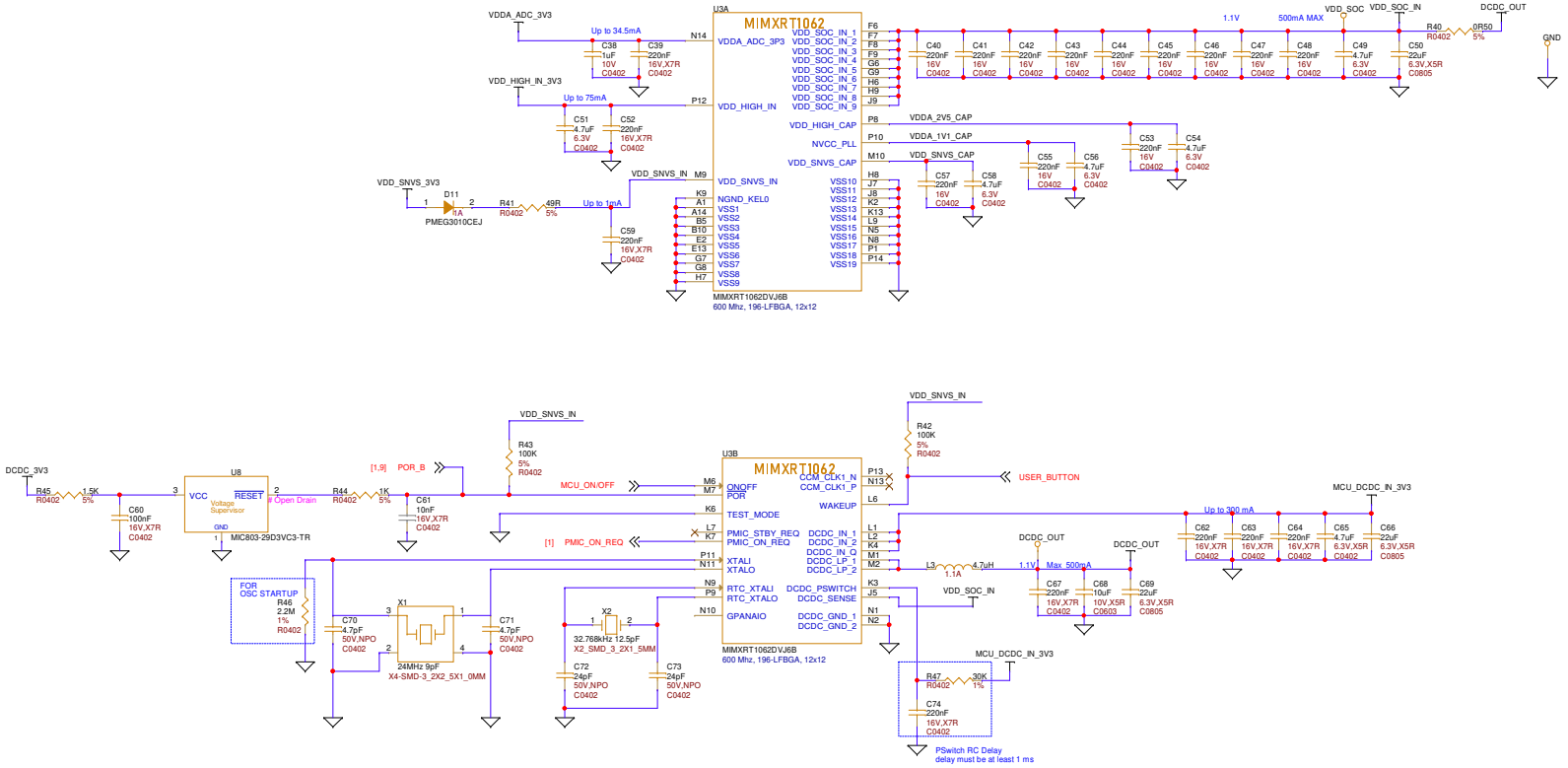
3V3 LDO



ON/OFF, RESET BUTTONS



MCU POWER



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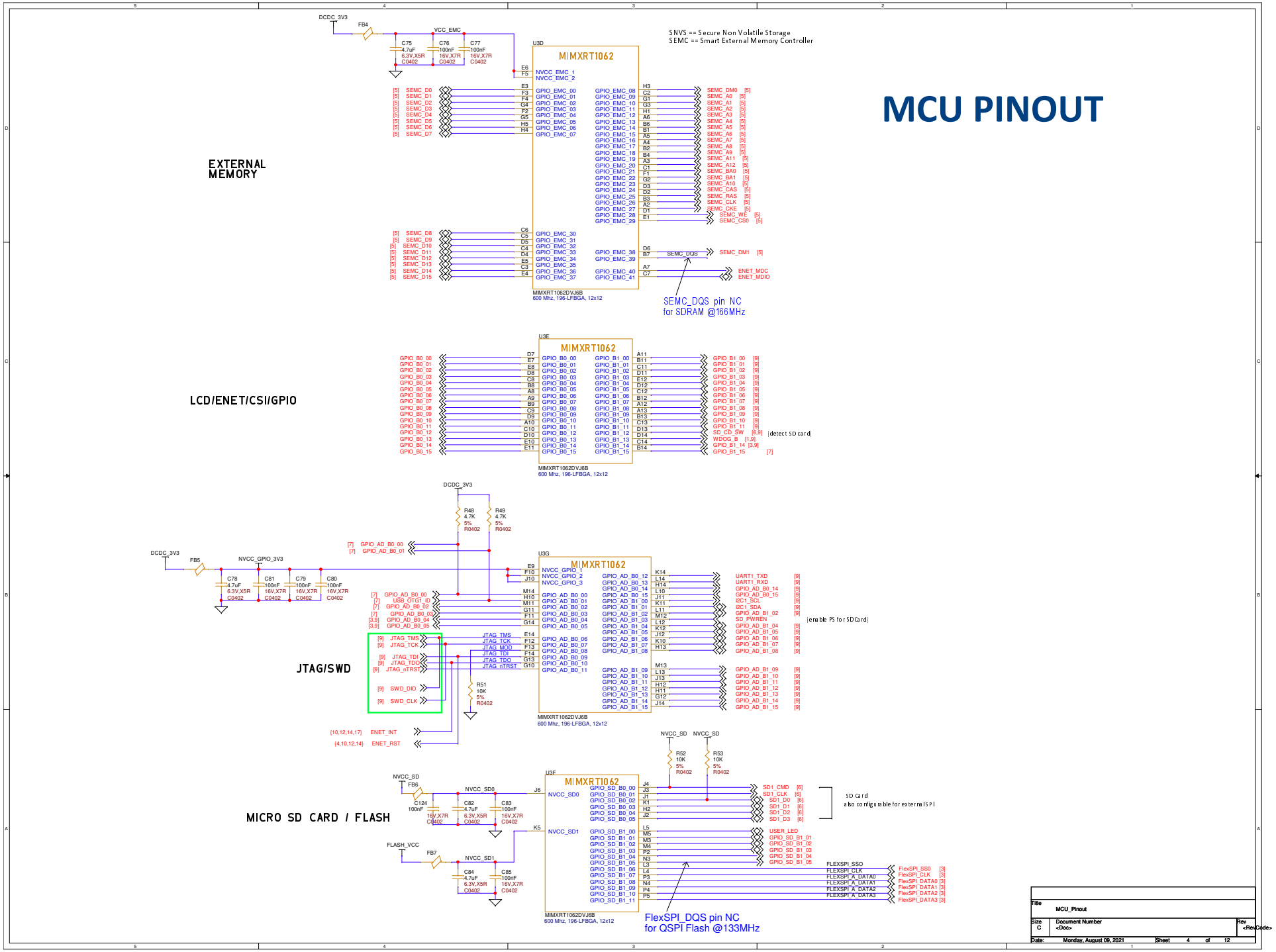
MCU PINOUT
SNVS == Secure Non Volatile Storage
SEMC == Smart External Memory Controller
EXTERNAL MEMORY
LCD/ENET/CSI/GPIO
JTAG/SWD
MICRO SD CARD / FLASH
MIMXRT1062
MIMXRT1062DVJ6B
600 Mhz, 196-LFBGA, 12x12
SEMC_DQS pin NC
for SDRAM @166MHz
FlexSPI_DQS pin NC
for QSPI Flash @133MHz
SD Card
also configurable for external SPI
Title
MCU_Pinout
Size
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Document Number
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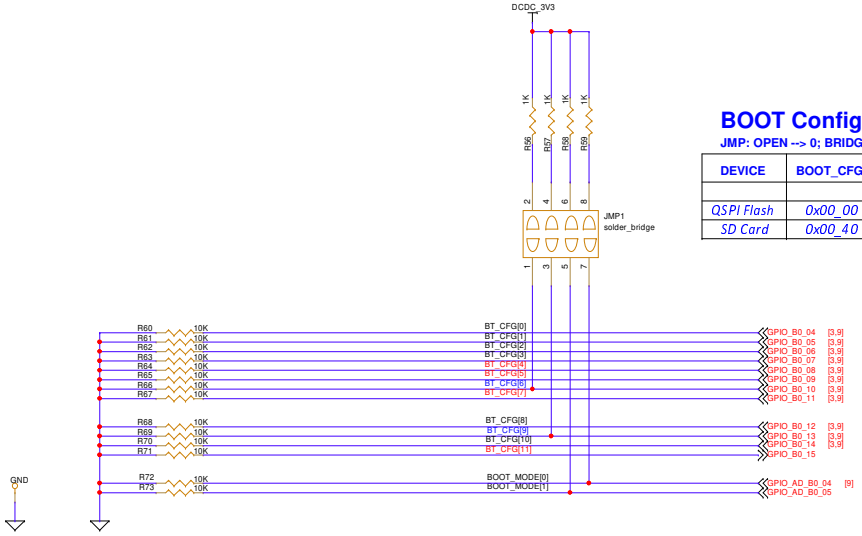
MCU BOOT



BOOT Configuration

JMP: OPEN --> 0; BRIDGED --> 1

DEVICE	BOOT_CFG	JUMPER
QSPI Flash	*0x00_00*	*0, 0, 1, 0*
SD Card	*0x00_40*	*1, 0, 1, 0*

FUSE MAP

	0/1	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*	*0/1*
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR*			*0*	*0*	*0*	*0*	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*EncryptedXIP 0 - Disabled 1- Enabled*	*Reserved*
SD	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*Reserved*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V*	*0*	*1*	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*

Title	MCU_Boot		
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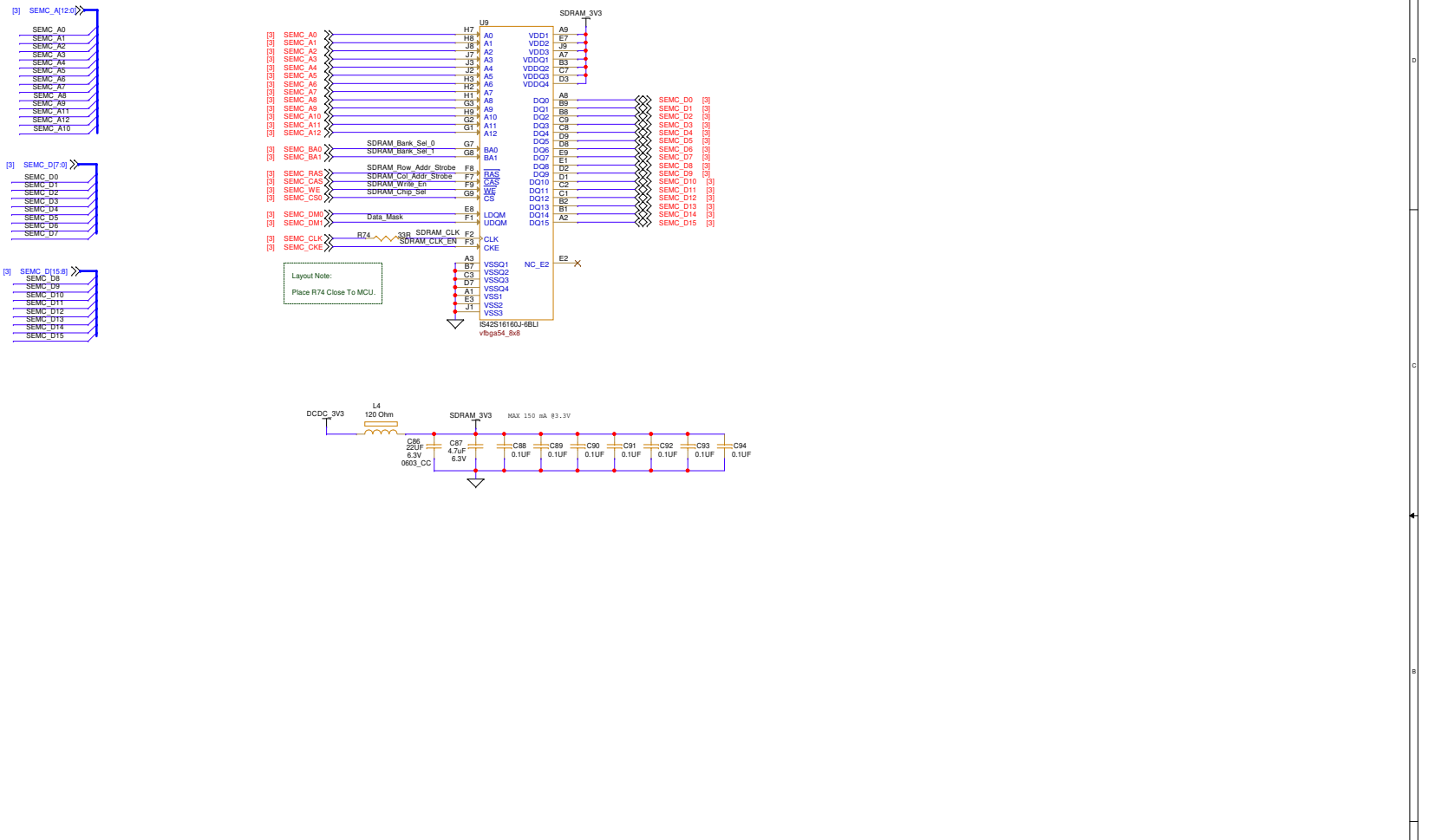
SDRAM 32MB



Title	RAM	
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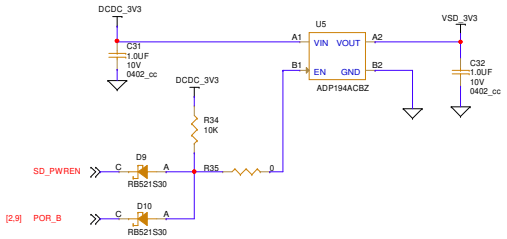
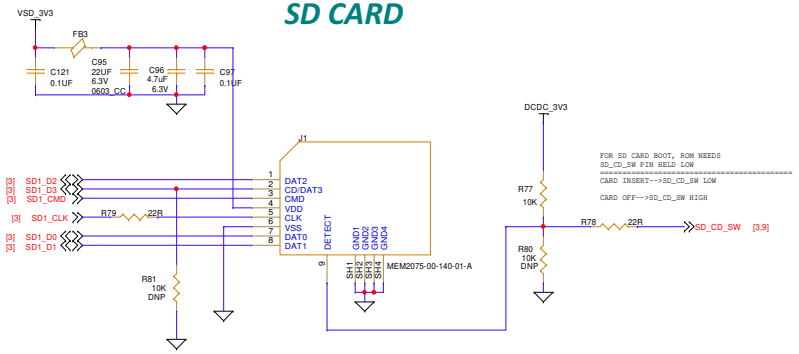
SD CARD

SD CARD POWER SWITCH



SD CARD



Title	SD CARD	
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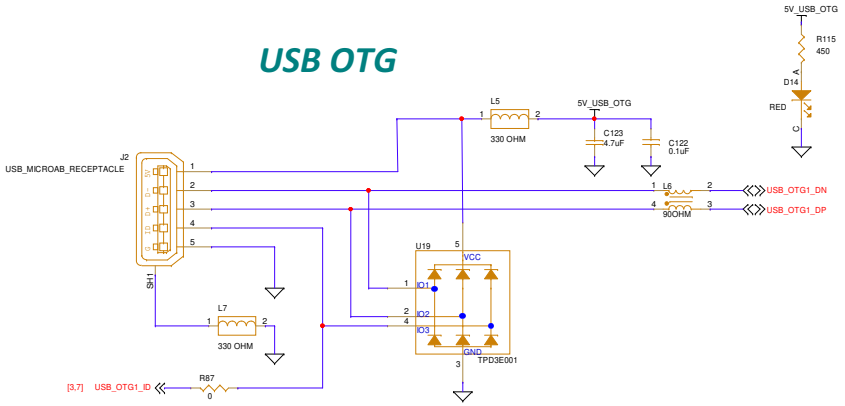
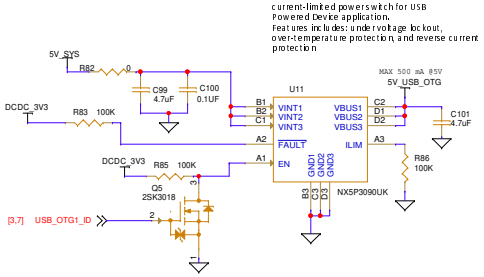
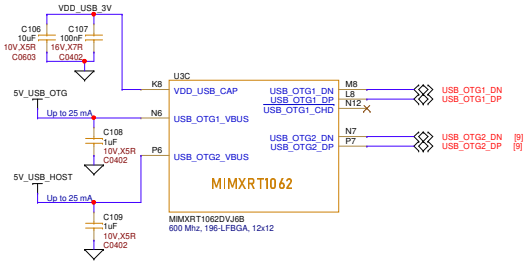
USB

USB OTG



USB POWER





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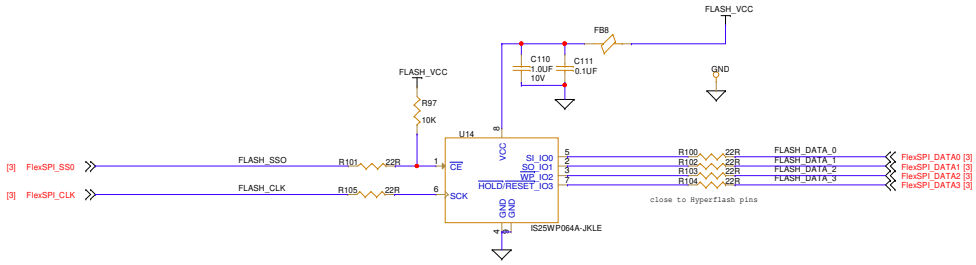
FLASH

1V8 QSPI Flash



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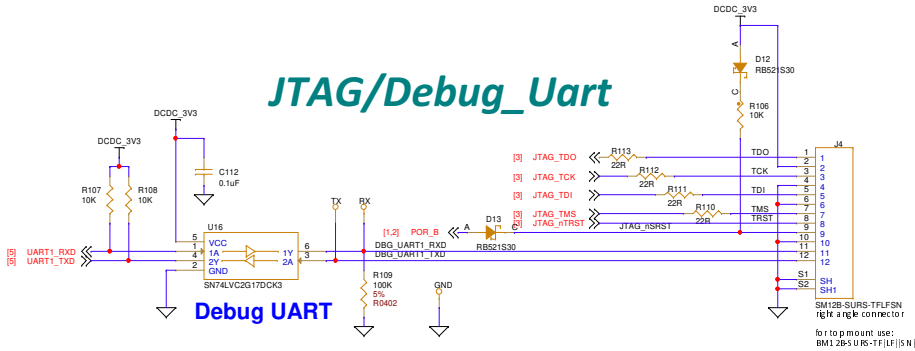
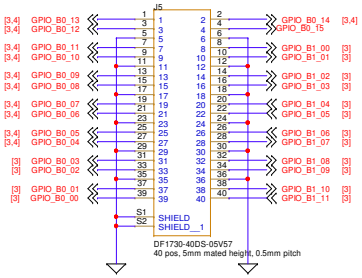
CONNECTORS

JTAG/Debug_Uart



LCD_Interface

HIROSE RECEPTACLE
DF17(3.0)-40DS-0.5V(57)



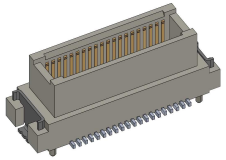
USB/CSI/ENET_Interface

HIROSE
DF17(3.0)-40DS-0.5V(57)

Mating Connectors:

HIROSE DF17(2.0)-40DP-0.5V(57)
Digikey PN: H11130TR-ND
Board -> Board Stacking Height == 5mm

HIROSE DF17(4.0)-40DP-0.5V(57)
Digikey PN: H11144TR-ND
Board -> Board Stacking Height == 7mm



Title	MCU_Connectors	
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ALT PINS

GPIO_EMC[00:07]

Signal	Default	ALT0	ALT1	ALT2	ALT3	ALT4
SEMC_D0	ALT5	SEMC_D0	PWM4_0_A	SPI2_SCLK	XBAR_02	FLEXIO_00
SEMC_D1	ALT5	SEMC_D1	PWM4_0_B	SPI2_CS0	XBAR_03	FLEXIO_01
SEMC_D2	ALT5	SEMC_D2	PWM4_1_A	SPI2_SDO	XBAR_04	FLEXIO_02
SEMC_D3	ALT5	SEMC_D3	PWM4_1_B	SPI2_SDI	XBAR_05	FLEXIO_03
SEMC_D4	ALT5	SEMC_D4	PWM4_2_A	SAI2_TX_DATA	XBAR_06	FLEXIO_04
SEMC_D5	ALT5	SEMC_D5	PWM4_2_B	SAI2_TX_SYNC	XBAR_07	FLEXIO_05
SEMC_D6	ALT5	SEMC_D6	PWM2_0_A	SAI2_TX_BCLK	XBAR_08	FLEXIO_06
SEMC_D7	ALT5	SEMC_D7	PWM2_0_B	SAI2_MCLK	XBAR_09	FLEXIO_07

GPIO_EMC[30:37]

Signal	Default	ALT0	ALT1	ALT2	ALT3	ALT4
SEMC_D8	ALT5	SEMC_D08	PWM3_B0	UART6_CTS_B	SPI1_CS0	CSI_DATA23
SEMC_D9	ALT5	SEMC_D09	PWM3_A1	UART7_TXD	SPI1_CS1	CSI_DATA22
SEMC_D10	ALT5	SEMC_D10	PWM3_B1	UART7_RXD	PMIC_RDY	CSI_DATA21
SEMC_D11	ALT5	SEMC_D11	PWM3_A2	SDHC1_RST_B	SAI3_RX_DAT	CSI_DATA20
SEMC_D12	ALT5	SEMC_D12	PWM3_B2	SDHC1_VSEL	SAI3_RX_SYNC	CSI_DATA19
SEMC_D13	ALT5	SEMC_D13	XBAR1_18	GPT1_CMP1	SAI3_RX_BCLK	CSI_DATA18
SEMC_D14	ALT5	SEMC_D14	XBAR1_22	GPT1_CMP2	SAI3_TX_DATA	CSI_DATA17
SEMC_D15	ALT5	SEMC_D15	XBAR1_23	GPT1_CMP3	SAI3_MCLK	CSI_DATA16

Title	ALT PIN TABLES	
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LAYOUT GUIDELINES

Routing guidlines for MIPI & LVDS

1)All differential routes are required to have the same length between the positive (true) and the negative (complimentary) routes.
Spacing between the positive (true) and the negative (complimentary) shall be 2 times trace width.

2)Target differential impedance shall be 100 Ohms

3)Trace length matching to be within 1.0 mm (40 mil) across the entire bus.

4)Use small humps for skew corrections

5)Place signal vias close together and remove copper in between vias.
Traces to be fully shielded with GND stitching terminating at both trace end points

6)Board trace impedance results must be within ±10 percent of target and
Power plane impedance to be within +/- 10 percent of target at operating frequency

MIPI &LVDS Simulation Requirement

1)MIPI Differential Mode insertion Loss shall be > -1.6dB at 750 MHz

2)MIPI Differential Mode Return Loss shall be < -15dB at 750 MHz

3)MIPI Common Mode Return Loss shall be < -15dB at 750 MHz

4)LVDS differential mode return loss shall be < -16.5db at 600 MHz

5)LVDS common mode return loss shall be < -16.5db at 600 MHz

6)LVDS insertion loss shall be > -1.7db at 600 MHz

7)LVDS Cross coupling shall be < -22 dB for victim IO at 600MHz

8)Power plane impedance to be within +/- 10 percent of target at operating frequency

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