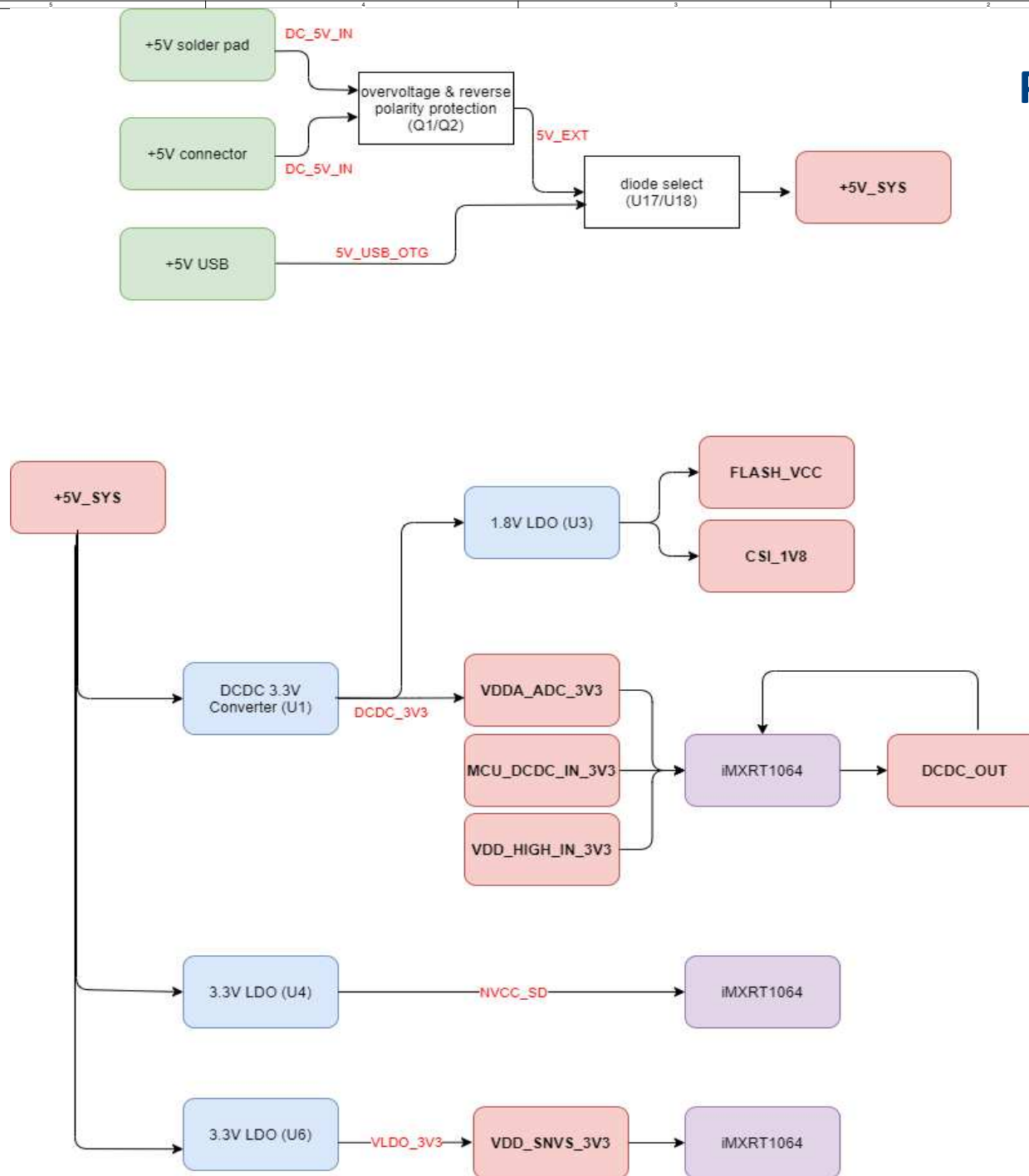
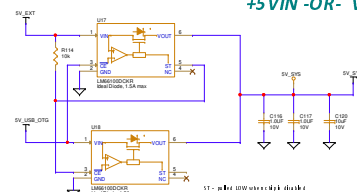


# POWER DIAGRAM

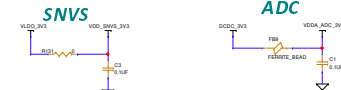


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**POWER INPUT SELECT:**  
**+5VIN -OR- VUSB**



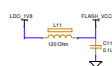
**ADC**



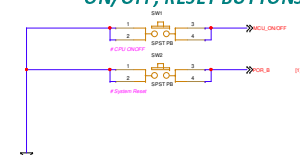
*VDD\_HIGH*



*USER LED*



### ON/OFF, RESET BUTTONS



File		Power Supplies	
Doc ID	Document Number	<Doc>	
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# MCU POWER

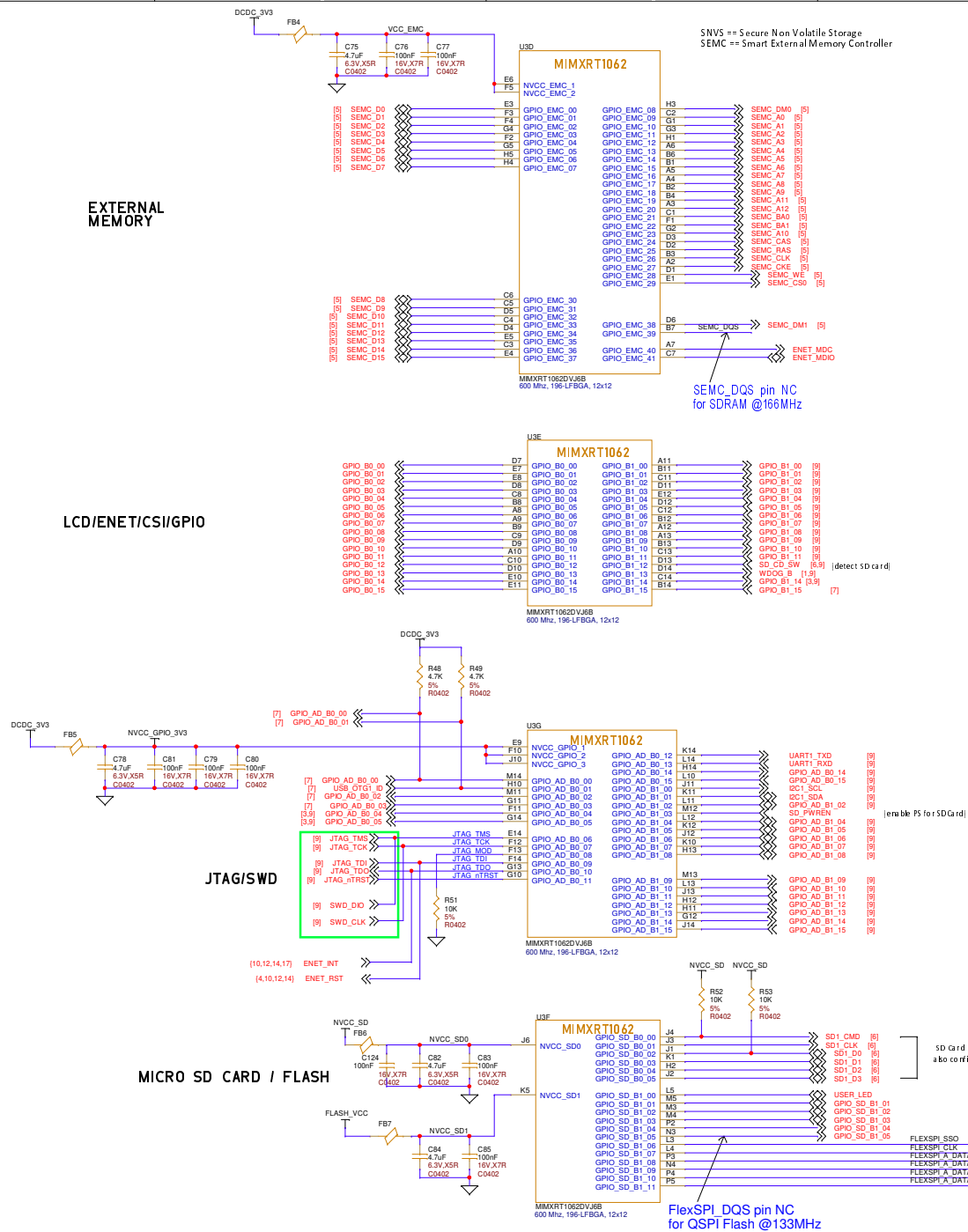
This schematic diagram illustrates the power management for the MIMXRT1062 microcontroller. It shows the internal power blocks (VDDA, VDD, VDD\_HIGH, VDD\_SNVS, VSS) and their connections to external components. Key features include:

- Power Input:** VDDA\_ADC\_3V3 and VDD\_HIGH\_IN\_3V3 are connected to the VDDA and VDD pins, respectively.
- Internal Power Blocks:** VDDA\_ADC\_3P3, VDD\_HIGH\_IN, VDD\_HIGH\_CAP, VDD\_SNVS\_CAP, VDD\_SNVS\_IN, and VSS are shown with their respective pins and connections.
- Capacitors:** Various capacitors (C38, C39, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74) are used for decoupling and filtering.
- Resistors:** Resistors (R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100) are used for current limiting and pull-up/pull-down.
- Connectors:** The diagram shows connections to various connectors (J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32, J33, J34, J35, J36, J37, J38, J39, J40, J41, J42, J43, J44, J45, J46, J47, J48, J49, J50, J51, J52, J53, J54, J55, J56, J57, J58, J59, J60, J61, J62, J63, J64, J65, J66, J67, J68, J69, J70, J71, J72, J73, J74, J75, J76, J77, J78, J79, J80, J81, J82, J83, J84, J85, J86, J87, J88, J89, J90, J91, J92, J93, J94, J95, J96, J97, J98, J99, J100).
- Notes:** The diagram includes several notes, such as "Up to 34.5mA", "Up to 75mA", "Up to 1mA", "Up to 300mA", and "Pswitch RC Delay delay must be at least 1 ms".

The schematic is a detailed representation of the MCU power system, showing the internal and external components and their connections. It is a critical part of the hardware design for the MIMXRT1062 microcontroller.

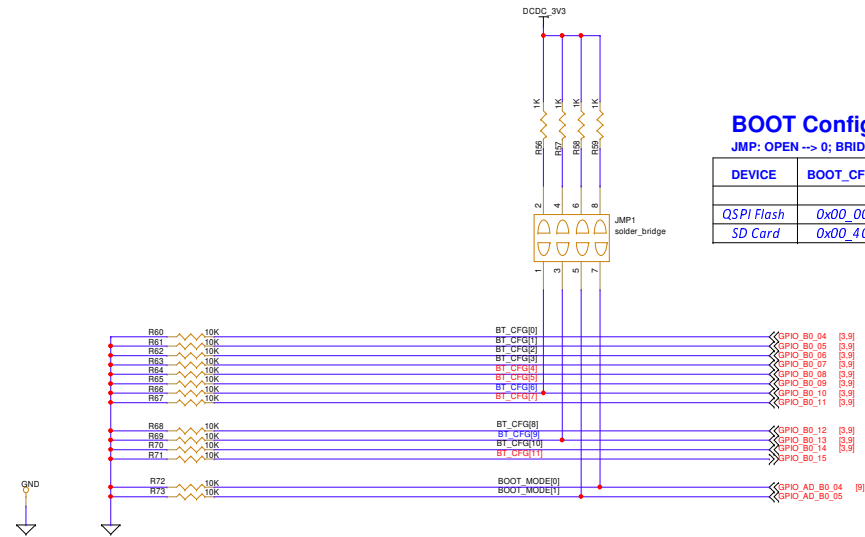
Title MCU Power		
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## MCU PINOUT



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MCU_Pinout			
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# MCU BOOT



## BOOT Configuration

JMP: OPEN --> 0; BRIDGED --> 1

DEVICE	BOOT_CFG	JUMPER
QSPI Flash	0x00_00	0, 0, 1, 0
SD Card	0x00_40	1, 0, 1, 0

## FUSE MAP

TYPE	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]	BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
FlexSPI1 - Serial NOR	Infinite-Loop: (Debug USE only) 0 - Disable 1 - Enable	FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR			0	0	0	0	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		EncryptedXIP 0 - Disabled 1 - Enabled	Reserved
SD	Infinite-Loop: (Debug USE only) 0 - Disable 1 - Enable	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V	0	1	SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad	SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct	Port Select: 0 - eSDHC1 1 - eSDHC2	Fast Boot: 0 - Regular 1 - Fast Boot

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**SDRAM 32MB**

**Pin Connections:**

- SEMC\_A[12:0]** to **SEMC\_A0** through **SEMC\_A10**
- SEMC\_D[7:0]** to **SEMC\_D0** through **SEMC\_D7**
- SEMC\_D[15:8]** to **SEMC\_D8** through **SEMC\_D15**
- SEMC\_A0** to **H7**
- SEMC\_A1** to **H8**
- SEMC\_A2** to **J8**
- SEMC\_A3** to **J7**
- SEMC\_A4** to **J2**
- SEMC\_A5** to **J3**
- SEMC\_A6** to **H3**
- SEMC\_A7** to **H2**
- SEMC\_A8** to **H1**
- SEMC\_A9** to **G8**
- SEMC\_A10** to **G9**
- SEMC\_A11** to **G2**
- SEMC\_A12** to **G1**
- SEMC\_BA0** to **SDRAM Bank Sel 0**
- SEMC\_BA1** to **SDRAM Bank Sel 1**
- SEMC\_RA** to **SDRAM Row Addr. Strobe**
- SEMC\_CA** to **SDRAM Col. Addr. Strobe**
- SEMC\_WE** to **SDRAM Write En**
- SEMC\_CS** to **SDRAM Chip Sel**
- SEMC\_DM** to **Data Mask**
- SEMC\_CLK** to **SDRAM CLK**
- SEMC\_OK** to **SDRAM CLK EN**
- SEMC\_D0** to **D00**
- SEMC\_D1** to **D01**
- SEMC\_D2** to **D02**
- SEMC\_D3** to **D03**
- SEMC\_D4** to **D04**
- SEMC\_D5** to **D05**
- SEMC\_D6** to **D06**
- SEMC\_D7** to **D07**
- SEMC\_D8** to **D08**
- SEMC\_D9** to **D09**
- SEMC\_D10** to **D10**
- SEMC\_D11** to **D11**
- SEMC\_D12** to **D12**
- SEMC\_D13** to **D13**
- SEMC\_D14** to **D14**
- SEMC\_D15** to **D15**

**Layout Note:**  
Place R74 Close To MCU.

**Component Values:**

- L4**: 120 Ohm
- C86**: 22uF
- C87**: 4.7uF
- C88**: 0.1uF
- C89**: 0.1uF
- C90**: 0.1uF
- C91**: 0.1uF
- C92**: 0.1uF
- C93**: 0.1uF
- C94**: 0.1uF

**Power Supply:** DCDC\_3V3

**SDRAM 3V3**

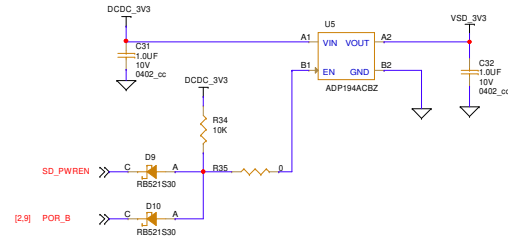
**MAX 150 mA @ 3.3V**

**IS42S16160J-6BLI**  
v0ga04\_bld

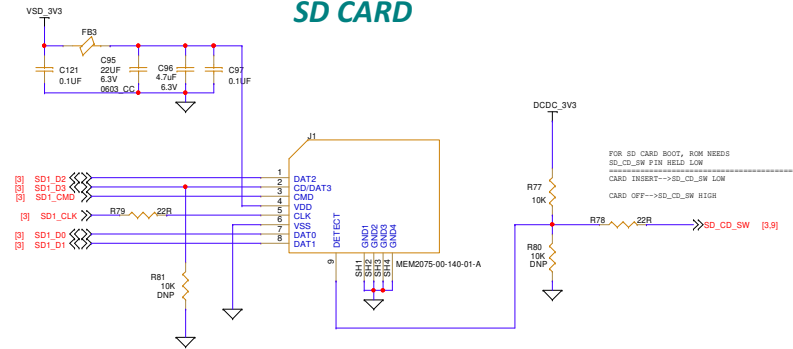
Title RAM			
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# SD CARD

## SD CARD POWER SWITCH



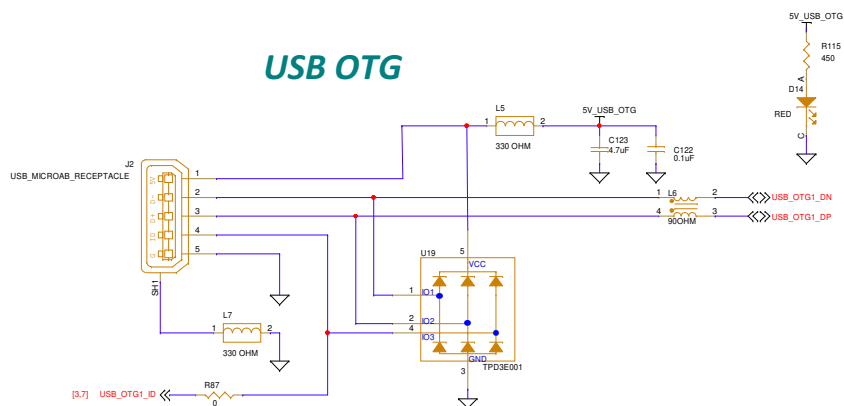
## SD CARD



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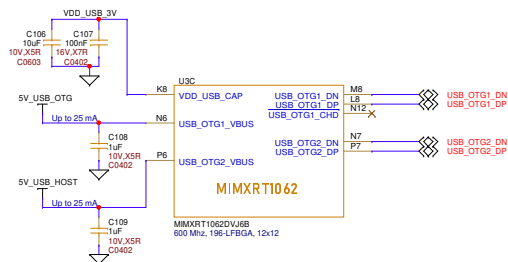
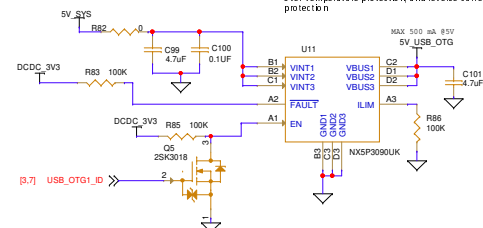
## USB

## USB OTG



## USB POWER

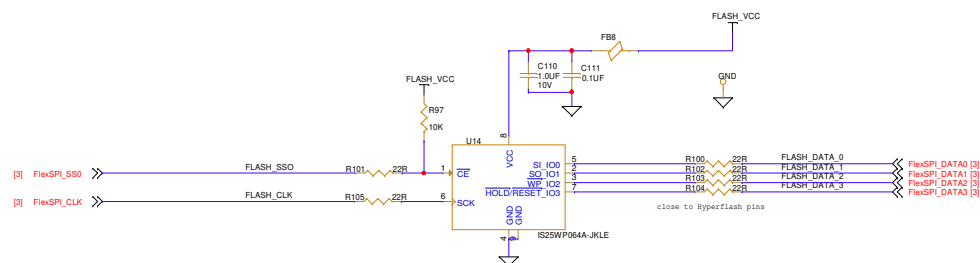
current-limited powerswitch for USB  
Powered Device application.  
Features include: undervoltage lockout,  
over-temperature protection and reverse current  
protection



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USB			
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### 1V8 QSPI Flash



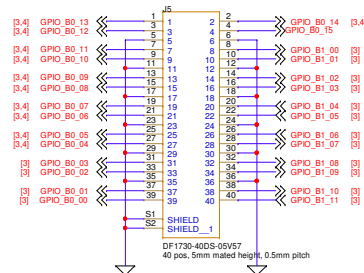
Title FLASH			
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# CONNECTORS

## LCD\_Interface



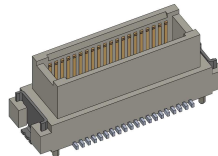
HIROSE RECEPTACLE  
DF17(3.0)-40DS-0.5V(57)



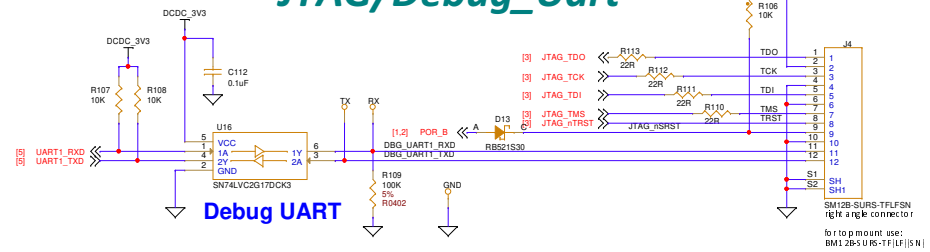
## Mating Connectors:

HIROSE DF17(2.0)-40DP-0.5V(57)  
Digkey PN: H11130TRND  
Board -> Board Stacking Height == 5mm

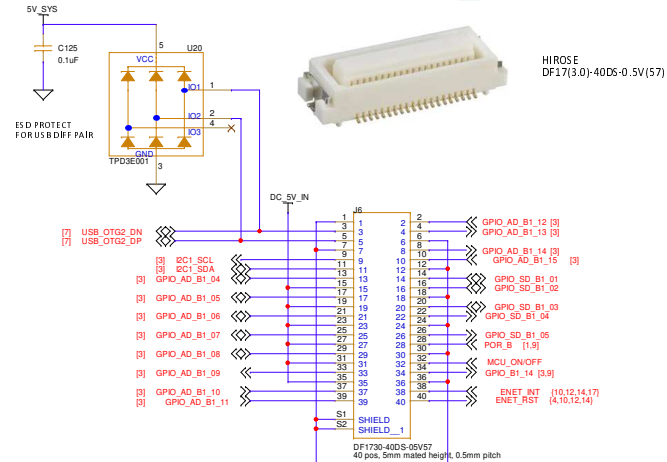
HIROSE DF17(4.0)-40DP-0.5V(57)  
Digkey PN: H11144TRND  
Board -> Board Stacking Height == 7mm



## JTAG/Debug\_Uart



## USB/CSI/ENET\_Interface



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# ALT PINS

GPIO\_EMC[00:07]

Signal	Default	ALT0	ALT1	ALT2	ALT3	ALT4
SEMC_D0	ALT5	SEMC_D0	PWM4_0_A	SPI2_SCLK	XBAR_D2	FLEXIO_00
SEMC_D1	ALT5	SEMC_D1	PWM4_0_B	SPI2_CS0	XBAR_D3	FLEXIO_01
SEMC_D2	ALT5	SEMC_D2	PWM4_1_A	SPI2_SDO	XBAR_D4	FLEXIO_02
SEMC_D3	ALT5	SEMC_D3	PWM4_1_B	SPI2_SDI	XBAR_D5	FLEXIO_03
SEMC_D4	ALT5	SEMC_D4	PWM4_2_A	SAI2_TX_DATA	XBAR_D6	FLEXIO_04
SEMC_D5	ALT5	SEMC_D5	PWM4_2_B	SAI2_TX_SYNC	XBAR_D7	FLEXIO_05
SEMC_D6	ALT5	SEMC_D6	PWM2_0_A	SAI2_TX_BCLK	XBAR_D8	FLEXIO_06
SEMC_D7	ALT5	SEMC_D7	PWM2_0_B	SAI2_MCLK	XBAR_D9	FLEXIO_07

GPIO\_EMC[30:37]

Signal	Default	ALT0	ALT1	ALT2	ALT3	ALT4
SEMC_D8	ALT5	SEMC_D08	PWM3_B0	UART6_CTS_B	SPI1_CS0	CSI_DATA23
SEMC_D9	ALT5	SEMC_D09	PWM3_A1	UART7_TXD	SPI1_CS1	CSI_DATA22
SEMC_D10	ALT5	SEMC_D10	PWM3_B1	UART7_RXD	PMIC_RDY	CSI_DATA21
SEMC_D11	ALT5	SEMC_D11	PWM3_A2	SDHCI_RST_B	SAI3_RX_DAT	CSI_DATA20
SEMC_D12	ALT5	SEMC_D12	PWM3_B2	SDHCI_VSEL	SAI3_RX_SYNC	CSI_DATA19
SEMC_D13	ALT5	SEMC_D13	XBAR1_18	GPT1_CMP1	SAI3_RX_BCLK	CSI_DATA18
SEMC_D14	ALT5	SEMC_D14	XBAR1_22	GPT1_CMP2	SAI3_TX_DATA	CSI_DATA17
SEMC_D15	ALT5	SEMC_D15	XBAR1_23	GPT1_CMP3	SAI3_MCLK	CSI_DATA16

# LAYOUT GUIDELINES

## Routing guidelines for MIPI & LVDS

- 1) All differential routes are required to have the same length between the positive (true) and the negative (complimentary) routes. Spacing between the positive (true) and the negative (complimentary) shall be 2 times trace width.
- 2) Target differential impedance shall be 100 Ohms
- 3) Trace length matching to be within 1.0 mm (40 mil) across the entire bus.
- 4) Use small humps for skew corrections
- 5) Place signal vias close together and remove copper in between vias. Traces to be fully shielded with GND stitching terminating at both trace end points
- 6) Board trace impedance results must be within  $\pm 10$  percent of target and Power plane impedance to be within  $\pm 10$  percent of target at operating frequency

## MIPI & LVDS Simulation Requirement

- 1) MIPI Differential Mode insertion Loss shall be  $> -1.6\text{dB}$  at 750 MHz
- 2) MIPI Differential Mode Return Loss shall be  $< -15\text{dB}$  at 750 MHz
- 3) MIPI Common Mode Return Loss shall be  $< -15\text{dB}$  at 750 MHz
- 4) LVDS differential mode return loss shall be  $< -16.5\text{dB}$  at 600 MHz
- 5) LVDS common mode return loss shall be  $< -16.5\text{dB}$  at 600 MHz
- 6) LVDS insertion loss shall be  $> -1.7\text{dB}$  at 600 MHz
- 7) LVDS Cross coupling shall be  $< -22\text{dB}$  for victim IO at 600MHz
- 8) Power plane impedance to be within  $\pm 10$  percent of target at operating frequency

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LAYOUT			
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