

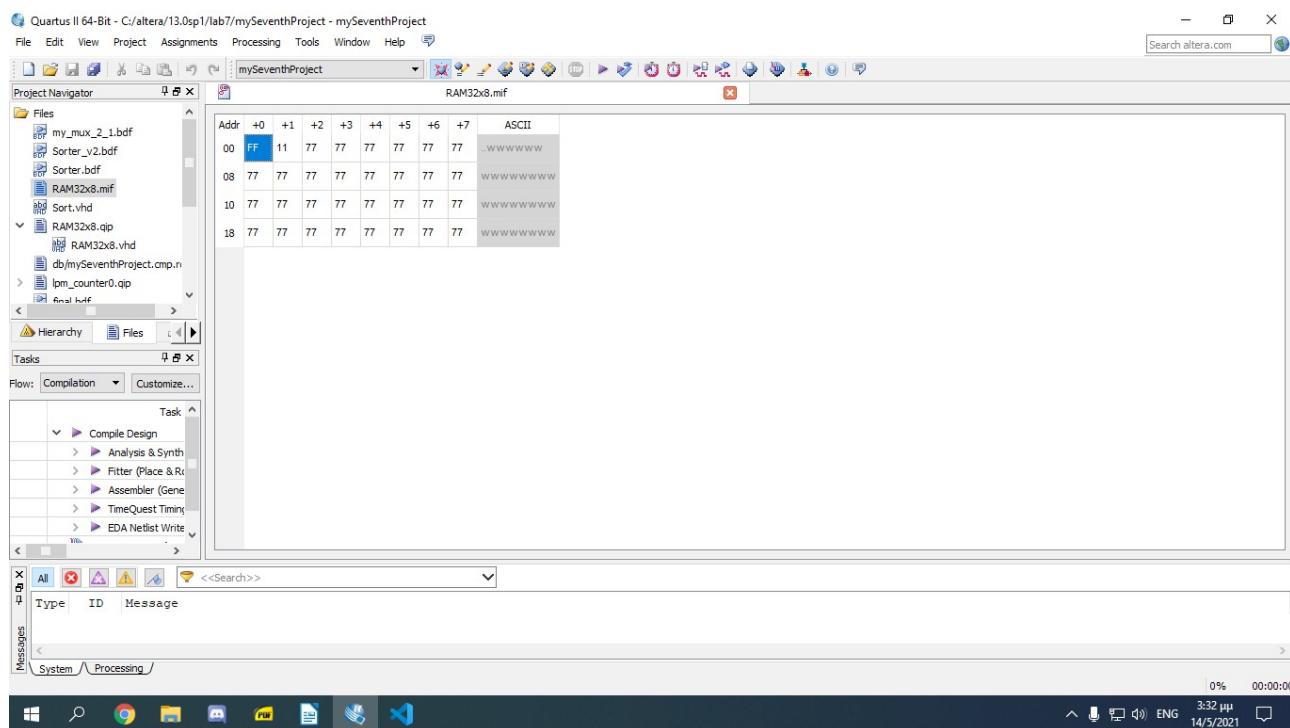
ΨΗΦΙΑΚΗ ΣΧΕΔΙΑΣΗ 2

7η Εργαστηριακή Άσκηση

Γκότσης Βασίλης 3206
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Ενσωμάτωση Μνήμης

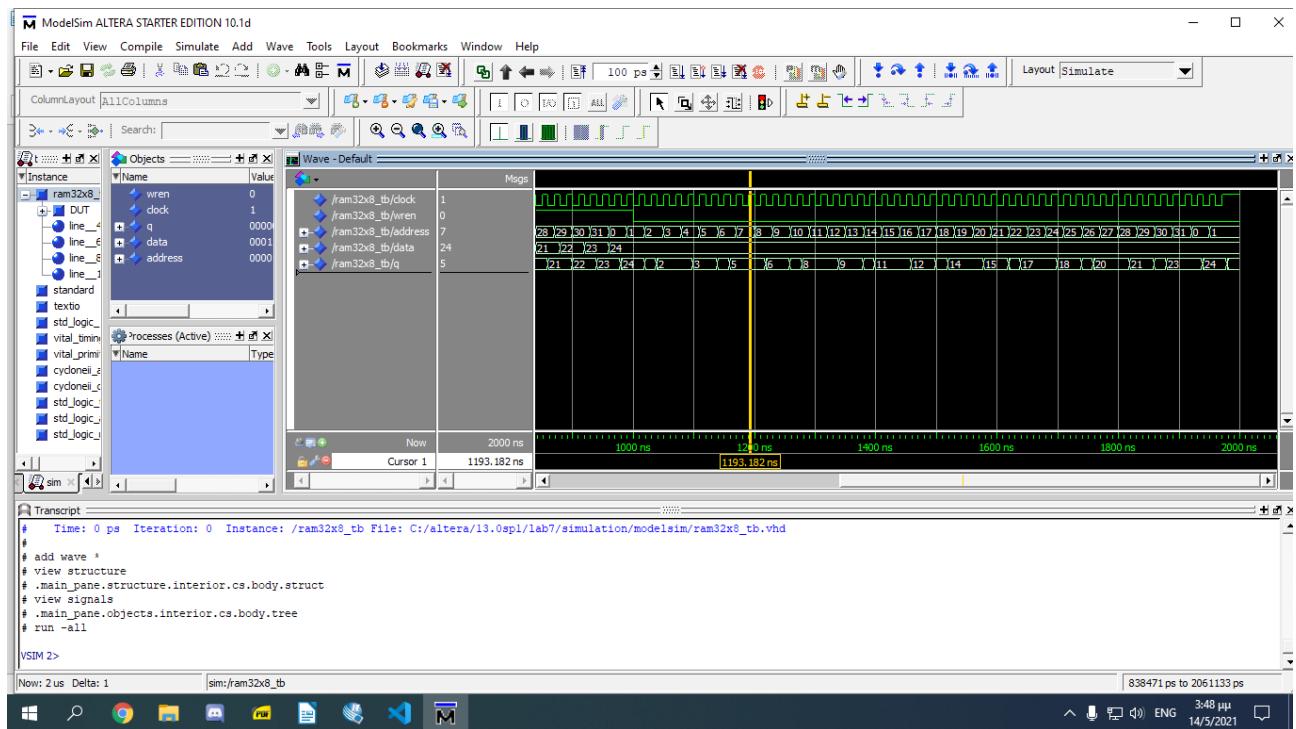
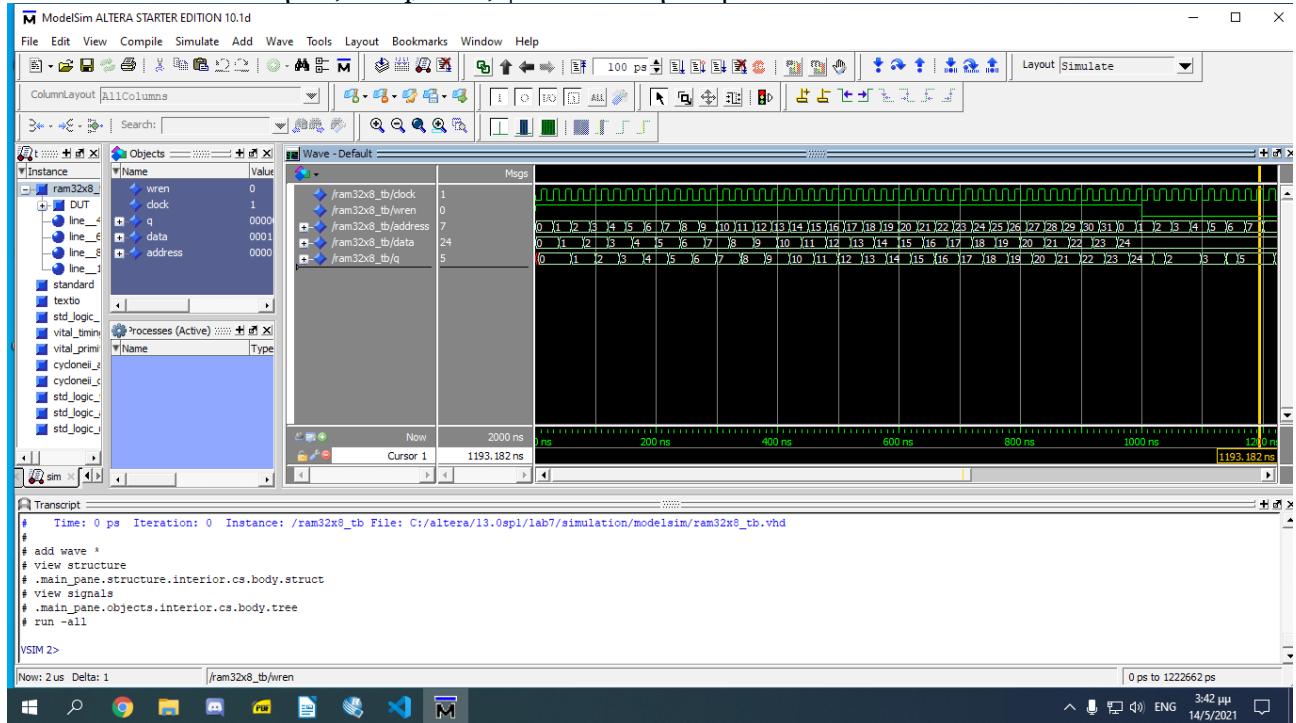
Ακολουθώντας τις οδηγίες της εκφώνησης δημιουργήσαμε ένα αρχείο αρχικοποίησης της μνήμης με όνομα RAM32x8.mif όπως φαίνεται στην παρακάτω εικόνα και συμπληρώσαμε τις θέσεις μνήμης με τα αντίστοιχα στοιχεία που δίνονται στην εκφώνηση:



The screenshot shows the RAM32x8.mif file opened in Visual Studio Code. The code is a memory initialization file (MIF) for Altera Quartus II. It includes a copyright notice, specifies WIDTH=8 and DEPTH=32, defines ADDRESS and DATA RADIX as HEX, and contains a CONTENT BEGIN section with memory data starting at address 00. The file is saved in the 'lab7' folder under 'altera > 13.0sp1'. The status bar at the bottom indicates the file has 28 lines, is in UTF-8 encoding, and was last modified on 14/5/2021 at 3:32 μμ.

```
File Edit Selection View Go Run Terminal Help • RAM32x8.mif - Visual Studio Code
C: > altera > 13.0sp1 > lab7 > RAM32x8.mif
1 -- Copyright (C) 1991-2013 Altera Corporation
2 -- Your use of Altera Corporation's design tools, logic functions
3 -- and other software and tools, and its AMPP partner logic
4 -- functions, and any output files from any of the foregoing
5 -- (including device programming or simulation files), and any
6 -- associated documentation or information are expressly subject
7 -- to the terms and conditions of the Altera Program License
8 -- Subscription Agreement, Altera MegaCore Function License
9 -- Agreement, or other applicable license agreement, including,
10 -- without limitation, that your use is for the sole purpose of
11 -- programming logic devices manufactured by Altera and sold by
12 -- Altera or its authorized distributors. Please refer to the
13 -- applicable agreement for further details.
14
15 -- Quartus II generated Memory Initialization File (.mif)
16
17 WIDTH=8;
18 DEPTH=32;
19
20 ADDRESS_RADIX=HEX;
21 DATA_RADIX=HEX;
22
23 CONTENT BEGIN
24   00 : FF;
25   01 : 11;
26   [02..1F] : 77;
27 END;
28
```

Στο επόμενο βήμα δημιουργήσαμε το test_bench της μνήμης με όνομα ram32x8_tb.vhd με το οποίο τεστάραμε την λειτουργία της μνήμης σε εγγραφή και ανάγνωση δεδομένων.
Παρατηρούμε ότι για wren=1 η μνήμη αποθηκεύει στοιχεία από την είσοδο data στην διεύθυνση address ενώ για wren=0 η μνήμη διαβάζει τα αποθηκευμένα στοιχεία από την διεύθυνση address και τα κατευθύνει στην έξοδο q, όπως φαίνεται στην παρακάτω εικόνα:



To clk και το wren είναι σε μορφή binary και τα υπόλοιπα(address, data, q) είναι σε μορφή unsigned για ευκολία.

Τέλος, την μνήμη την πακετάραμε σε κουτάκι.

Σχεδίαση με VHDL

Αρχικά σχεδιάσαμε το κύκλωμα ταξινόμησης που υλοποιεί τον αλγόριθμο bubble short όπως ακριβώς δίνεται στην εκφώνηση σε ένα αρχείο Sort.vhd το οποίο και το πακετάραμε σε κουτάκι. Το κύκλωμα φαίνεται στις παρακάτω εικόνες:

The screenshot shows the Quartus II IDE interface with the project 'mySeventhProject' open. The main window displays the VHDL source code for 'Sort.vhd'. The code defines an entity 'Sort' with a port section and an architecture 'RTL' of 'Sort'. The architecture contains a state transition table with columns for current state, event, and next state. Below the code is a 'Compilation Report' showing a successful compilation with 0 errors and 16 warnings. The 'Messages' panel at the bottom shows a single message indicating a full compilation was successful. The system tray at the bottom right shows the date as 14/5/2021.

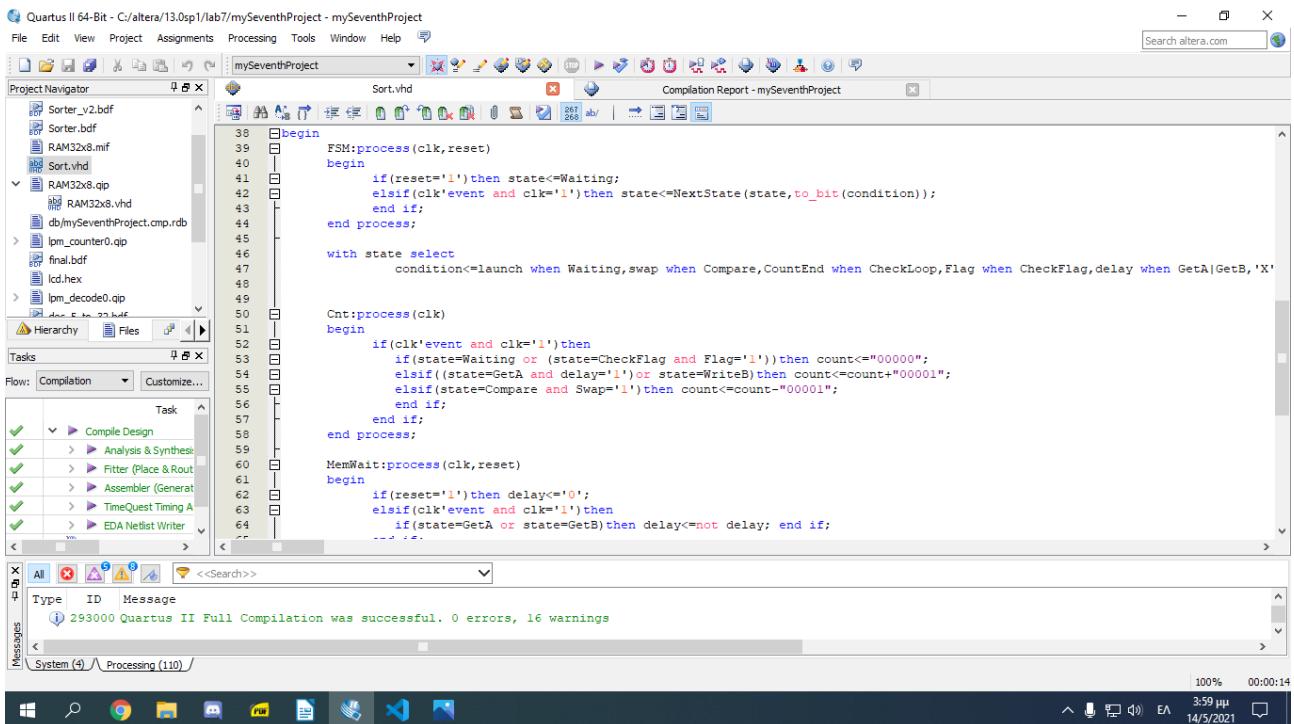
```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

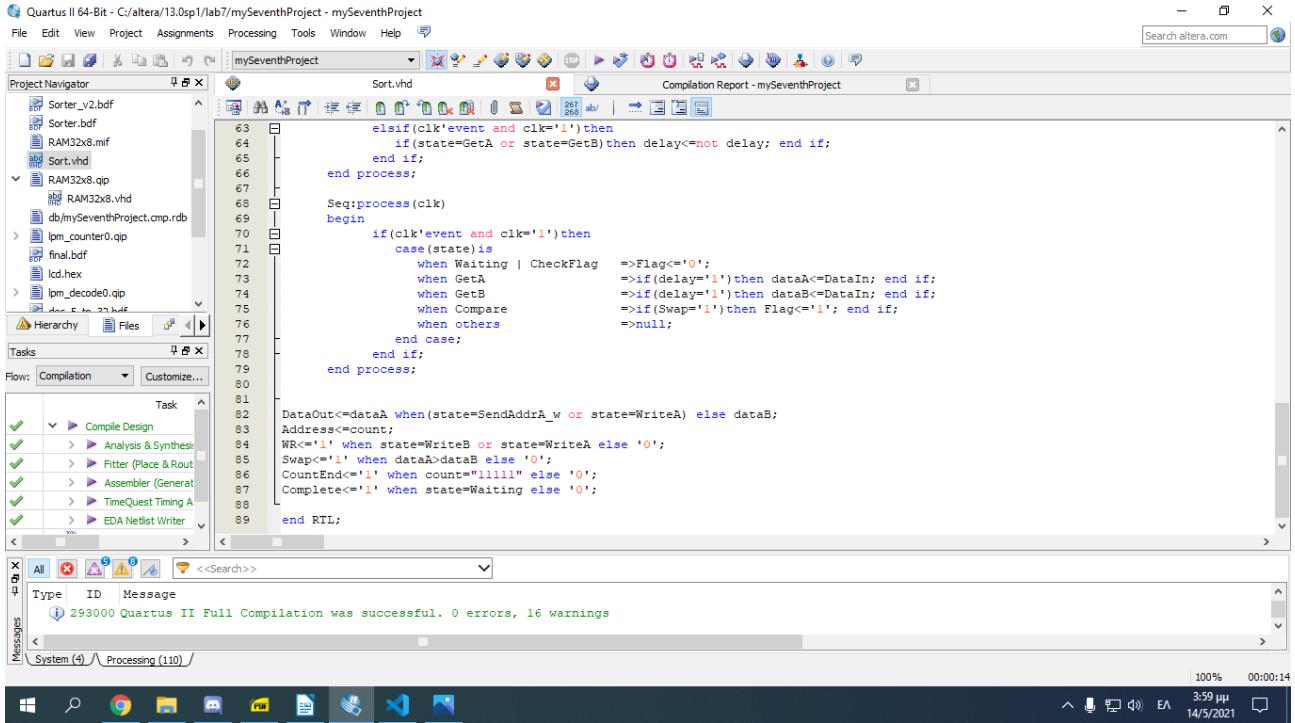
entity Sort is
port(
    clk,launch,reset: in std_logic;
    DataIn : in std_logic_vector(7 downto 0);
    Address : out std_logic_vector(4 downto 0);
    DataOut : out std_logic_vector(7 downto 0);
    Complete,WR : out std_logic);
end Sort;

architecture RTL of Sort is
begin
    type state_type is (Waiting, SendAddrA_r,GetA,SendAddrB_r,GetB,Compare,SendAddrA_w,WriteA,SendAddrB_w,WriteB,CheckLoop,CheckFlag);
    type StateArray is array (state_type,bit) of state_type;
    constant NextState: StateArray:=(
        Waiting      => ('0'=>Waiting,'1'=>SendAddrA_r),
        SendAddrA_r  => ('others'=>GetA),
        GetA         => ('0'=>GetA,'1'=>SendAddrB_r),
        SendAddrB_r  => ('others'=>GetB),
        GetB         => ('0'=>GetB,'1'=>Compare),
        Compare      => ('0'=>CheckLoop,'1'=>SendAddrB_w),
        SendAddrB_w  => ('others'=>WriteB),
        WriteB       => ('others'=>SendAddrA_w),
        SendAddrA_w  => ('others'=>WriteA),
        ...           => ...
    );
end;
signal state: state_type;
signal dataA,dataB: std_logic_vector(7 downto 0);
signal count: std_logic_vector(4 downto 0);
signal Flag,Swap,CountEnd,condition,delay: std_logic;
begin
    FSM:process(clk,reset)
    begin
        if(reset='1')then state<=Waiting;
        elsif(clk'event and clk='1')then state<=NextState(state,to_bit(condition));
        end if;
    end process;
    with state select
        ...
```

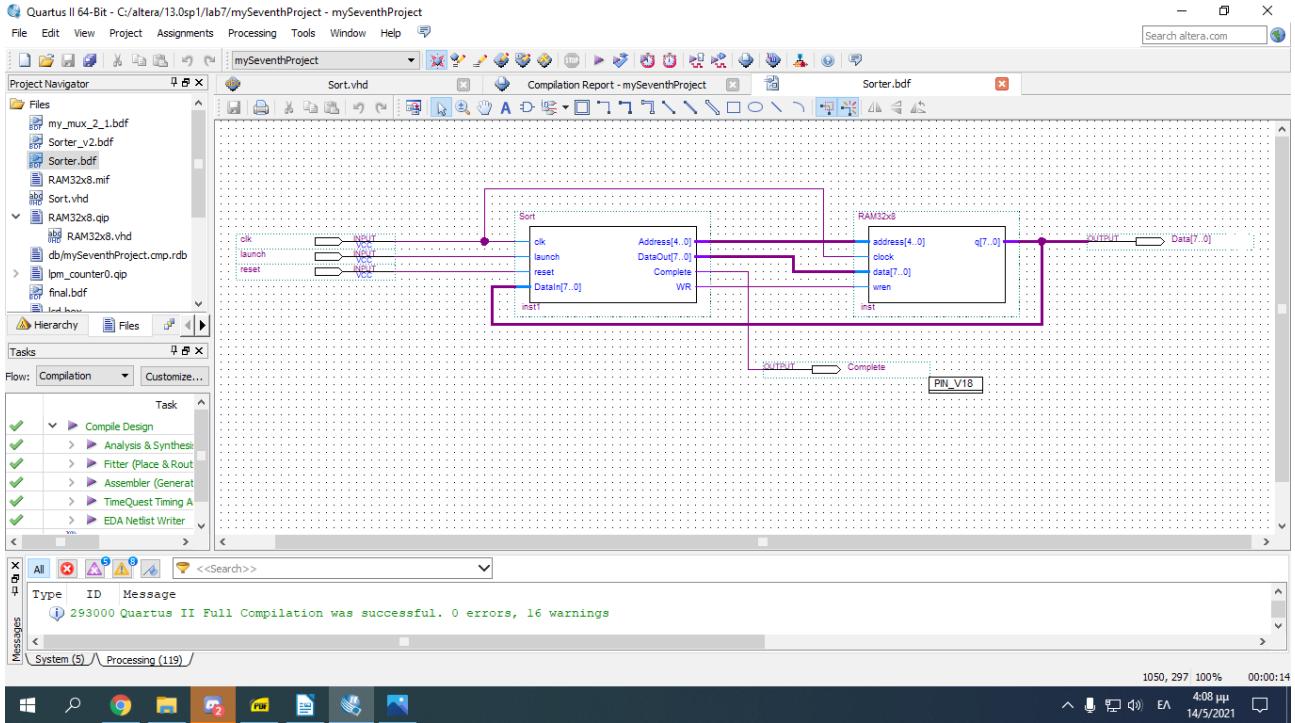
This screenshot continues the display of the 'Sort.vhd' source code from the previous one. It shows the lower portion of the state transition table and the beginning of the 'with state select' block. The rest of the code is identical to the first screenshot. The compilation report and message panel are also present, confirming a successful compilation.

```
        ...           => ...
    );
begin
    FSM:process(clk,reset)
    begin
        if(reset='1')then state<=Waiting;
        elsif(clk'event and clk='1')then state<=NextState(state,to_bit(condition));
        end if;
    end process;
    with state select
        ...
```

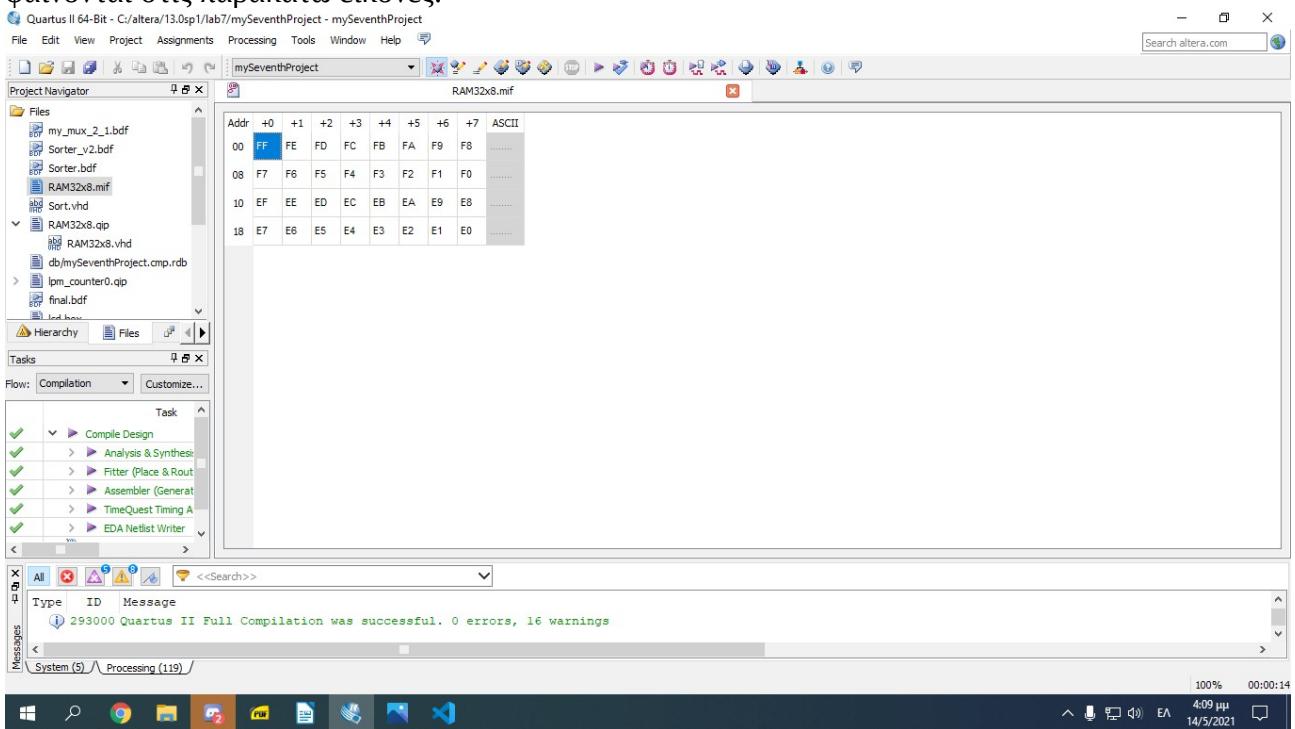




Στην συνέχεια δημιουργήσαμε ένα Sorter.bdf στο οποίο τοποθετήσαμε τα blocks που δημιουργήσαμε προηγουμένως όπως αναγράφεται στην εκφώνηση.
Το κύκλωμα φαίνεται στην παρακάτω εικόνα:



Τέλος, αρχικοποιήσαμε τις 32 θέσεις της μνήμης με τα αντίστοιχα στοιχεία όπως ακριβώς φαίνονται στις παρακάτω εικόνες:



The screenshot shows a hex dump of the `RAM32x8.mif` file in Visual Studio Code. The file contains memory contents from address 24 to 55, with values ranging from FF to E0. The interface includes a sidebar with icons for file operations, a status bar at the bottom, and a taskbar at the bottom.

```

C:\> altera > 13.0sp1 > lab7 > RAM32x8.mif
24 00 : FF;
25 01 : FE;
26 02 : FD;
27 03 : FC;
28 04 : FB;
29 05 : FA;
30 06 : F9;
31 07 : F8;
32 08 : F7;
33 09 : F6;
34 0A : F5;
35 0B : F4;
36 0C : F3;
37 0D : F2;
38 0E : F1;
39 0F : F0;
40 10 : EF;
41 11 : EE;
42 12 : ED;
43 13 : EC;
44 14 : EB;
45 15 : EA;
46 16 : E9;
47 17 : E8;
48 18 : E7;
49 19 : E6;
50 1A : E5;
51 1B : E4;
52 1C : E3;
53 1D : E2;
54 1E : E1;
55 1F : E0;

```

Εξομοίωση του κυκλώματος

Αρχικά μετατρέψαμε το αρχείο Sorter.bdf σε Sorter.vhd το οποίο και φαίνεται στις παρακάτω εικόνες:

The screenshot shows the Quartus II interface with the project `mySeventhProject`. It displays the `Sorter.vhd` source code, which contains VHDL logic for a sorting algorithm. The `Project Navigator` shows files like `Sorter.vhd`, `RAM32x8.mif`, and `Sort.vhd`. The `Tasks` pane shows a successful compilation process with 0 errors and 16 warnings. The `Messages` pane indicates a successful compilation. The interface includes a toolbar, a status bar at the bottom, and a taskbar at the bottom.

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity Sort is
port(
    clk,launch,reset: in std_logic;
    DataIn : in std_logic_vector(7 downto 0);
    Address : out std_logic_vector(4 downto 0);
    DataOut : out std_logic_vector(7 downto 0);
    Complete,WR : out std_logic);
end Sort;
architecture RTL of Sort is
type state_type is (Waiting, SendAddrA_r,GetA,SendAddrB_r,Compare,SendAddrA_w,WriteA,SendAddrB_w,WriteB,CheckLoop,CheckF1);
type StateArray is array (state_type,bit) of state_type;
constant NextState: StateArray:=(
    Waiting =>('0'=>Waiting,'1'=>SendAddrA_r),
    SendAddrA_r =>(others=>GetA),
    GetA =>('0'=>GetA,'1'=>SendAddrB_r),
    SendAddrB_r =>(others=>GetB),
    GetB =>('0'=>GetB,'1'=>Compare),
    Compare =>('0'=>CheckLoop,'1'=>SendAddrB_w),
    SendAddrB_w =>(others=>WriteB),
    WriteB =>(others=>SendAddrA_w),
    SendAddrA_w =>(others=>WriteA),
    ...
)

```

Quartus II 64-Bit - C:/altera/13.0sp1/lab7/mySeventhProject - mySeventhProject

File Edit View Project Assignments Processing Tools Window Help

Project Navigator RAM32x8.mif Sorter.bdf Sorter.vhd Sort.vhd Compilation Report - mySeventhProject

Files

- Sorter.vhd
- my_mux_2_1.bdf
- Sorter_v2.bdf
- RAM32x8.mif
- Sort.vhd
- RAM32x8.qip
- db/mySeventhProject.cmp.rdb
- jpm_counter0.qip
- final.bdf
- lcd.hex
- lpm_doubl0.aif

Hierarchy Files

Tasks

Flow: Compilation Customize...

```

20      SendAddrA_r => (others=>GetA),
21      GetA => ('0'=>GetA, '1'=>SendAddrB_r),
22      SendAddrB_r => (others=>GetB),
23      GetB => ('0'=>GetB, '1'=>Compare),
24      Compare => ('0'=>CheckLoop, '1'=>SendAddrB_w),
25      SendAddrB_w => (others=>WriteB),
26      WriteB => (others=>SendAddrA_w),
27      SendAddrA_w => (others=>WriteA),
28      WriteA => (others=>CheckLoop),
29      CheckLoop => ('0'=>SendAddrA_r, '1'=>CheckFlag),
30      CheckFlag => ('0'=>Waiting, '1'=>SendAddrA_r);

31
32
33      signal state:          state_type;
34      signal dataA,dataB:    std_logic_vector(7 downto 0);
35      signal count:          std_logic_vector(4 downto 0);
36      signal Flag,Swap,CountEnd,condition,delay: std_logic;
37
38 begin
39   FSM:process(clk,reset)
40   begin
41     if(reset='1') then state<=Waiting;
42     elsif(clk'event and clk='1') then state<=NextState(state,to_bit(condition));
43     end if;
44   end process;
45
46   with state select
47     condition<=launch when Waiting,swap when Compare,CountEnd when CheckLoop,Flag when CheckFlag,delay when GetA|GetB,X';
48
49
50   Cnt:process(clk)
51   begin
52     if(clk'event and clk='1')then
53       if(state=Waiting or (state=CheckFlag and Flag='1'))then count<="00000";
54       elsif(state=GetA and delay='1')or state=WriteB)then count<=count+"00001";
55       elsif(state=Compare and Swap='1')then count<=count-"00001";
56       end if;
57     end if;
58   end process;
59
60   MemWait:process(clk,reset)
61   begin
62     if(reset='1') then delay<='0';
63     elsif(clk'event and clk='1')then
64       if(state=GetA or state=GetB)then delay<=not delay; end if;
65     end if;
66   end process;

```

Messages

Type	ID	Message
293000 Quartus II Full Compilation was successful. 0 errors, 16 warnings		

System (5) / Processing (119) /

100% 00:00:14 4:22 μs 14/5/2021

Quartus II 64-Bit - C:/altera/13.0sp1/lab7/mySeventhProject - mySeventhProject

File Edit View Project Assignments Processing Tools Window Help

Project Navigator RAM32x8.mif Sorter.bdf Sorter.vhd Sort.vhd Compilation Report - mySeventhProject

Files

- Sorter.vhd
- my_mux_2_1.bdf
- Sorter_v2.bdf
- RAM32x8.mif
- Sort.vhd
- RAM32x8.qip
- db/mySeventhProject.cmp.rdb
- jpm_counter0.qip
- final.bdf
- lcd.hex
- lpm_doubl0.aif

Hierarchy Files

Tasks

Flow: Compilation Customize...

```

39   FSM:process(clk,reset)
40   begin
41     if(reset='1') then state<=Waiting;
42     elsif(clk'event and clk='1') then state<=NextState(state,to_bit(condition));
43     end if;
44   end process;
45
46   with state select
47     condition<=launch when Waiting,swap when Compare,CountEnd when CheckLoop,Flag when CheckFlag,delay when GetA|GetB,X';
48
49
50   Cnt:process(clk)
51   begin
52     if(clk'event and clk='1')then
53       if(state=Waiting or (state=CheckFlag and Flag='1'))then count<="00000";
54       elsif(state=GetA and delay='1')or state=WriteB)then count<=count+"00001";
55       elsif(state=Compare and Swap='1')then count<=count-"00001";
56       end if;
57     end if;
58   end process;
59
60   MemWait:process(clk,reset)
61   begin
62     if(reset='1') then delay<='0';
63     elsif(clk'event and clk='1')then
64       if(state=GetA or state=GetB)then delay<=not delay; end if;
65     end if;
66   end process;

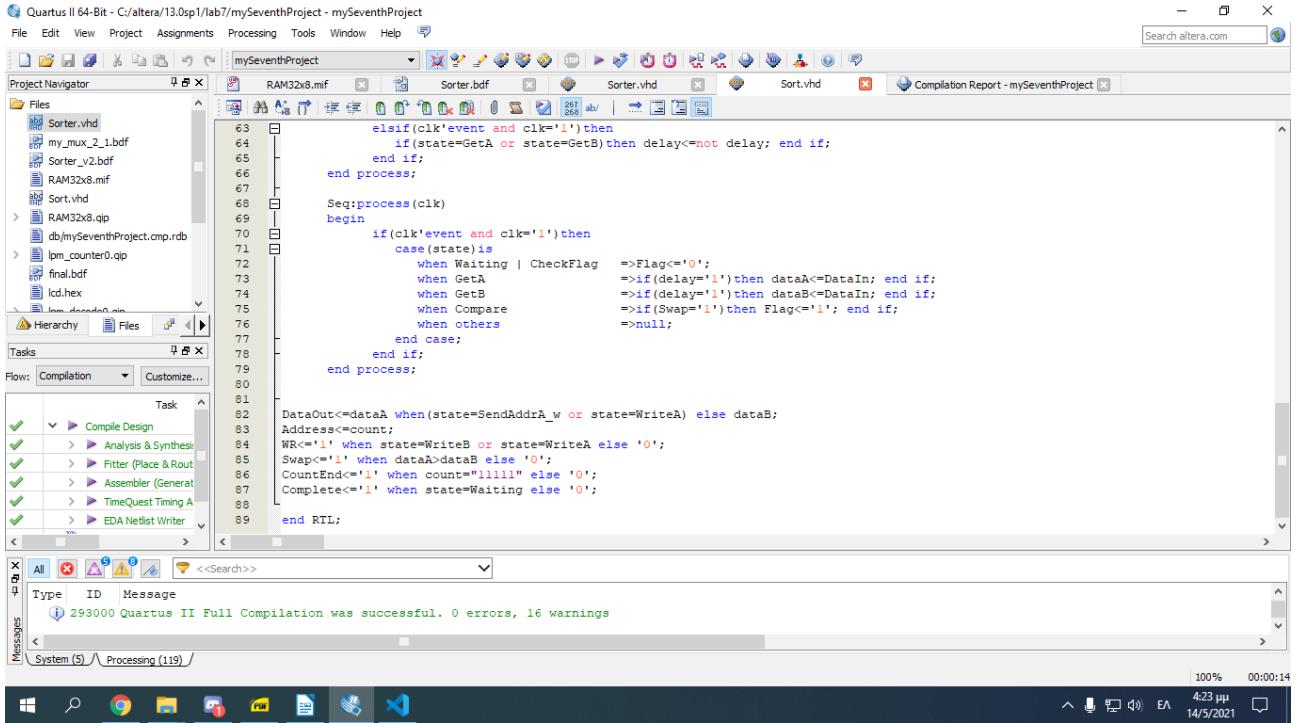
```

Messages

Type	ID	Message
293000 Quartus II Full Compilation was successful. 0 errors, 16 warnings		

System (5) / Processing (119) /

100% 00:00:14 4:22 μs 14/5/2021



Για το παραπόνω κύκλωμα δημιουργήσαμε το test_bench με όνομα Sorter_tb.vhd το οποίο και τροποποιήσαμε κατάλληλα τοποθετώντας την process που δίνεται στην εκφώνηση πριν από την process του ρολογιού, όπως ακριβώς φαίνεται στις παρακάτω εικόνες:

```

LIBRARY cycloneii ;
LIBRARY ieee ;
LIBRARY std ;
USE cycloneii.cycloneii_components.all ;
USE ieee.std_logic_1164.all ;
USE ieee.std_logic_textio.all ;
USE ieee.std_logic_unsigned.all ;
USE std.textio.all ;
ENTITY Sorter_tb IS
END ;
ARCHITECTURE Sorter_tb_arch OF Sorter_tb IS
SIGNAL Complete : STD_LOGIC ;
SIGNAL Data : STD_LOGIC_VECTOR(7 DOWNTO 0) ;
SIGNAL clk : STD_LOGIC ;
SIGNAL reset : STD_LOGIC ;
SIGNAL launch : STD_LOGIC ;
COMPONENT Sorter
PORT (
    Complete : OUT STD_LOGIC ;
    Data : OUT STD_LOGIC_VECTOR(7 DOWNTO 0) ;
    clk : IN STD_LOGIC ;
    reset : IN STD_LOGIC ;
    launch : IN STD_LOGIC );
END COMPONENT ;
BEGIN
DUT : Sorter
PORT MAP (
    Complete => Complete ,
    Data => Data ,
    clk => clk ,
    reset => reset ,
    launch => launch ) ;

```

File Edit Selection View Go Run Terminal Help Sorter_tb.vhd - Visual Studio Code

```
C: > altera > 13.0sp1 > lab7 > simulation > modelsim > Sorter_tb.vhd
```

```
26 BEGIN
27   DUT : Sorter
28   PORT MAP (
29     Complete  => Complete ,
30     Data      => Data ,
31     clk       => clk ,
32     reset    => reset ,
33     launch   => launch );
34
35
36
37 process
38 begin
39   reset<='1';
40   launch<='0';
41   wait for 12 ns;
42   reset<='0';
43   launch<='1';
44   wait for 50 ns;
45   launch<='0';
46   wait;
47 end process;
48
49
50 -- "Clock Pattern" : dutyCycle = 50
51 -- Start Time = 0 ns, End Time = 2 us, Period = 20 ns
52 Process
53 Begin
54   |clk <= '0' ;
55   wait for 10 ns ;
56 -- 10 ns, single loop till start period.
57   for Z in 1 to 1000000000
58   loop
59     |clk <= '1' ;
60     wait for 10 ns ;
61     |clk <= '0' ;
62     wait for 10 ns ;
63     exit when (Complete'last_value = '0' and Complete = '1');
64 -- 1990 ns, repeat pattern in loop.
65   end loop;
66   |clk <= '1' ;
67   wait for 10 ns ;
68 -- dumped values till 2 us
69   wait;
70 End Process;
71
72
73 END;
```

Live Share

Ln 44, Col 24 Tab Size: 4 UTF-8 CRLF VHDL 4:29 μs 14/5/2021

File Edit Selection View Go Run Terminal Help Sorter_tb.vhd - Visual Studio Code

```
C: > altera > 13.0sp1 > lab7 > simulation > modelsim > Sorter_tb.vhd
```

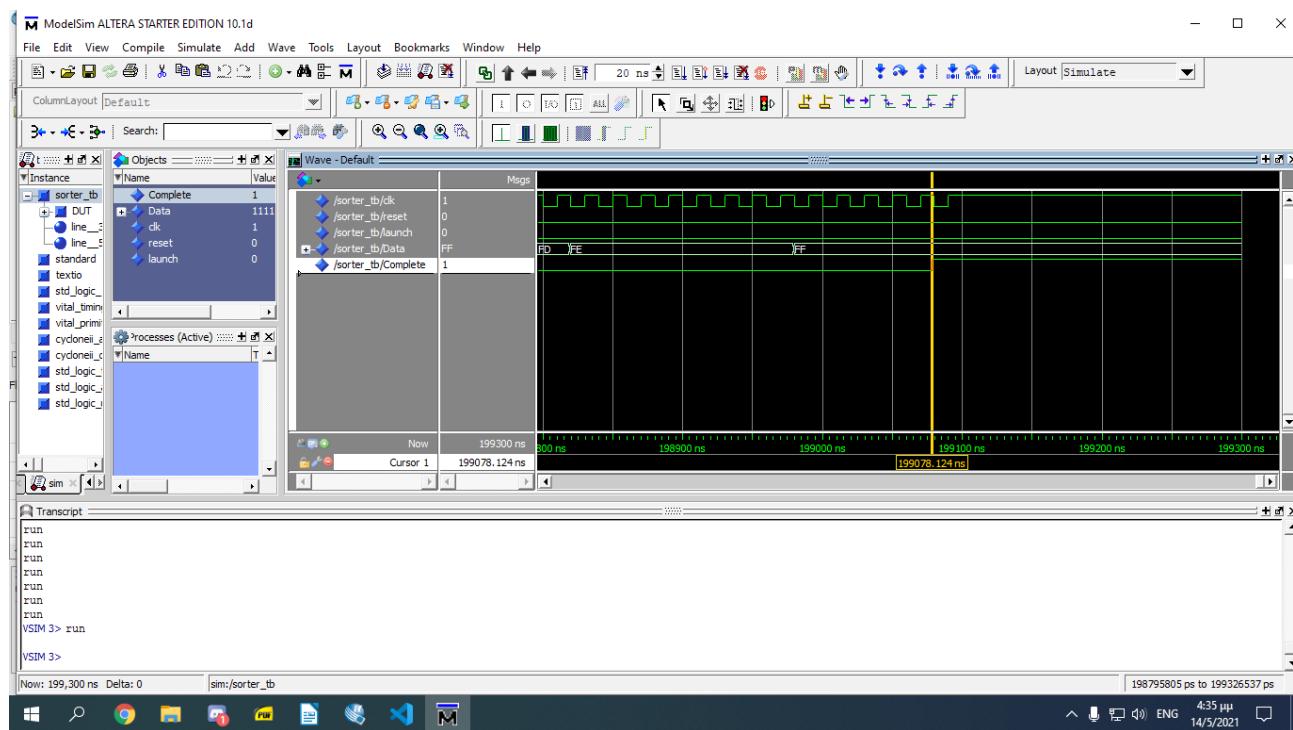
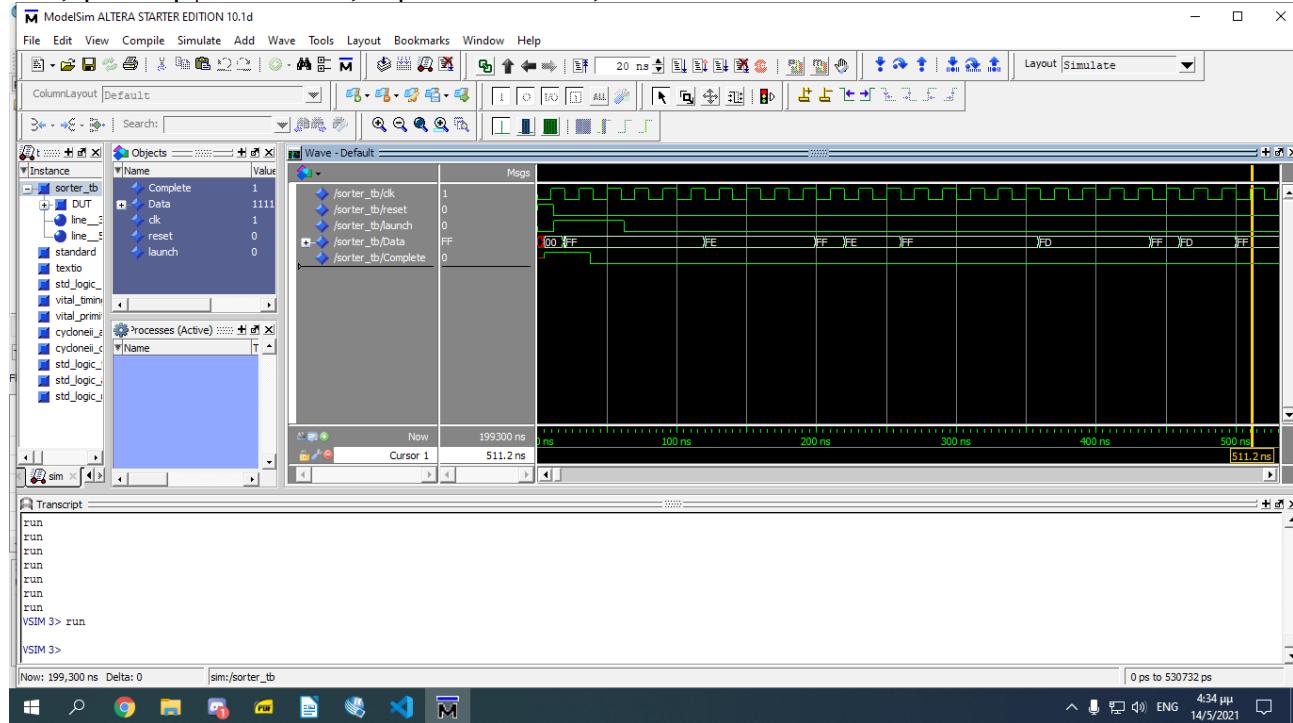
```
46   |wait;
47 end process;
48
49
50 -- "Clock Pattern" : dutyCycle = 50
51 -- Start Time = 0 ns, End Time = 2 us, Period = 20 ns
52 Process
53 Begin
54   |clk <= '0' ;
55   wait for 10 ns ;
56 -- 10 ns, single loop till start period.
57   for Z in 1 to 1000000000
58   loop
59     |clk <= '1' ;
60     wait for 10 ns ;
61     |clk <= '0' ;
62     wait for 10 ns ;
63     exit when (Complete'last_value = '0' and Complete = '1');
64 -- 1990 ns, repeat pattern in loop.
65   end loop;
66   |clk <= '1' ;
67   wait for 10 ns ;
68 -- dumped values till 2 us
69   wait;
70 End Process;
71
72
73 END;
```

Live Share

Ln 44, Col 24 Tab Size: 4 UTF-8 CRLF VHDL 4:29 μs 14/5/2021

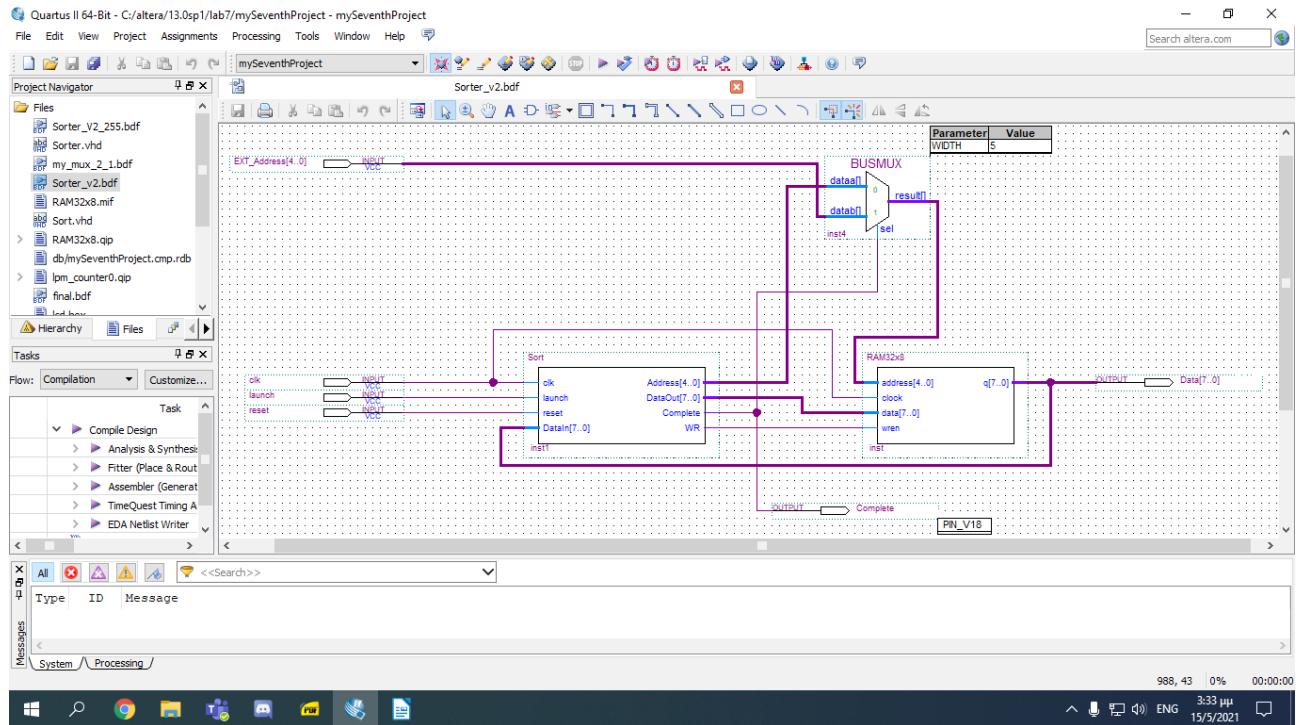
Εκτελώντας gate level simulation παρατηρούμε ότι το κύκλωμα δουλεύει σωστά και ότι ταξινομεί τα περιεχόμενα της μνήμης σε 199078.124ns και σηματοδοτεί το τέλος της διαδικασίας με Complete=1.

Η εξομοίωση φαίνεται στις παρακάτω εικόνες:



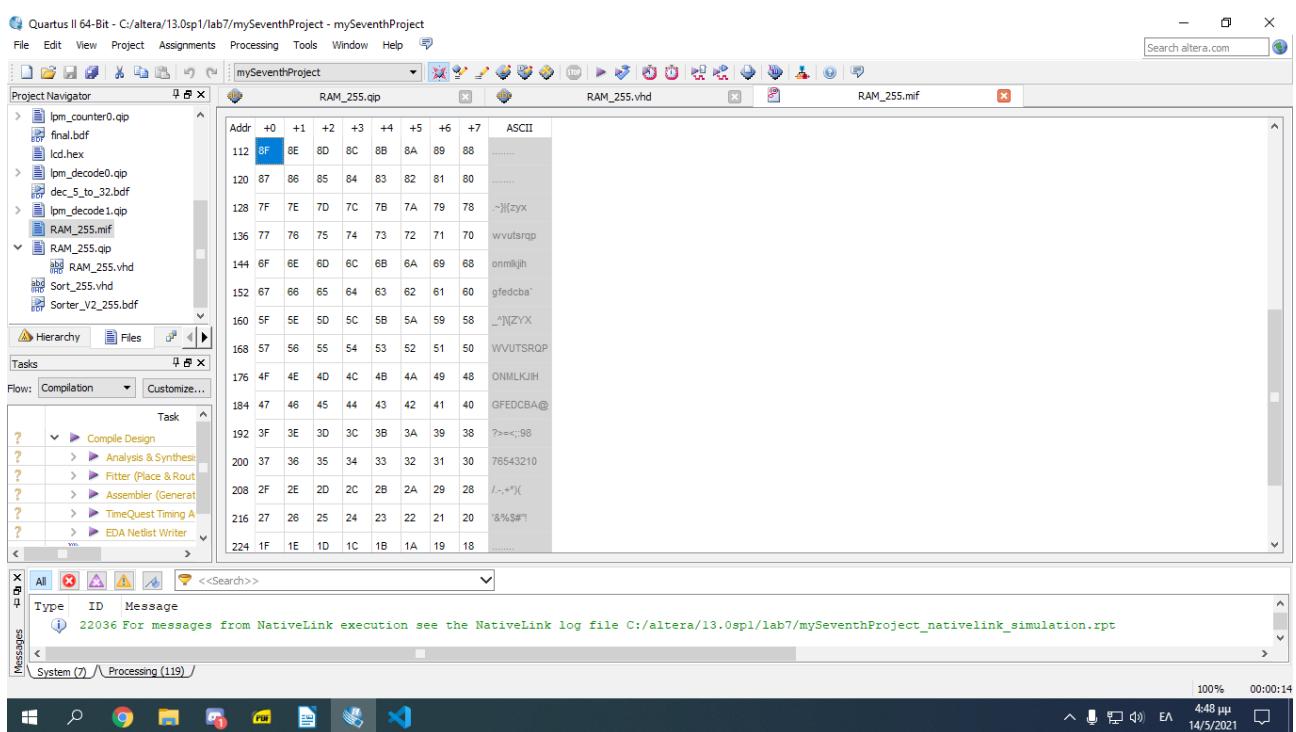
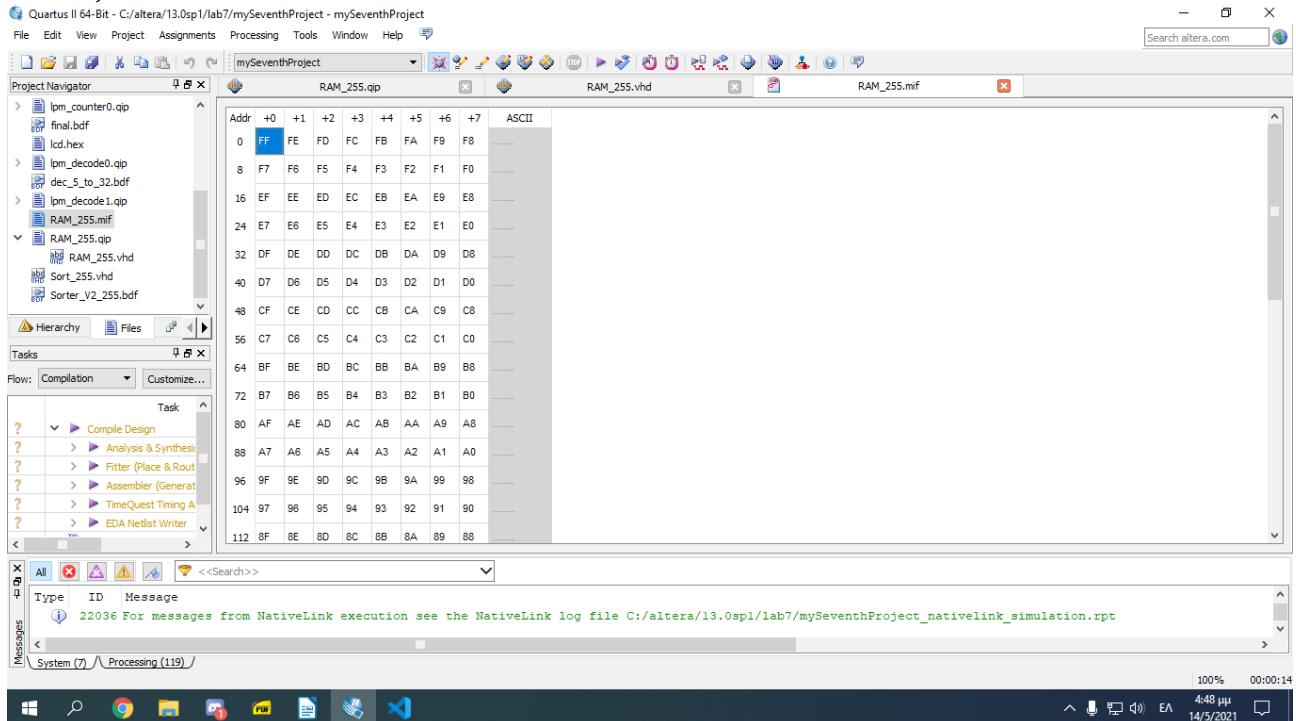
Υλοποίηση και έλεγχος στο board

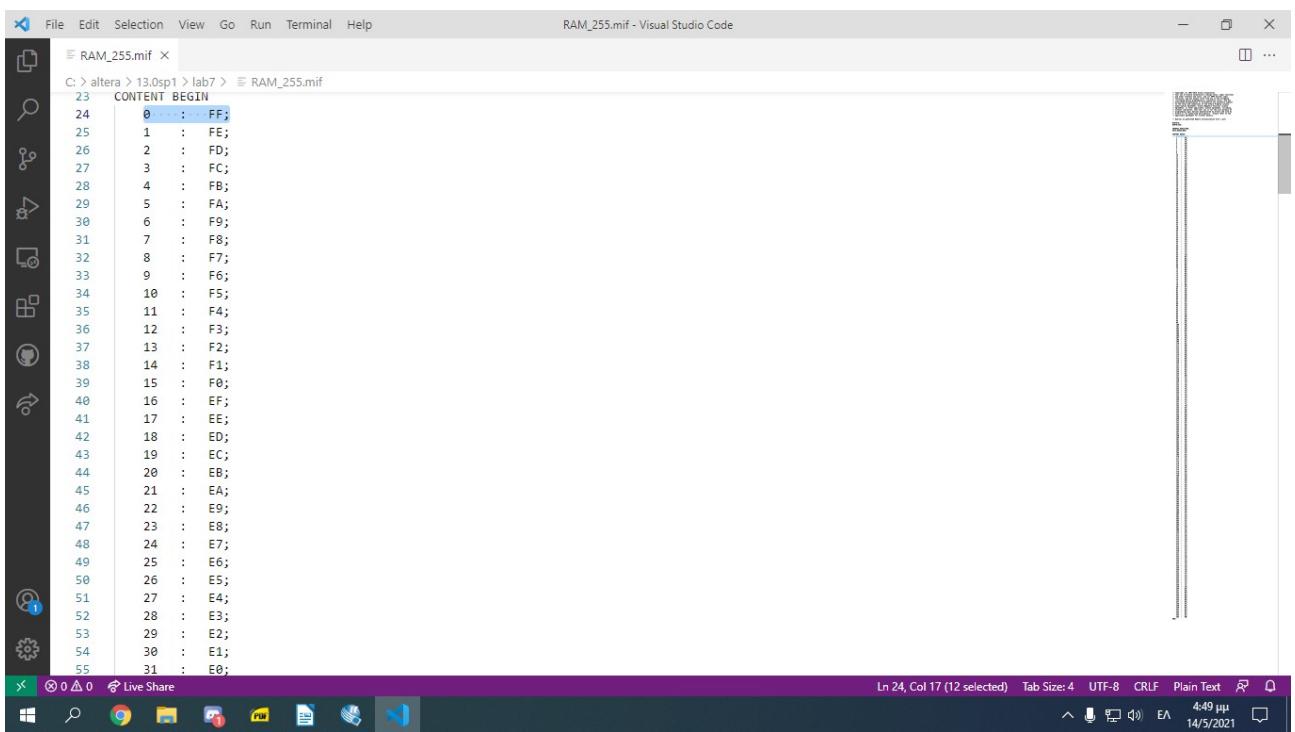
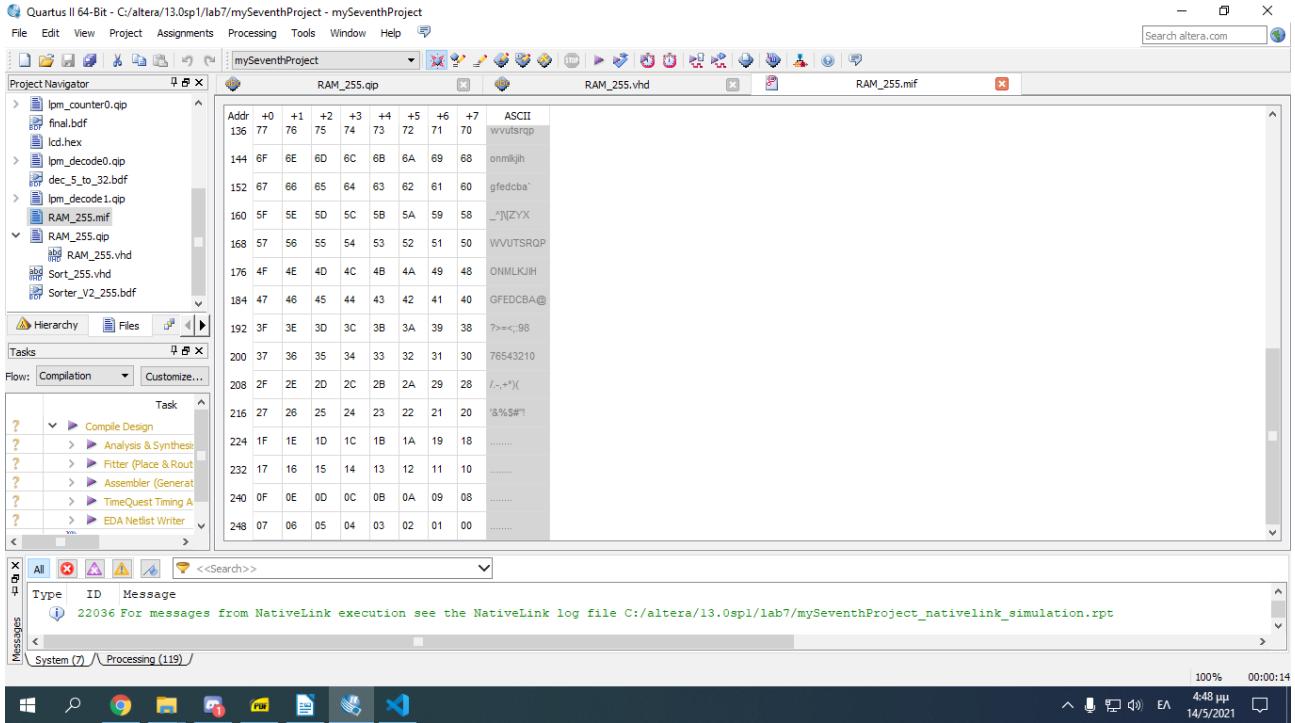
Ακολουθώντας τα βήματα της εκφώνησης φτιάξαμε το παρακάτω κύκλωμα το οποίο και πακετάραμε σε κουτάκι:



Παραδοτέα

Ακολουθώντας την ίδια διαδικασία που κάναμε προηγουμένως για την δημιουργία της μνήμης των 32 θέσεων το μόνο που αλλάξαμε αυτήν την φορά είναι η παράμετρος 32 σε 256 ώστε να έχει τις θέσεις μνήμης από 0 έως 255 και αντίστοιχα δημιουργήσαμε και το αρχείο αρχικοποίησης της μνήμης με όνομα RAM_255.mif στο οποίο βάλαμε και τις αντίστοιχες τιμές που δίνονται στην εκφώνηση. Η μνήμη(RAM_255.vhd) και το αρχείο αρχικοποίησης της φαίνονται στις παρακάτω εικόνες:





Για ευκολία παραλείψαμε τα ενδιάμεσα στιγμιότυπα διότι είναι πάρα πολλά.

File Edit Selection View Go Run Terminal Help

RAM_255.mif - Visual Studio Code

C:\altera>13.0sp1>lab7> RAM_255.mif

```
248      224 : 1F;
249      225 : 1E;
250      226 : 1D;
251      227 : 1C;
252      228 : 1B;
253      229 : 1A;
254      230 : 19;
255      231 : 18;
256      232 : 17;
257      233 : 16;
258      234 : 15;
259      235 : 14;
260      236 : 13;
261      237 : 12;
262      238 : 11;
263      239 : 10;
264      240 : 0F;
265      241 : 0E;
266      242 : 0D;
267      243 : 0C;
268      244 : 0B;
269      245 : 0A;
270      246 : 09;
271      247 : 08;
272      248 : 07;
273      249 : 06;
274      250 : 05;
275      251 : 04;
276      252 : 03;
277      253 : 02;
278      254 : 01;
279      255 : 00;
280 END;
```

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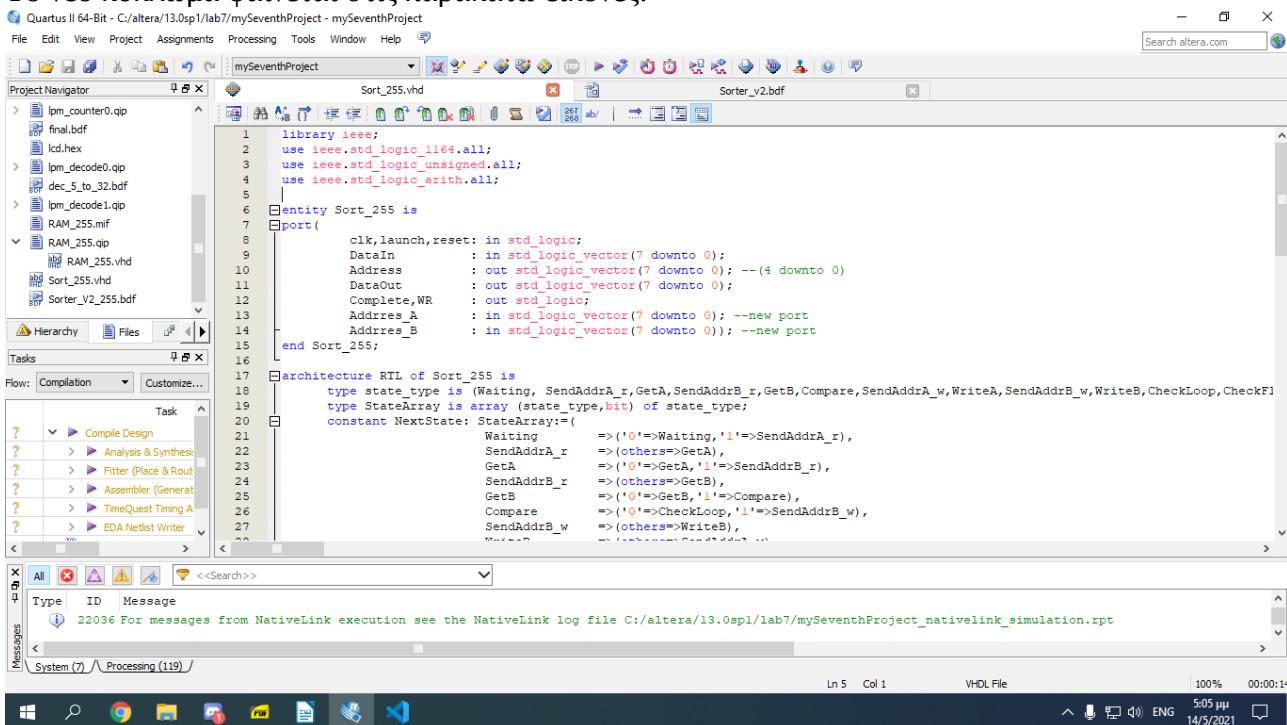
Ln 33, Col 17 Tab Size: 4 UTF-8 CRLF Plain Text

4:50 μ 14/5/2021

Στην συνέχεια τροποποιήσαμε το κύκλωμα του sort ώστε να κάνει τα ζητούμενα.

- Αλλάξαμε το μέγεθος του Address από 5bit σε 8bit
 - Προσθέσαμε δύο επιπλέον εισόδους των 8bit(Addrres_A, Addrres_B)
 - Στην κατάσταση Waiting αλλάξαμε το count="00000" σε count=Addrres_A ώστε να ζεκινάει από την διεύθυνση Addrres_A.
 - Αλλάξαμε το count<=count+"00001" σε count<=count+"00000001" ώστε από 5bit να γίνει 8bit.
 - Αλλάξαμε το count<=count-"00001" σε count<=count-"00000001" ώστε από 5bit να γίνει 8bit.
 - Τέλος για CountEnd=1 αλλάξαμε το count="11111" σε count=Addrres_B ώστε να τερματίζει στην διεύθυνση Addrres_B.

Το νέο κύκλωμα φαίνεται στις παρακάτω εικόνες:



Quartus II 64-Bit - C:/altera/13.0sp1/lab7/mySeventhProject - mySeventhProject

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Sort_255.vhd Sorter_v2.bdf

```

28      WriteB      => (others=>SendAddrA_W),
29      SendAddrA_W  => (others=>WriteA),
30      WriteA      => (others=>CheckLoop),
31      CheckLoop   => ('0'=>SendAddrA_F,'1'=>CheckFlag),
32      CheckFlag   => ('0'=>Waiting,'1'=>SendAddrA_F);

33
34
35      signal state:           state_type;
36      signal dataA,dataB:     std_logic_vector(7 downto 0);
37      signal count:          std_logic_vector(7 downto 0); --(4 downto 0)
38      signal Flag,Swap,CountEnd,condition,delay: std_logic;
39
40 begin
41   FSM:process(clk,reset)
42   begin
43     if(reset='1')then state<=Waiting;
44     elsif(clk'event and clk='1')then state<=NextState(state,to_bit(condition));
45     end if;
46   end process;
47
48   with state select
49     condition<=launch when Waiting,swap when Compare,CountEnd when CheckLoop,Flag when GetA|GetB,'X'
50
51
52   Cnt:process(clk)
53   begin
54     if(clk'event and clk='1')then
55       ...
56   end if;
57   end process;
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```

Quartus II 64-Bit - C:/altera/13.0sp1/lab7/mySeventhProject - mySeventhProject

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Sort_255.vhd Sorter_v2.bdf

```

65      elsif(clk'event and clk='1')then
66          if(state=GetA or state=GetB)then delay<=not delay; end if;
67      end if;
68  end process;
69
70  Seq:process(clk)
71 begin
72     if(clk'event and clk='1')then
73         case(state)is
74             when Waiting | CheckFlag =>Flag<='0';
75             when GetA =>if(delay='1')then dataA<=DataIn; end if;
76             when GetB =>if(delay='1')then dataB<=DataIn; end if;
77             when Compare =>if(Swap='1')then Flag<='1'; end if;
78             when others =>null;
79         end case;
80     end if;
81 end process;
82
83
84 DataOut<=dataA when (state=SendAddrA_w or state=WriteA) else dataB;
85 Address=<count;
86 WR<='1' when state=WriteB or state=WriteA else '0';
87 Swap<='1' when dataA>dataB else '0';
88 CountEnd<='1' when count=Address_B else '0'; --count="1111"
89 Complete<='1' when state=Waiting else '0';
90
91 end RTL;

```

Messages

Type ID Message

22036 For messages from NativeLink execution see the NativeLink log file C:/altera/13.0sp1/lab7/mySeventhProject_nativelink_simulation.rpt

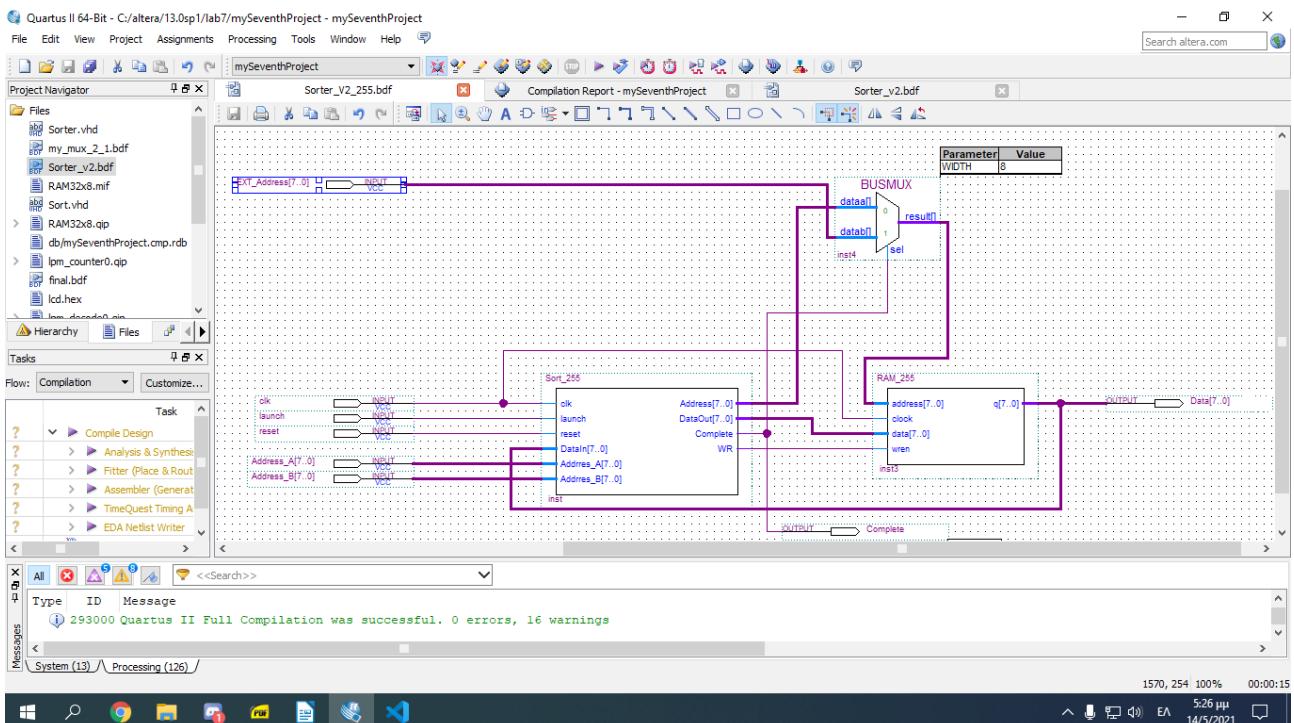
System (7) / Processing (119)

Ln 5 Col 1 VHD File 100% 00:00:14

505 µs ENG 14/5/2021

Στην συνέχεια κάναμε compile χωρίς σφάλματα και βάλαμε το νέο κύκλωμα σε κουτάκι το οποίο και στην συνέχεια το αντικαταστήσαμε με το παλιό στο κύκλωμα του Sorter(Sorter_v2_255.bdf). Επιπλέον αλλάξαμε την παράμετρο WIDTH του MUX από 5bit σε 8bit, την είσοδο EXT_Address από 5bit σε 8bit(EXT_Address[7..0]) καθώς και προσθέσαμε τις εισόδους Address_A[7..0] και Address_B[7..0] των 8bit.

Το τελικό κύκλωμα φαίνεται στην παρακάτω εικόνα:



Στην συνέχεια δημιουργήσαμε μέσα από ρυθμίσεις του Quartus ένα αρχείο Sorter_v2_255.vhd του παραπάνω κυκλώματος με την διαδικασία που περιγράφηκε σε προηγούμενο ερώτημα.
Το κύκλωμα σε μορφή vhdl φαίνεται στις παρακάτω εικόνες:

The screenshot shows the Quartus II 64-Bit software interface. The Project Navigator pane on the left lists files including Sorter_v2_255.vhd, Sorter.vhd, my_mux_2_1.bdf, Sorter_v2.bdf, RAM32x8.mif, Sort.vhd, RAM32x8.qip, db/mySeventhProject.cmp.rdb, lpm_counter0.qip, final.bdf, and test.bdf. The Source Editor pane displays the VHDL code for Sorter_v2_255.vhd. The code includes a copyright notice, program details, library declarations (ieee), and the entity definition for Sorter_V2_255. The entity has a port section with clk, launch, reset, Address_A, Address_B, EXT_Address, Complete, and Data. The architecture section is named bdf_type and contains attributes for black_box and noopt, and a component declaration for busmux_0 with its own port and dataaa, datab, result connections. The Compilation Report pane at the bottom shows a successful compilation with 0 errors and 18 warnings. The Windows taskbar at the bottom right indicates the date as 14/5/2021 and the time as 5:31 μμ.

```

1 -- Copyright (C) 1991-2013 Altera Corporation
2 -- Your use of Altera Corporation's design tools, logic functions
3 -- and other software and tools, and its AMPP partner logic
4 -- functions, and any output files from any of the foregoing
5 -- (including device programming or simulation files), and any
6 -- associated documentation or information are expressly subject
7 -- to the terms and conditions of the Altera Program License
8 -- Subscription Agreement, Altera MegaCore Function License
9 -- Agreement, or other applicable license agreement, including,
10 -- without limitation, that your use is for the sole purpose of
11 -- programming logic devices manufactured by Altera and sold by
12 -- Altera or its authorized distributors. Please refer to the
13 -- applicable agreement for further details.

14
15 -- PROGRAM      "Quartus II 64-Bit"
16 -- VERSION     "Version 13.0.1 Build 232 06/12/2013 Service Pack 1 SJ Web Edition"
17 -- CREATED     "Wed May 12 20:51:54 2021"

18
19 LIBRARY ieee;
20 USE ieee.std_logic_1164.all;
21
22 LIBRARY work;
23
24 ENTITY Sorter_V2_255 IS
25 PORT(
26   clk : IN STD_LOGIC;
27   launch : IN STD_LOGIC;
28   reset : IN STD_LOGIC;
29   Address_A : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
30   Address_B : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
31   EXT_Address : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
32   Complete : OUT STD_LOGIC;
33   Data : OUT STD_LOGIC_VECTOR(7 DOWNTO 0)
34 );
35 END Sorter_V2_255;
36
37 ARCHITECTURE bdf_type OF Sorter_V2_255 IS
38
39   ATTRIBUTE black_box : BOOLEAN;
40   ATTRIBUTE noopt : BOOLEAN;
41
42   COMPONENT busmux_0
43   PORT(sel : IN STD_LOGIC;
44         dataa : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
45         datab : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
46         result : OUT STD_LOGIC_VECTOR(7 DOWNTO 0));
47   END COMPONENT;
48   ATTRIBUTE black_box OF busmux_0: COMPONENT IS true;
49   ATTRIBUTE noopt OF busmux_0: COMPONENT IS true;
50
51   COMPONENT sort_255
52   PORT(...); -- This part is cut off.
53

```

This screenshot shows the same Quartus II 64-Bit interface as the previous one, but with a larger portion of the VHDL code visible in the Source Editor pane. The code continues from the previous snippet, showing the busmux_0 component instantiation and the sort_255 component instantiation. The compilation report at the bottom remains the same, indicating a successful compilation with 0 errors and 18 warnings. The system tray at the bottom right shows the date as 14/5/2021 and the time as 5:31 μμ.

Quartus II 64-Bit - C:/altera/13.0sp1/lab7/mySeventhProject - mySeventhProject

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Sorter_V2_255.vhd Compilation Report - mySeventhProject

Files

- Sorter_V2_255.vhd
- Sorter.vhd
- my_mux_2_1.bdf
- Sorter_v2.bdf
- RAM32x8.mif
- Sort.vhd
- RAM32x8.qip
- db/mySeventhProject.cmp.rdb
- lpm_counter0.qip
- final.bdf
- led.bdf

Hierarchy Files

Tasks Flow: Compilation Customize...

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Rout)
- Assembler (Generate)
- TimeQuest Timing A
- EDA Netlist Writer

Messages

Type	ID	Message
Info	293000	Quartus II Full Compilation was successful. 0 errors, 18 warnings

System (13) / Processing (129)

100% 00:00:15 5:31 μs 14/5/2021

```

49  ATTRIBUTE black_box OF busmux_0: COMPONENT IS true;
50  ATTRIBUTE noopt OF busmux_0: COMPONENT IS true;
51
52  COMPONENT sort_255
53    PORT(clk : IN STD_LOGIC;
54        launch : IN STD_LOGIC;
55        reset : IN STD_LOGIC;
56        Address_A : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
57        Address_B : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
58        DataIn : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
59        Complete : OUT STD_LOGIC;
60        WR : OUT STD_LOGIC;
61        Address : OUT STD_LOGIC_VECTOR(7 DOWNTO 0);
62        DataOut : OUT STD_LOGIC_VECTOR(7 DOWNTO 0)
63    );
64  END COMPONENT;
65
66  COMPONENT ram_255
67    PORT(clock : IN STD_LOGIC;
68        wren : IN STD_LOGIC;
69        address : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
70        data : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
71        q : OUT STD_LOGIC_VECTOR(7 DOWNTO 0)
72    );
73  END COMPONENT;
74
75  SIGNAL  SYNTHESIZED_WIRE_0 : STD_LOGIC_VECTOR(7 DOWNTO 0);
76  SIGNAL  SYNTHESIZED_WIRE_1 : STD_LOGIC;
77  SIGNAL  SYNTHESIZED_WIRE_2 : STD_LOGIC_VECTOR(7 DOWNTO 0);
78  SIGNAL  SYNTHESIZED_WIRE_3 : STD_LOGIC_VECTOR(7 DOWNTO 0);
79  SIGNAL  SYNTHESIZED_WIRE_4 : STD_LOGIC;
80  SIGNAL  SYNTHESIZED_WIRE_5 : STD_LOGIC_VECTOR(7 DOWNTO 0);
81
82
83 BEGIN
84  Complete <= SYNTHESIZED_WIRE_4;
85  Data <= SYNTHESIZED_WIRE_0;
86
87
88  b2w_inst : sort_255
89  PORT MAP(clk => clk,
90            launch => launch,
91            reset => reset,
92            Address_A => Address_A,
93            Address_B => Address_B,
94            DataIn => SYNTHESIZED_WIRE_0,
95            Complete => SYNTHESIZED_WIRE_4,
96            WR => SYNTHESIZED_WIRE_1
97 
```

Quartus II 64-Bit - C:/altera/13.0sp1/lab7/mySeventhProject - mySeventhProject

File Edit View Project Assignments Processing Tools Window Help

Project Navigator Sorter_V2_255.vhd Compilation Report - mySeventhProject

Files

- Sorter_V2_255.vhd
- Sorter.vhd
- my_mux_2_1.bdf
- Sorter_v2.bdf
- RAM32x8.mif
- Sort.vhd
- RAM32x8.qip
- db/mySeventhProject.cmp.rdb
- lpm_counter0.qip
- final.bdf
- led.bdf

Hierarchy Files

Tasks Flow: Compilation Customize...

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Rout)
- Assembler (Generate)
- TimeQuest Timing A
- EDA Netlist Writer

Messages

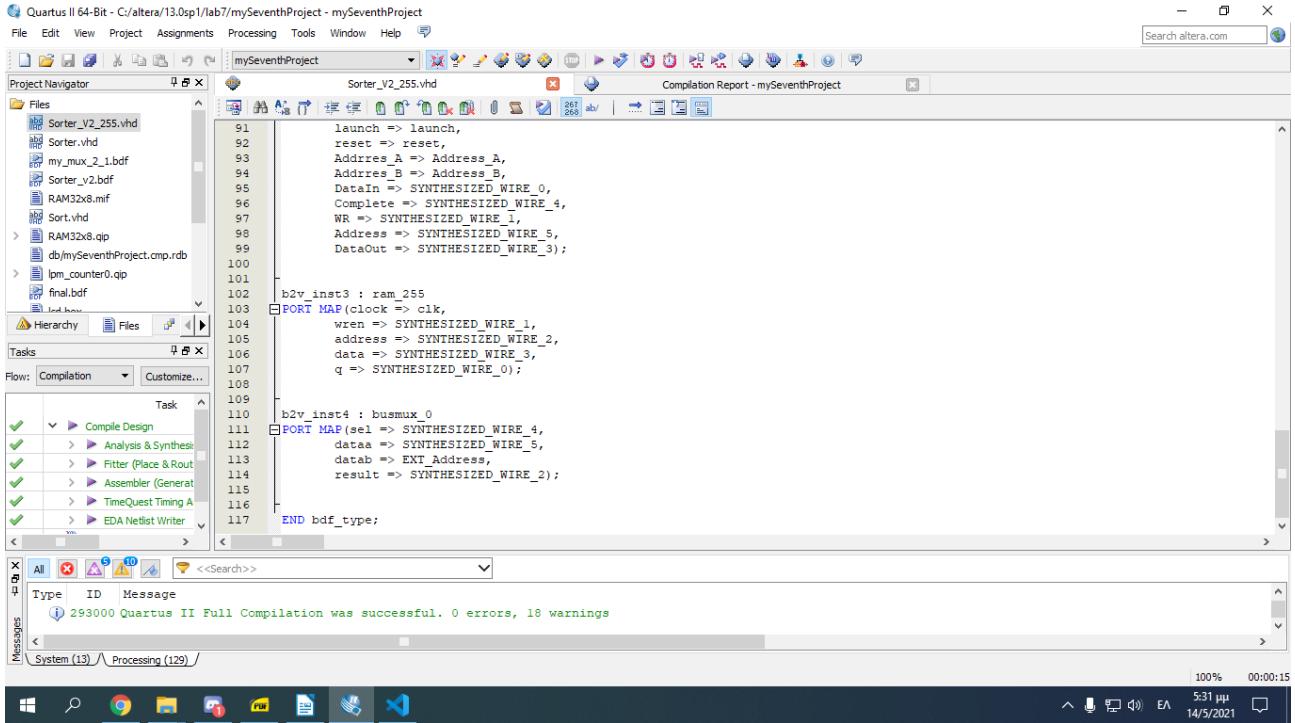
Type	ID	Message
Info	293000	Quartus II Full Compilation was successful. 0 errors, 18 warnings

System (13) / Processing (129)

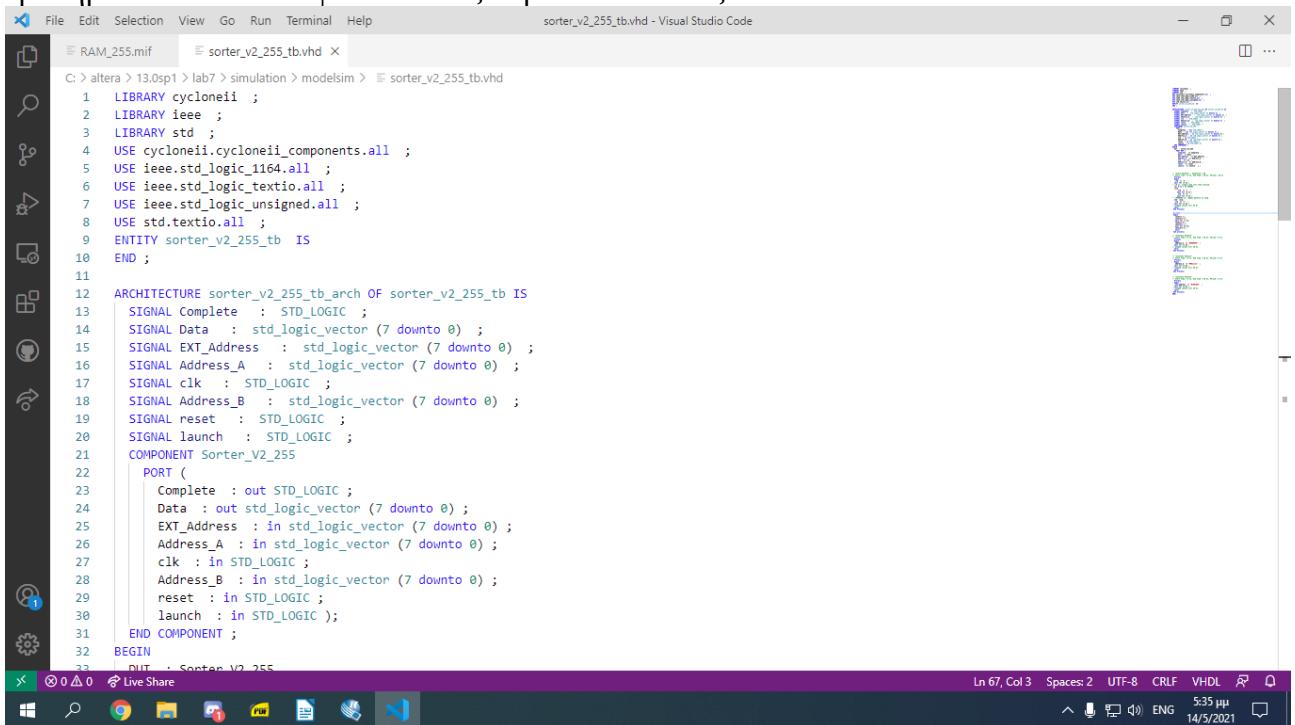
100% 00:00:15 5:31 μs 14/5/2021

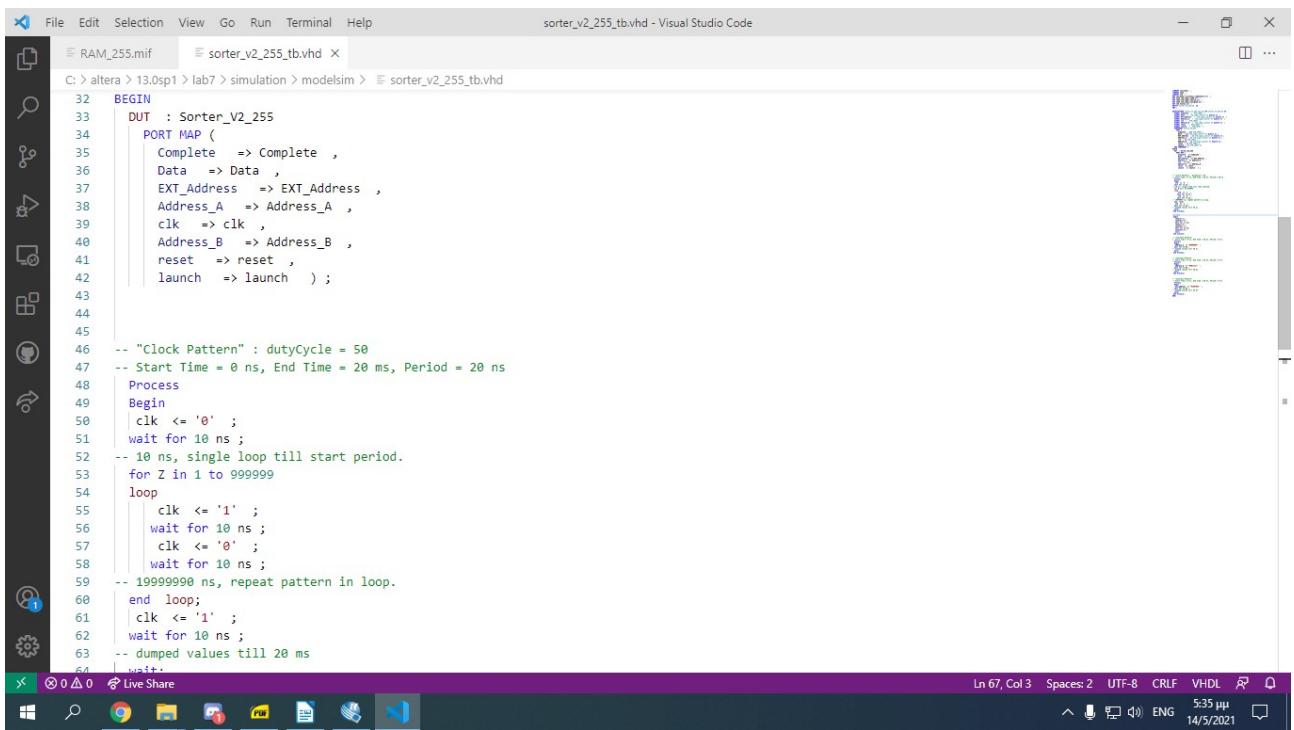
```

70  data : IN STD_LOGIC_VECTOR(7 DOWNTO 0);
71  q : OUT STD_LOGIC_VECTOR(7 DOWNTO 0)
72  );
73 END COMPONENT;
74
75 SIGNAL  SYNTHESIZED_WIRE_0 : STD_LOGIC_VECTOR(7 DOWNTO 0);
76 SIGNAL  SYNTHESIZED_WIRE_1 : STD_LOGIC;
77 SIGNAL  SYNTHESIZED_WIRE_2 : STD_LOGIC_VECTOR(7 DOWNTO 0);
78 SIGNAL  SYNTHESIZED_WIRE_3 : STD_LOGIC_VECTOR(7 DOWNTO 0);
79 SIGNAL  SYNTHESIZED_WIRE_4 : STD_LOGIC;
80 SIGNAL  SYNTHESIZED_WIRE_5 : STD_LOGIC_VECTOR(7 DOWNTO 0);
81
82
83 BEGIN
84  Complete <= SYNTHESIZED_WIRE_4;
85  Data <= SYNTHESIZED_WIRE_0;
86
87
88  b2w_inst : sort_255
89  PORT MAP(clk => clk,
90            launch => launch,
91            reset => reset,
92            Address_A => Address_A,
93            Address_B => Address_B,
94            DataIn => SYNTHESIZED_WIRE_0,
95            Complete => SYNTHESIZED_WIRE_4,
96            WR => SYNTHESIZED_WIRE_1
97 
```



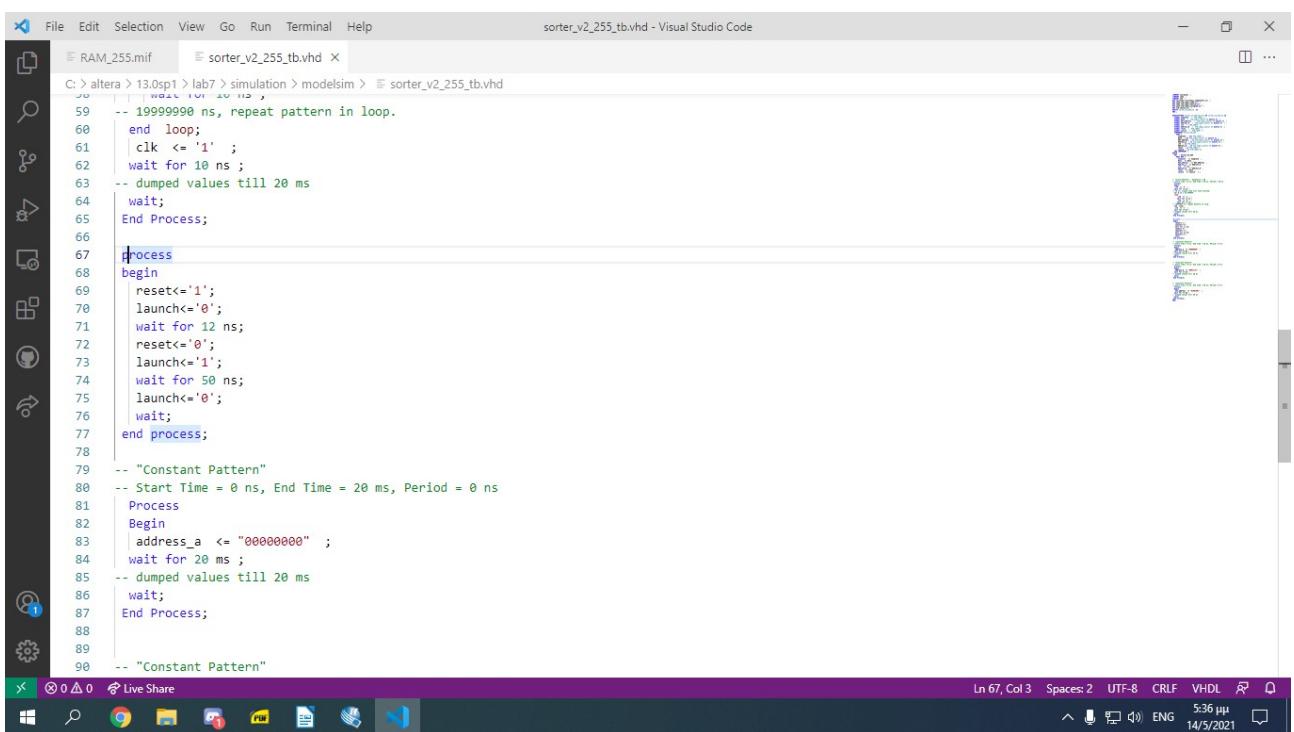
Κάναμε compile το νέο κύκλωμα Sorter_v2_255.vhd χωρίς σφάλματα και δημιουργήσαμε ένα test_bench με όνομα sorter_v2_255_tb.vhd με την διαδικασία που περιγράφηκε σε προηγούμενο ερώτημα. To test bench φαίνεται στις παρακάτω εικόνες:





```
File Edit Selection View Go Run Terminal Help sorter_v2_255_tb.vhd - Visual Studio Code
RAM_255.mif sorter_v2_255_tb.vhd
C:\altera>13.0sp1>lab7>simulation>modelsim>sorter_v2_255_tb.vhd
32 BEGIN
33   DUT : Sorter_V2_255
34   PORT MAP (
35     Complete => Complete ,
36     Data => Data ,
37     EXT_Address => EXT_Address ,
38     Address_A => Address_A ,
39     clk => clk ,
40     Address_B => Address_B ,
41     reset => reset ,
42     launch => launch ) ;
43
44
45
46 -- "Clock Pattern" : dutyCycle = 50
47 -- Start Time = 0 ns, End Time = 20 ms, Period = 20 ns
48 Process
49 Begin
50   clk <= '0' ;
51   wait for 10 ns ;
52   -- 10 ns, single loop till start period.
53   for Z in 1 to 999999
54   loop
55     clk <= '1' ;
56     wait for 10 ns ;
57     clk <= '0' ;
58     wait for 10 ns ;
59   -- 19999990 ns, repeat pattern in loop.
60   end loop;
61   clk <= '1' ;
62   wait for 10 ns ;
63   -- dumped values till 20 ms
64   wait;
65 End Process;
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```

Ln 67, Col 3 Spaces: 2 UTF-8 CRLF VHDL 5:35 μμ 14/5/2021



```
File Edit Selection View Go Run Terminal Help sorter_v2_255_tb.vhd - Visual Studio Code
RAM_255.mif sorter_v2_255_tb.vhd
C:\altera>13.0sp1>lab7>simulation>modelsim>sorter_v2_255_tb.vhd
50   -- 19999990 ns, repeat pattern in loop.
51   end loop;
52   clk <= '1' ;
53   wait for 10 ns ;
54   -- dumped values till 20 ms
55   wait;
56 End Process;
57
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```

Ln 67, Col 3 Spaces: 2 UTF-8 CRLF VHDL 5:36 μμ 14/5/2021

```

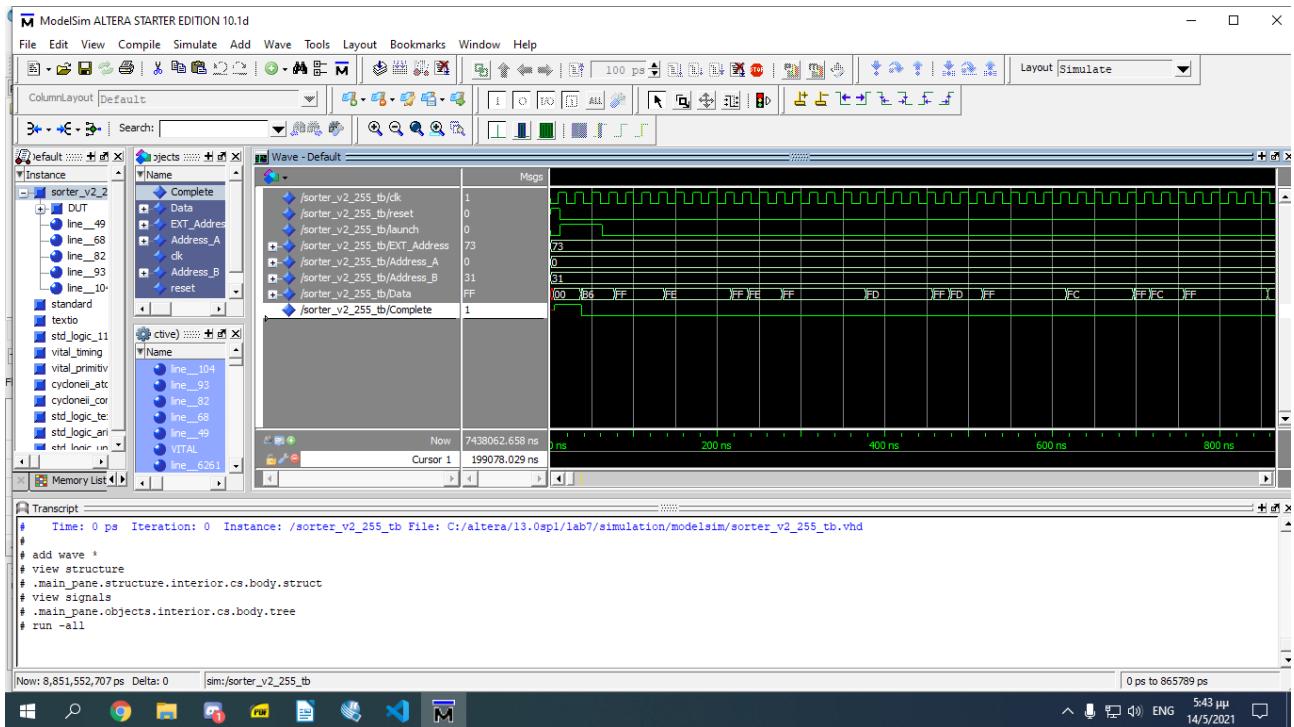
File Edit Selection View Go Run Terminal Help sorter_v2_255_tb.vhd - Visual Studio Code
C:\altera>13.0sp1>lab7>simulation>modelsim>sorter_v2_255_tb.vhd
RAM_255.mif sorter_v2_255_tb.vhd
79 | -- "Constant Pattern"
80 |-- Start Time = 0 ns, End Time = 20 ms, Period = 0 ns
81 | Process
82 | Begin
83 | | address_a <= "0000000" ;
84 | | wait for 20 ms ;
85 |-- dumped values till 20 ms
86 | | wait;
87 | End Process;
88 |
89 |
90 |-- "Constant Pattern"
91 |-- Start Time = 0 ns, End Time = 20 ms, Period = 0 ns
92 | Process
93 | Begin
94 | | address_b <= "0001111" ;
95 | | wait for 20 ms ;
96 |-- dumped values till 20 ms
97 | | wait;
98 | End Process;
99 |
100 |
101 |-- "Constant Pattern"
102 |-- Start Time = 0 ns, End Time = 20 ms, Period = 0 ns
103 | Process
104 | Begin
105 | | ext_address <= "01001001" ;
106 | | wait for 20 ms ;
107 |-- dumped values till 20 ms
108 | | wait;
109 | End Process;
110 | END;

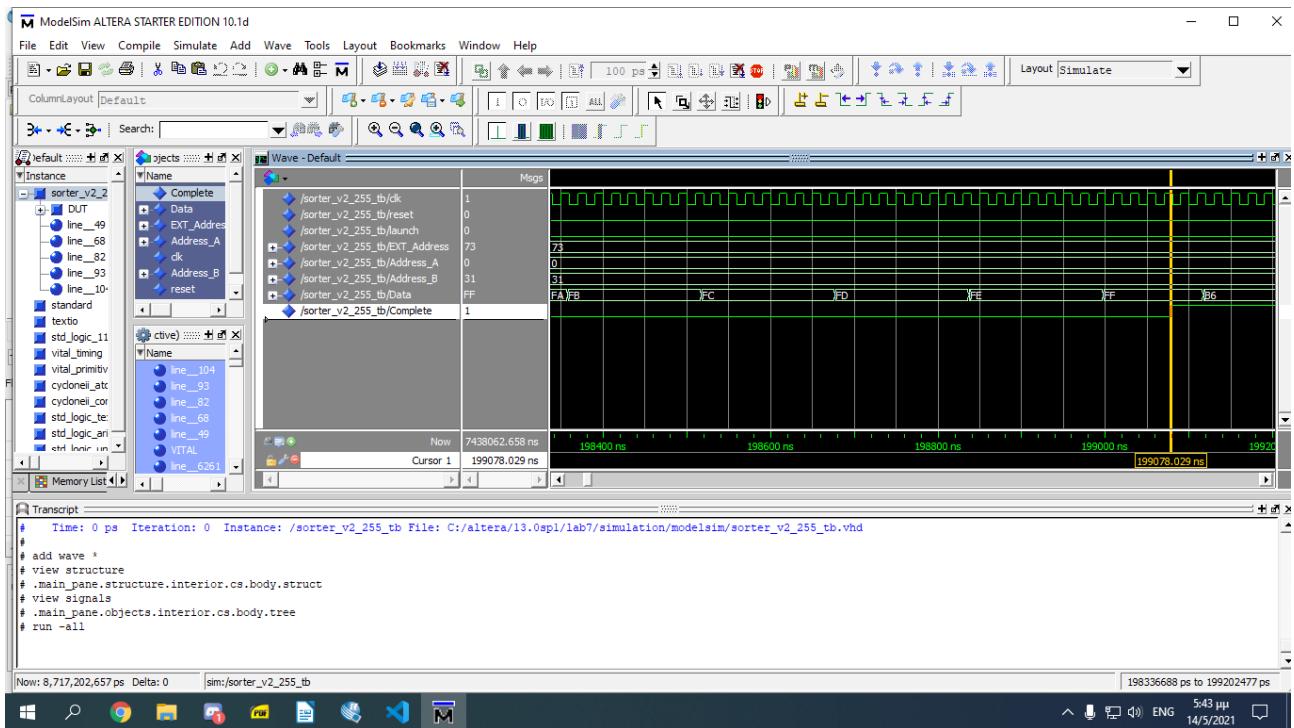
```

Live Share

Ln 67, Col 3 Spaces: 2 UTF-8 CRLF VHDL 5:36 μμ 14/5/2021

Στην συνέχεια εκτελέσαμε gate level simulation με Address_A=0 και Address_B=31 παρατηρούμε ότι το κύκλωμα λειτουργεί ακριβώς όπως και στην περίπτωση των 32 θέσεων όπως φαίνεται στις παρακάτω εικόνες:





Εκτελούμε ξανά την εξομοίωση αυτήν την φορά όμως με Address_A="00010101" και Address_B="00011000"(AM=3321). Η εξομοίωση φαίνεται στις παρακάτω εικόνες:

