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Analog Audio Amplifier with JFET Saturation

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Contents

1. OVERVIEW

This document describes the design, simulation, and implementation of an analog audio amplifier intended for guitar-level signals. The project focuses on gain staging, tone shaping, and controlled nonlinear behavior using a JFET saturation stage. The work includes schematic design, circuit simulation, breadboard prototyping, PCB layout, and final assembly, with performance verified through frequency response, distortion, and noise analysis.

2. SPECIFICATIONS

2.1 Inputs/Outputs

2.1.1 Input: ¼" Unbalanced TS
2.1.2 Nominal Input Level: 100 mV RMS (≈ -20 dBV) @ 1 kHz
2.1.3 Maximum Input Level: 300 mV RMS (≈ -10.5 dBV) @ 1 kHz (clean headroom not guaranteed)
2.1.4 Input Impedance: > 1M Ω
2.1.5 Output: ¼" Unbalanced TS
2.1.6 Rated Load: > 10 kΩ (typical instrument/line input)
2.1.7 Output Impedance: < 1kΩ
2.1.8 Maximum Output level (before hard clipping):

2.2 User Interface/Controls

2.2.1 BYPASS: True Bypass (3PDT or relay) 2 position footswitch
2.2.2 INDICATOR: LED On/off (with series resistor sized for 9v)
2.2.3 GAIN: Input Stage Gain (controls drive into JFET stage)
2.2.4 MASTER: Output level trim (post-processing)
2.2.5 LOW: Baxandall bass boost/cut, flat at center
2.2.6 HIGH: Baxandall treble boost/cut, flat at center

2.3 Gain/Frequency Response

2.3.1 Gain Structure: Input gain stage, JFET Saturation Stage, Buffer, active Baxandall EQ, Output Buffer, Master Level
2.3.2 Midband Gain Range (tone flat): 0 to +20 dB
2.3.3 Gain at neutral controls ("12 o'clock"): 0 dB +/- 3dB
2.3.4 Frequency Response (tone flat): +/- 3 dB from 20 Hz to 20 kHz
2.3.5 Low Frequency Cutoff: < 20 Hz
2.3.6 High Frequency Cutoff: >20 kHz

2.4 Tone Control (EQ)

2.4.1 Type: Active Baxandall 2-band EQ
2.4.2 Bands: Bass, Treble
2.4.3 Range: +/- 10 to +-15 dB boost/cut (tone controls centered, nominally flat)
2.4.4 Turnover Frequencies (nominal): ≈ 1 kHz

2.5 Distortion

2.5.1 THD (clean condition): <1% @ 1 kHz, nominal input, neutral controls
2.5.2 THD (driven condition): Adjustable up to 15% @ 1kHz with higher Vin and Gain settings
2.5.3 Harmonic Content: Even order dominant

2.6 Noise/Dynamic Range

2.6.1 Output Noise (20 – 20 kHz, tone flat): < 200 uV RMS referenced to output, input shorted
2.6.2 SNR (nominal): > 70 dB with 100 mV RMS input @ 1 kHz, controls neutral, MASTER set for nominal output level
2.6.3 Dynamic Range: 85 dB +

2.7 Power/Implementation

2.7.1 Supply: 9v DC (center negative pedal standard)
2.7.2 Current Draw:
2.7.3 Reverse Polarity Protection: Yes

2.8 Physical Layout

2.8.1 PCB: Through Hole

3. THEORY OF OPERATION

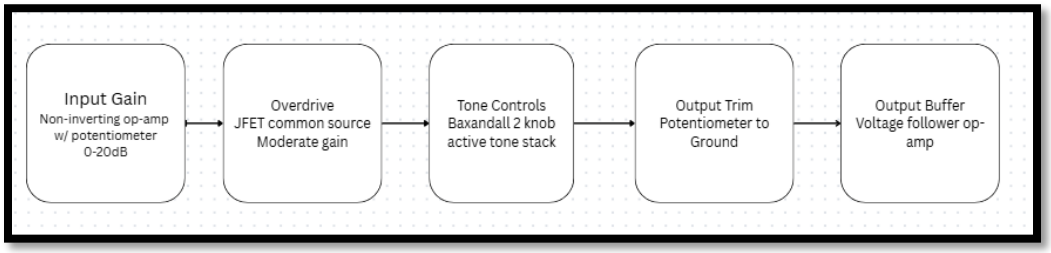
3.1 Overview

This circuit is an analog audio amplifier designed for guitar-level signals, with controllable gain, tone shaping, and soft JFET saturation. It operates from a single 9 V supply and uses a mid-supply virtual ground to allow single-supply op-amp stages.

The signal path is divided into several functional stages. An input gain stage provides high input impedance and adjustable clean gain. This stage sets the overall signal level and determines how hard the following JFET stage is driven. At low gain settings the circuit behaves as a clean boost, while higher gain settings drive the JFET into saturation.

The JFET stage is biased to operate near cutoff, producing soft, asymmetrical clipping that emphasizes even-order harmonics. The amount of distortion is not fixed and depends on both the input signal level and the gain setting of the preceding stage, resulting in a dynamic, touch-sensitive response rather than hard clipping.

Following the JFET, a unity-gain buffer isolates the nonlinear stage from the tone control network. This prevents loading effects and ensures consistent behavior of the saturation stage across different tone settings.



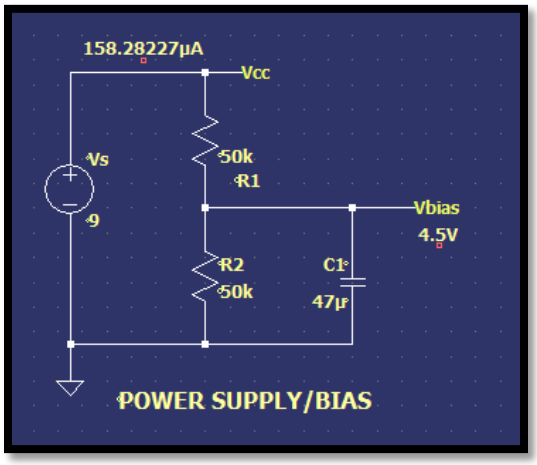
Tone shaping is performed using an active two-band Baxandall equalizer, providing independent boost and cut of low and high frequencies around a flat midband response. The EQ is centered around a neutral “flat” position and is capable of both subtle correction and more pronounced tonal shaping.

The final stage is a unity-gain output buffer followed by a potentiometer that serves as a master output level control. This stage provides low output impedance and allows the overall output level to be adjusted without affecting the gain structure or distortion characteristics of earlier stages.

3.2 Power Supply and Bias Generation

The circuit runs from a single 9 V supply. Since the op-amp stages need to process an AC signal that swings both above and below a reference point, the circuit creates a mid-supply reference voltage, Vbias, at approximately 4.5 V. This node acts as the “virtual ground” for the signal path.

Vbias is generated using a simple resistor divider. A large capacitor from Vbias to ground provides a low-impedance AC path, so Vbias stays stable and does not move with the audio signal. Keeping this node quiet is important: if Vbias is noisy or has significant impedance at audio frequencies, it can inject hum, add distortion, or create unintended feedback between stages.

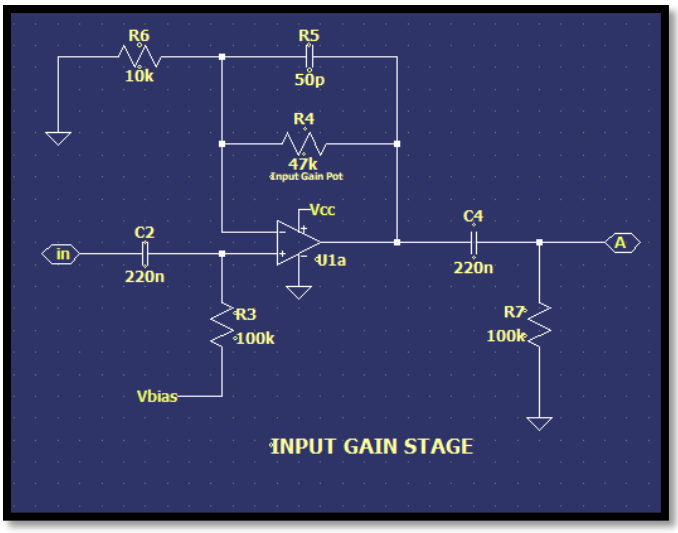


Vbias is then distributed to the op-amp input and feedback networks wherever a DC reference is needed. Any node that is tied to Vbias for biasing is treated as an AC ground in the small-signal sense, meaning the signal rides on top of a steady DC offset while the audio itself is referenced to the virtual ground.

For stability, each active stage also uses local supply decoupling near the op-amp package to reduce oscillation risk and keep transients from one stage from coupling into another through the supply rails.

3.3 Input Gain Stage

The input stage provides high input impedance and adjustable clean gain, and establishes the signal level driving the nonlinear stages that follow. This stage is intended to remain linear across its operating range so that distortion is dominated by the JFET saturation stage rather than the input amplifier.



The input signal is AC-coupled into the circuit to block any external DC offset. A high-value resistor ties the input node to Vbias, setting the DC operating point while maintaining a high input impedance appropriate for guitar and line-level sources. The coupling capacitor and bias resistor form a first-order high-pass filter with a cutoff frequency well below the audio band, ensuring negligible low-frequency attenuation

The op-amp is configured as a non-inverting amplifier referenced to Vbias. Gain is set by the feedback network, which includes a logarithmic potentiometer to provide smooth, perceptually useful control over gain. At minimum setting, the stage operates near unity gain, while higher settings provide progressively greater voltage amplification.

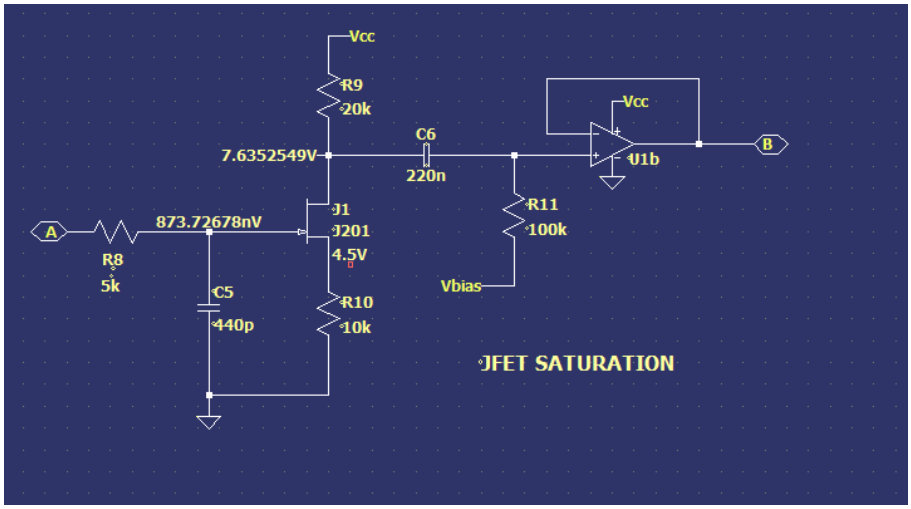
A capacitor in the feedback path limits low-frequency gain, preventing excessive amplification of sub-audio content and improving stability at higher gain settings. A small series resistor at the op-amp output isolates the device from capacitive loading due to coupling capacitors and downstream wiring, reducing the risk of high-frequency oscillation.

The output of this stage is AC-coupled into the JFET stage, removing the Vbias offset and allowing the JFET to establish its own DC operating point. The overall function of the input gain stage is to provide controlled, low-noise amplification and to determine the drive level applied to the saturation stage under a wide range of input conditions.

3.4 *JFET Saturation Stage*

The JFET stage is the primary source of intentional nonlinearity in the amplifier. It is implemented as a common-source amplifier and is biased to operate near cutoff, where the device exhibits asymmetric transfer characteristics. This bias point favors the generation of even-order harmonics as the signal level increases, producing soft, musically useful saturation rather than hard clipping.

The gate of the JFET is driven from the preceding stage through a series resistor, which acts as a gate stopper to limit high-frequency content and reduce the risk of parasitic oscillation. The input signal is AC-coupled into the gate, allowing the JFET to establish its own DC operating point independently of the op-amp stages.

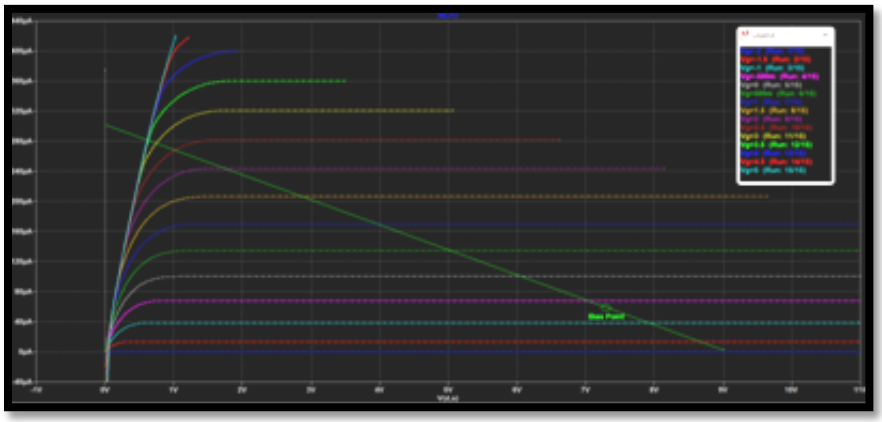


The drain resistor sets the DC operating point and small-signal gain of the stage, while the source resistor provides self-biasing and local negative feedback. Together, these components position the quiescent operating point close to cutoff without forcing the device into abrupt conduction. As the input signal amplitude increases, the JFET transitions smoothly into saturation, producing a gradual increase in distortion rather than a sharp clipping threshold.

A small capacitor at the gate is used to limit excessive high-frequency gain, preventing brittle distortion and improving stability under large-signal conditions. The output of the JFET stage is AC-coupled to remove its DC offset before being passed to the following buffer stage.

The amount of distortion produced by this stage is not fixed. It depends on both the input signal level and the gain setting of the preceding stage, making the response dynamic and touch-sensitive. At lower drive levels the stage contributes minimal coloration, while higher drive levels produce progressively stronger harmonic content dominated by even-order components.

To prevent loading effects and preserve consistent saturation behavior, the JFET stage is followed by a unity-gain buffer. This buffer presents a high input impedance to the JFET and a low output impedance to the tone control stage, ensuring that changes in tone settings do not alter the operating conditions of the saturation stage.



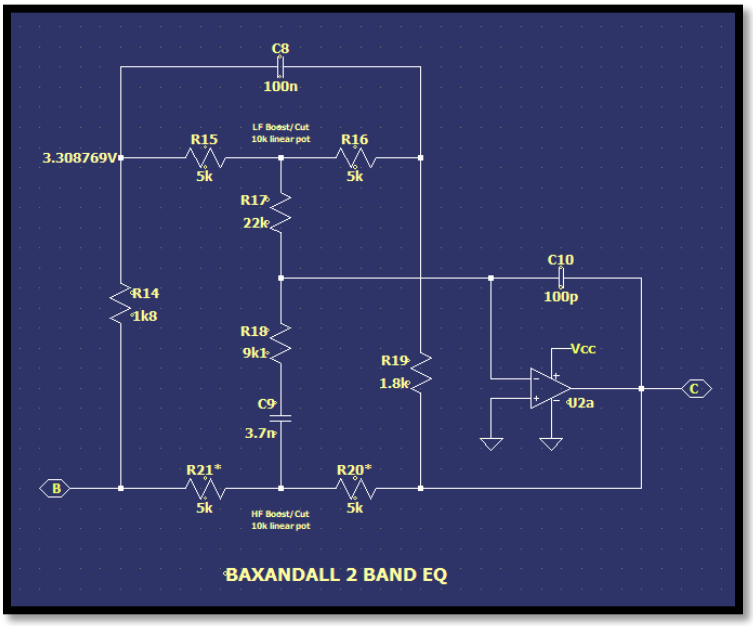
3.5 *Baxandall 2-Band Tone Control*

Tone shaping is provided by an active two-band Baxandall equalizer, offering independent boost and cut of low and high frequencies with an approximately flat response when the controls are centered. The active topology provides predictable control behavior and minimizes interaction between the bass and treble adjustments.

The tone control is placed after the JFET saturation stage so that nonlinear characteristics are established prior to frequency shaping. This allows the equalizer to act as a post-distortion tonal adjustment without influencing the clipping behavior of the circuit.

The bass and treble controls operate through frequency-selective feedback networks that adjust gain below and above their respective turnover frequencies. When both controls are set to their midpoint, the midband response remains nominally flat.

The tone network is buffered at both its input and output to isolate it from surrounding stages. This ensures consistent frequency response across the full range of control settings and prevents loading effects from altering the behavior of the saturation stage or output stage.

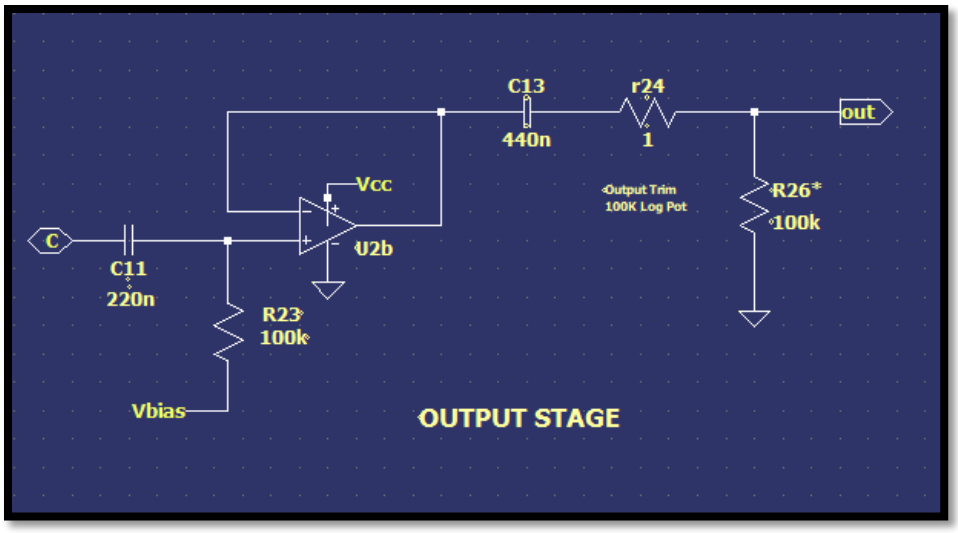


3.6 *Output Stage*

The output stage consists of a unity-gain buffer followed by a potentiometer that serves as a master output level control. The buffer provides a low output impedance and isolates the preceding tone control stage from variations in load and cable capacitance.

The output level control allows the final signal amplitude to be adjusted without altering the gain structure or distortion characteristics of earlier stages. This ensures that overall output level can be set independently of the input gain and saturation behavior.

The buffered output is AC-coupled to remove the DC bias component before being presented at the output jack. This stage ensures compatibility with downstream equipment and maintains stable performance across a range of loads.



4. SIMULATION TESTING

Simulation was used to verify that the circuit meets the design targets across a practical range of operating conditions. Tests focused on frequency response, tone control range, gain structure, and nonlinear behavior (THD and harmonic content). Unless otherwise noted, all simulations were performed in LTspice with the circuit biased from a single 9 V supply and referenced to Vbias.

4.1 Test Conditions

4.1.1 Nominal Input Level: 100 mV RMS
4.1.2 High Input Level: 300 mV RMS
4.1.3 Reference Frequency for gain/THD: 1 kHz
4.1.4 Neutral Tone Setting: Controls centered (“12 o’clock”)
4.1.5 Max Settings: GAIN max, BASS max, TREBLE max, MASTER as needed
4.1.6 Load Condition: 10 kΩ
4.1.7 Measurement Points: Gains measured as 20Log10(Vout/Vin)

4.2 DC Operating Point

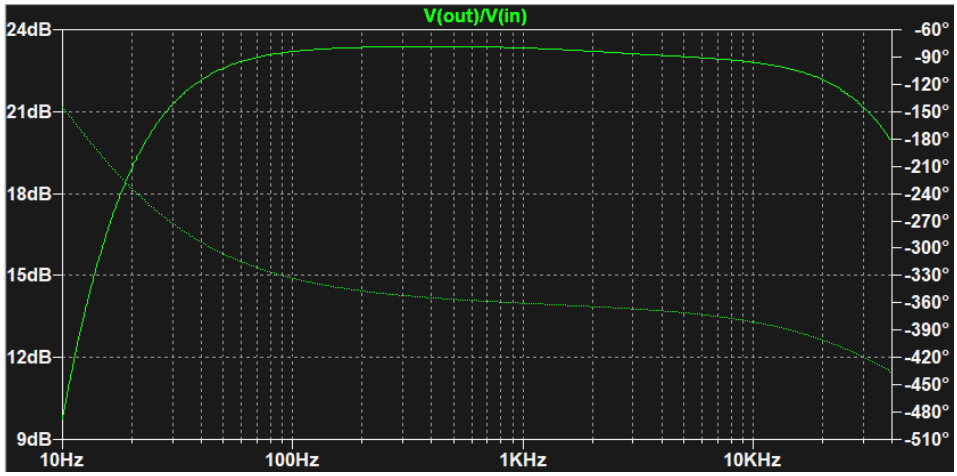
A DC operating point analysis was run to confirm expected bias levels and headroom throughout the signal path, including Vbias stability and JFET operating region

4.2.1 VBias: 4.5 v
4.2.2 JFET Quiescent ID: 120 uA
4.2.3 JFET Vgs: - 0.599 V
4.2.4 JFET Vds: 6.00 V

4.3 Small-Signal Frequency Response (flat tone settings

An AC analysis was performed with tone controls at neutrol position to verify a flat passband response and confirm LF/HF cutoff frequencies.

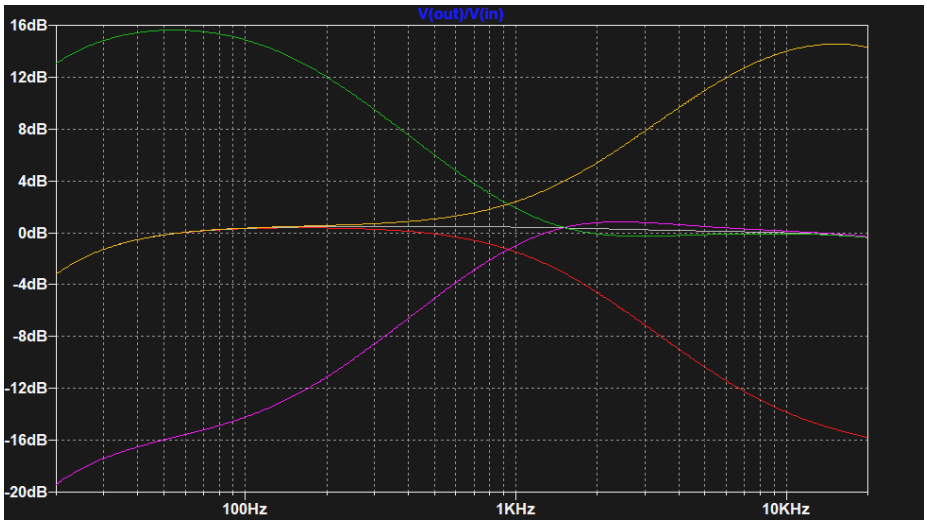
4.3.1 Passband Gain @ 1 kHz: 23.3 dB
4.3.2 Low cutoff (-3 dB): 37 Hz
4.3.3 High cutoff (-3 dB): 37 kHz
4.3.4 Passband Flatness (20 Hz – 20 kHz): 4.42 dB (1 dB from 50 Hz to 17 kHz)



4.4 Tone Control Range

To characterize the Baxandall EQ, AC response was simulated while sweeping the bass and treble controls through their ranges. Plots are shown for extreme settings and representative intermediate positions.

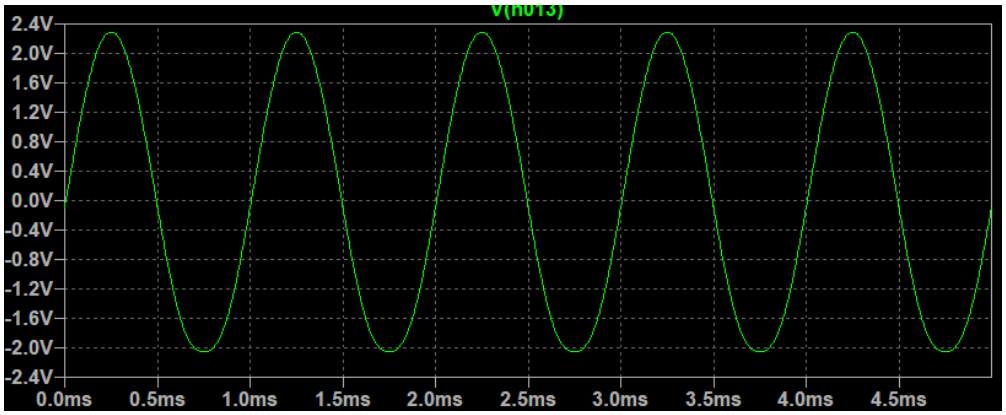
4.4.1 Bass, Maximum Boost: +16 dB
4.4.2 Bass, Maximum Cut: -16 dB
4.4.3 Bass, Turnover Frequency: 730-750 Hz
4.4.4 Treble, Maximum Boost: +14 dB
4.4.5 Treble, Maximum Cut: -16 dB
4.4.6 Treble, Turnover Frequency: 1.3 – 1.5 kHz



4.5 Distortion Characteristics

Distortion was quantified using Fourier analysis under defined operating points. For each case, THDand harmonic distortion were recorded, with emphasis on the H2:H3 ratio as a proxy for even-order dominance.

4.5.1 Clean/Nominal case: 0.927% THD, H2:H3 12.8:1
4.5.2 Driven case: 4.851% THD, H2:H3 3.2:1
4.5.3 Maximum driven Case: 16.292% THD, 2.33:1



4.6 Noise Analysis

A noise analysis was run to estimate the output-referred noise and compute SNR under nominal conditions.

4.6.1 Output Noise Density: 136 nV/Hz @ 1 kHz
4.6.2 Integrated Output Noise: 46.287 uV from 20 Hz to 20 kHz at nominal input
4.6.3 SNR at nominal Output Level: 90.7 dB
4.6.4 Dynamic Range: 86.7 dB (20 Hz to 20 kHz, output referred, 1% THD)