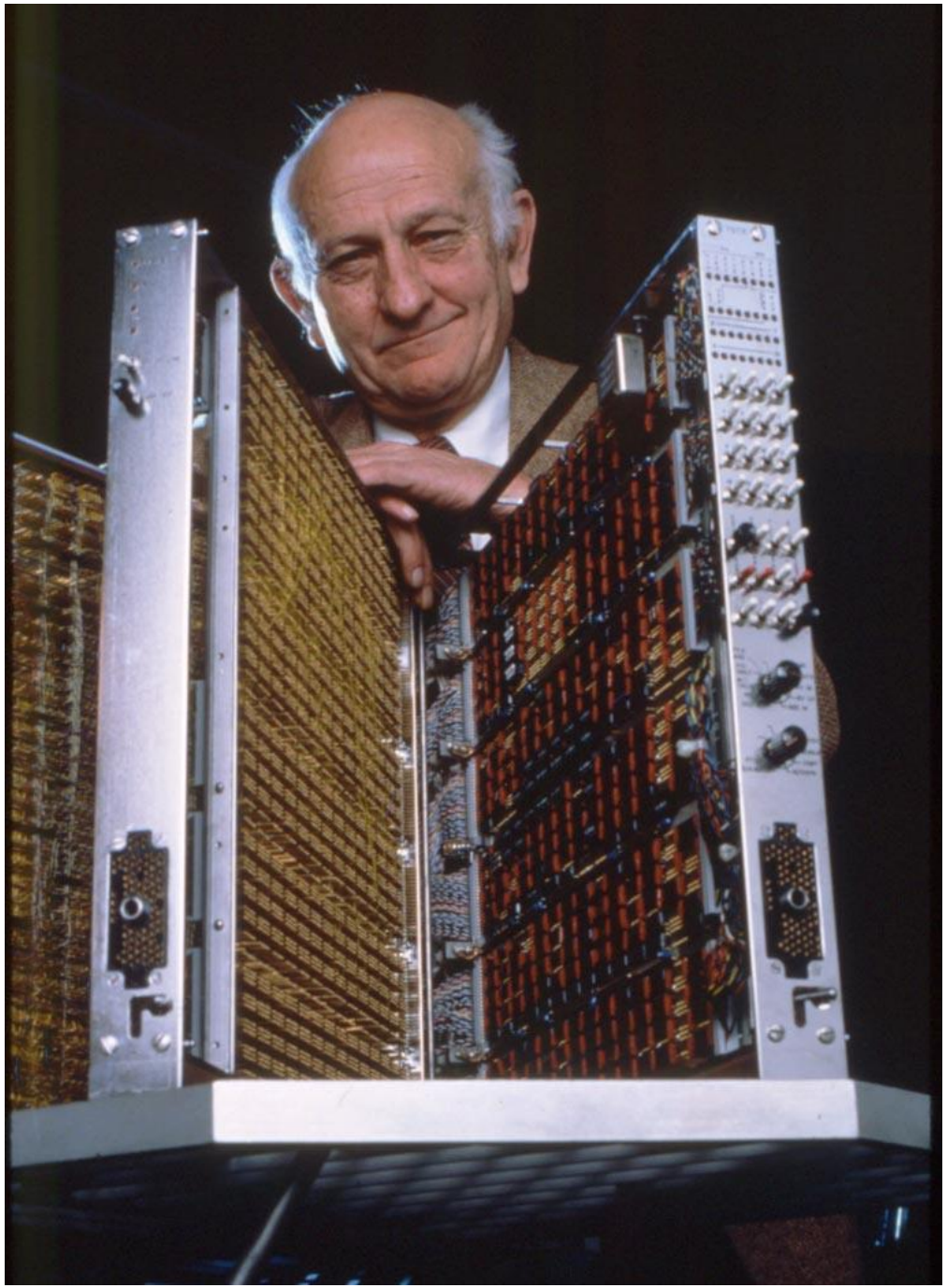

John Cocke

"If I see an opportunity, I drop all the rules, even when doing so is probably a mistake."

RISC ARCHITECTURE

COMPILER OPTIMIZATION

JOHN SHIELDS - G00348436

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Introduction

In the early 1970s, John Cocke transformed computing by simplifying the set of instructions that tell computers which functions to perform.

Cocke was the Turing award winner of 1987. Cocke won this award for his significant contributions in the design and theory of compilers, the architecture of large systems and the development of RISC, for discovering and systematizing many fundamental transformations now used in optimizing compilers including the reduction of:

- Operator Strength
- Elimination of Common Subexpressions
- Register Allocation
- Constraint Propagation
- Dead Code Elimination

RISC Architecture

- Reduced Instruction Set Computers.
- Simpler hardware by using a reduced instruction set
- Although this is a reduced instruction set this approach tries to increase the CPU performance.
- Reduce the cycles per instruction at the cost of the number of instructions per program.

Characteristic of RISC

- Relatively few instructions
- One word instructions
- Instruction take a single clock cycle to get executed
- More number of general purpose register
- Simple Addressing Modes
- Less Data types
- Pipeline can be achieved

Pipelining

- Pipelining a standard feature in RISC processors, is much like an assembly line because the processor works on different steps of the instruction at the same time, more instructions can be executed in a shorter period of time.
- Pipelining is a technique of decomposing a sequential process into sub-processes, with each sub-process being executed in a special dedicated segment that operates concurrently with all other segments
- Any operation that can be composed into a sequence of a sub-operation of about the same complexity can be implemented by a pipeline processor

RISC Projects

John Cocke was involved in three RISC projects:

- IBM 801 machine (1974)
- Berkeley's RISC-I and RISC-II processors (1980)
- Stanford's MIPS processor (1981)

IBM 801 machine

- Experimental minicomputer
- Telephone switch to handle a million calls per hour
- 6 MIPS processor.
- Thomas J. Watson Research Center
- IBM used the resulting architecture in various roles out through to the 1980s

Berkeley’s RISC-I processors

- Originally known as Gold
- VLSI design course
- ACM ISCA
- 44,500 transistors
- 31 instructions
- 78 32-bit registers

Berkeley’s RISC-II processors

- Blue design
- 138 registers
- 8 windows
- 16 registers each
- 10 globals
- RISC instruction set with only 39,000 transistors

Stanford’s MIPS processor

- Strong background in compilers
- Develop a processor
- MIPS processor implemented a smaller and simpler instruction set
- 32 registers
- 32 bits wide

Stretch

- Also known as the IBM 7030 System
- A supercomputer created in 1961 that was considered the fastest computer at it’s time.
- It’s technical goal was to be 100 times faster than the IBM 704 however it did not reach this requirement.
- While considered a technical failure, it’s work with partitioning, lookahead and pipelining paved the way for IBM and contributed towards many of their future works and the project is considered a major success in hindsight.

The concept of RISC

- "We knew we wanted a computer with a simple architecture and a set of simple instructions that could be executed in a single machine cycle—making the resulting machine significantly more efficient than possible with other, more complex computer designs," - John Cocke, 1987.
- John Cocke through research concluded that 20% of instructions in a computer performed 80% of the work.
- By removing seldom used instructions they planned create a simple set of instructions that could execute in a single cycle which would increase efficiency.

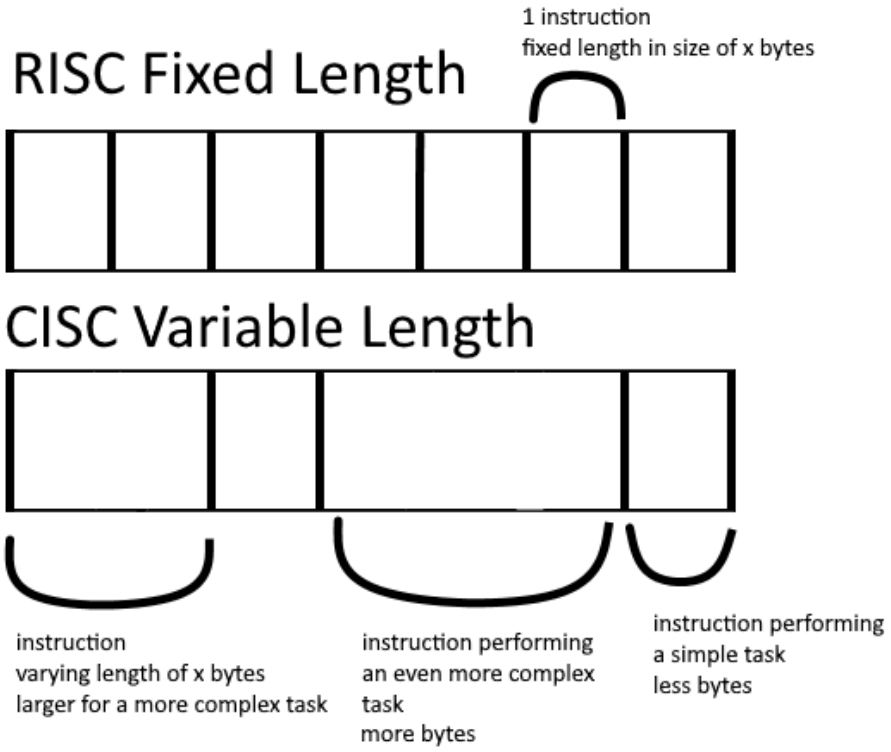
CISC

- Complex Instruction Set Computer.
- It refers to any computer designed with a full set of computer instructions
- While Cocke did not work on CISC, it was the norm architecture before RISC was developed and the pair are often compared.
- The name was created in contrast to RISC.
- Commands were long and powerful which used fewer individual instructions to perform complex tasks
- Commonly used in Intel CPUs

RISC and CISC

- RISCs shorter commands which required more individual instructions but allowed for less cycles is a direct contrast to the CISC design.
- CISC has more emphasis on hardware centric design in comparison to RISC being in favour of software.
- RISC using much more RAM which can cause bottlenecking issues while CISC is more efficient.
- RISC having only one layer of instructions while CISC can support microcode.

RISC and CISC



RISC and CISC in Modern Days

- In modern day computing, RISC and CISC are very similar and have adopted several of each others features causing them to have few differences compared to when RISC was originally created.
- These include RISC architectures often containing variable length instructions along with containing microcode and multi cycle instructions.
- RISC and CISC are now used as umbrella terms to describe groups of architectures which each use its main features but with features from the opposite architecture.

Modern Day RISC

- Used in high end applications such as video/image processing and telecommunications.
- A13 Bionic(iPhone 11 model) and the A12X Bixonic(iPad Pro) systems use ARM architecture which is a family of RISC architectures.
- Summit Supercomputer which was created by IBM used in Oak Ridge National Laboratory uses
- IBM Power Instruction Set Architecture which is based upon RISC
- Super-computer Fugaku(one of the worlds fastest computers)
- The NASA path finder utilises a Radiation Hardened IBM Risc 6000 Single Chip(Rad06000 SC) CPU

Achievements

- BSE in Mechanical Engineering 1945 - Duke University
- PHD in Mathematics 1956 - Duke University
- 1991 National Medal of Technology for "his development and implementation of Reduced Instruction Set Computer architecture that significantly increased the speed and efficiency of computers, thereby enhancing US technological competitiveness.“
- In 2002, he was made a Fellow of the Computer History Museum "for his development and implementation of reduced instruction set computer architecture and program optimization technology."

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[13] CISC

[14] RISC and CISC

[15] RISC Concept

[16] Achievements