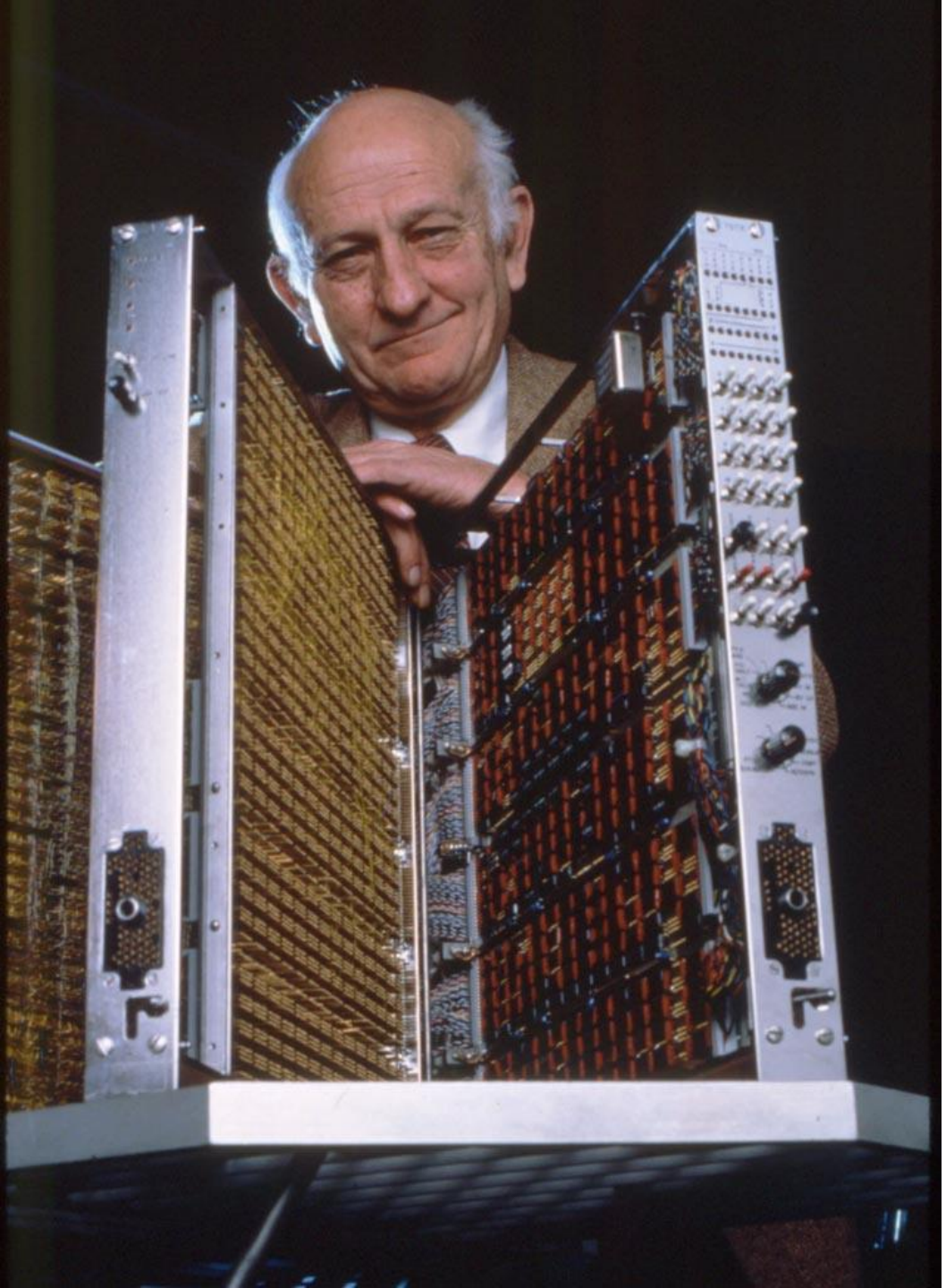

John Cocke

RISC ARCHITECTURE

COMPILER OPTIMIZATION

Introduction

In the early 1970s, John Cocke transformed computing by simplifying the set of instructions that tell computers which functions to perform.

Cocke was the Turing award winner of 1987. Cocke won this award for his significant contributions in the design and theory of compilers, the architecture of large systems and the development of Computers RISC for discovering and systematizing many fundamental transformations now used in optimizing compilers including the reduction of:

- Operator Strength
- Elimination of Common Subexpressions
- Register Allocation
- Constraint Propagation
- Dead Code Elimination

RISC Architecture

- Reduced Instruction Set Computers.
- The main idea behind this architecture was to make simpler hardware by using a reduced instruction set composed by a few basic step for loading evaluating and storing operations.
- Although this is a reduced instruction set this approach tries to increase the CPU performance.
- Reduce the cycles per instruction at the cost of the number of instructions per program.

Characteristic of RISC

- Relatively few instructions
- One word instructions
- Instruction take a single clock cycle to get executed
- More number of general purpose register
- Simple Addressing Modes
- Less Data types
- Pipeline can be achieved

Pipelining

- Pipelining a standard feature in RISC processors, is much like an assembly line because the processor works on different steps of the instruction at the same time, more instructions can be executed in a shorter period of time.
- Pipelining is a technique of decomposing a sequential process into sub-processes, with each sub-process being executed in a special dedicated segment that operates concurrently with all other segments
- Any operation that can be composed into a sequence of a sub-operation of about the same complexity can be implemented by a pipeline processor

RISC Projects

John Cocke was involved in three RISC projects:

- IBM 801 machine (1974)
- Berkeley's RISC-I and RISC-II processors (1980)
- Stanford's MIPS processor (1981)

IBM 801 machine

- IBM designed an experimental minicomputer named the 801.
- In the early-mid 1970s, IBM were interested in the possibility of constructing a telephone switch to handle a million calls per hour.
- 6 MIPS processor.
- Thomas J. Watson Research Center.
- IBM used the resulting architecture in various roles out through to the 1980s.

Berkeley’s RISC-I processors

- Originally known as Gold
- VLSI design course
- ACM ISCA
- 44,500 transistors
- 31 instructions
- 78 32-bit registers

Berkeley’s RISC-II processors

- Blue design
- 138 registers
- 8 windows
- 16 registers each
- 10 globals
- RISC instruction set with only 39,000 transistors

Stanford’s MIPS processor

- Strong background in compilers
- Develop a processor
- MIPS processor implemented a smaller, simpler instruction set
- 32 registers
- 32 bits wide

References

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[6] Computer Organization | RISC and CISC

[7] IBM 801

[8] RISC I & RISC II

[9] MIPS

10 RISC Pipeline