Verification Interview questions

1. What is callback ?
2. What is factory pattern ?
3. Explain the difference between data types logic and reg and wire
4. What is the need of clocking blocks ?
5. What are the ways to avoid race condition between testbench and RTL using SystemVerilog?
6. Explain Event regions in SV.
7. What are the types of coverages available in SV ?
8. What is OOPS?
9. What is inheritance and polymorphism?
10. What is the need of virtual interfaces ?
11. Explain about the virtual task and methods .
12. What is the use of the abstract class?
13. What is the difference between mailbox and queue?
14. What data structure you used to build scoreboard
15. What are the advantages of linkedlist over the queue ?
16. How parallel case and full cases problems are avoided in SV
17. What is the difference between pure function and cordinary function ?
18. What is the difference between $random and $urandom?
19. What is scope randomization
20. List the predefined randomization methods.
21. What is the dfference between always_combo and always@(*)?
22. What is the use of packagess?
23. What is the use of $cast?
24. How to call the task which is defined in parent object into derived class ?
25. What is the difference between rand and randc?

26. What is $root?
27. What is $unit?
28. What are bi-directional constraints?
29. What is solve...before constraint ?
30. Without using randomize method or rand,generate an array of unique values?
31. Explain about pass by ref and pass by value?
32. What is the difference between bit[7:0] sig_1; and byte sig_2;
33. What is the difference between program block and module ?
34. What is final block ?
35. How to implement always block logic in program block ?
36. What is the difference between fork/joins, fork/join_none fork/join_any ?
37. What is the use of modports ?
38. Write a clock generator without using always block.
39. What is forward referencing and how to avoid this problem?
40. What is circular dependency and how to avoid this problem ?
41. What is cross coverage ?
42. Describe the difference between Code Coverage and Functional Coverage Which is more important and Why we need them
43. How to kill a process in fork/join?
44. Difference between Associative array and Dynamic array ?
45. Difference b/w Procedural and Concurrent Assertions?
46. What are the advantages of SystemVerilog DPI?
47. How to randomize dynamic arrays of objects?
48. What is randsequence and what is its use?
49. What is bin?
50. Why always block is not allowed in program block?
51. Which is best to use to model transaction? Struct or class ?
52. How SV is more random stable then Verilog?
53. Difference between assert and expect statements?
54. How to add a new processs with out disturbing the random number generator state ?

55. What is the need of alias in SV?
56. What is the need to implement explicitly a copy() method inside a transaction , when we can simple assign one object to other ?
57. How different is the implementation of a struct and union in SV.
58. What is "this"?
59. What is tagged union ?
60. What is "scope resolution operator"?
61. What is the difference between Verilog Parameterized Macros and SystemVerilog Parameterized Macros?
62. What is the difference between

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1. logic data_1;
2. var logic data_2;
3. wire logic data_3j;
4. bit data_4;
5. var bit data_5;
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63. What is the difference between bits and logic?
64. Write a Statemechine in SV styles.
65. What is the difference between $rose and posedge?
66. What is advantage of program block over clockcblock w.r.t race condition?
67. How to avoid the race condition between programblock ?
68. What is the difference between assumes and assert?
69. What is coverage driven verification?
70. What is layered architecture ?
71. What are the simulation phases in your verification environment?
72. How to pick a element which is in queue from random index?
73. What data structure is used to store data in your environment and why ?
74. What is casting? Explain about the various types of casting available in SV.
75. How to import all the items declared inside a package ?
76. Explain how the timescale unit and precision are taken when a module does not have any timescalerdeclaration in RTL?

77. What is streaming operator and what is its use?
78. What are void functions ?
79. How to make sure that a function argument passed has ref is not changed by the function?
80. What is the use of "extern"?
81. What is the difference between initial block and final block?
82. How to check weather a handles is holding object or not ?
83. How to disable multiple threads which are spawned by fork...join

----------**UVM**----------

84. What is the difference between uvm_component and uvm_object?

    OR

    We already have uvm_object, why do we need uvm_component which is actually derived class of uvm_object?
85. Why phasing is used? What are the different phases in uvm?
86. a) Which uvm phase is top - down , bottom – up & parallel?
    b) Why build phase is top – down & connect phase is bottom – up?
    c) Which phase is function & which phase is task?
87. How uvm phases gets initiated?
88. How test cases run from simulation command line?
89. Difference between module & class based TB?
90. What is UVM Test bench Architecture?
91. What is UVM active and passive agent?
92. What is difference b/w tlm analysis port/export and other non analysis port/export?
93. What is diff b/w uvm_tlm_fifo and uvm_tlm_analysis_fifo?
94. uvm_tlm_fifo and uvm_tlm_analysis_fifo have tlm port or export?
95. What are the different functions or method in uvm_tlm_fifo and uvm_tlm_analysis_fifo?
96. What Driver , Monitor and Sequencer Do?

97. How driver and sequencer connected?
98. How driver and sequences communicated via sequencer?
99. How sequences run?
100. How many types of driver implemented?
101. What is virtual sequencer?
102. What is virtual sequences?
103. What is uvm_config_db ? List all the static functions of uvm_config_db.
104. What are the syntax and different parameter of config_db set & get function?
105. What is difference between config_db & resource_db?
106. What is uvm factory? What is factory override?
107. What is difference b/w new() and create() ?
108. How instance and component overrides ?
109. What is difference between m_sequencer & p_sequencer?
110. How develop pipe line driver?
111. What is in-order and out-of-order scoreboard?
112. How monitor communicate through scoreboard or coverage?
113. How more than one monitor communicate through single scoreboard?
114. When you can use super.build or super.connect?
115. Why super.new is used in every uvm component?
116. What is uvm_root & uvm_void?
117. What is difference b/w pre_body and pre_do,mid_do,post_do?
118. What is difference b/w IP and SOC level verification?
119. How Intrrupts are handled in SOC?
120. How Async Reset or System Reset was handle in UVM?
121. What is sequence layering?
122. What is verbosity and severity level in UVM?
123. How Error Injection Done in UVM? Or Erroneous Test cases?
124. Why phase objection is used? Or END of test mechanism in UVM?