Course Code	Course Name	L	T	P	C
VEC316	SoC DESIGN AND VERIFICATION	2	0	2	3

Category: Professional Elective

a. Preamble

This course promotes students to gain the fundamentals of SoC Design and verification to obtain knowledge to model, design, simulate, test and implement electronic systems.

b. Course Outcome (for Theory)

After successful completion of the course, the students will be able to

CO. No.	Course Outcome	Knowledge Level
CO1	Explore the use of System Verilog to create correct, efficient, and re-usable models for digital designs.	K2
CO2	Construct system Verilog to create testbenches for digital designs.	K2
CO3	Interpret new constructs in System Verilog for verification.	K2
CO4	Illustrate the communication between modules.	K2
CO5	Realize a complete system model using Verilog.	K3

Course Outcome (for Laboratory)

After successful completion of the course, the students will be able to

CO. No.	Course Outcome	Knowledge Level
CO1	Design and verify various digital logic modules.	K3
CO2	Construct and implement mailbox by allocating memory.	K3
CO3	Make use of Coverage & Assertion techniques for Verification of DUT.	K3
CO4	Create testbenches for digital device under test.	K3
CO5	Design a complete system model using System Verilog.	K3

c. Course Syllabus (for Theory) **Total : 30 Periods**

SoC & VERIFICATION METHODOLOGY **6**

System on Chip (SoC) – Architecture – Design Flow and Methodologies - Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained - Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench.

SYSTEM VERILOG BASICS AND CONCEPTS **6**

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with Typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings. Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions.

OBJECT ORIENTED PROGRAMMING (OOPS) IN SYSTEMVERILOG **6**

Introduction - Where to Define a Class - OOPS Terminology - Creating New Objects - Object Deallocation - Using Objects - Static Variables Vs. Global Variables - Class Routines - Defining Routines Outside of The Class - Scoping Rules - Using One Class Inside Another - Understanding Dynamic Objects -Copying Objects -Public Vs. Private -Straying Off Course - Building a Testbench.

THREADS AND INTER-PROCESS COMMUNICATION AND FUNCTIONAL COVERAGE **6**

Working with Threads, Inter-Process Communication, Events, Semaphores, Mailboxes, Building a Test bench with Threads and IPC. Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analysing Coverage Data, Measuring Coverage Statistics.

COMPLETE DESIGN MODEL USING SYSTEM VERILOG - CASE STUDY **6**

System Verilog ATM Example, Data Abstraction, Interface Encapsulation, Receivers and Transmitters, Test Bench for ATM.

Course Syllabus (for Laboratory) **Total : 30 Periods**

LIST OF EXPERIMENTS

1. Design a Testbench for 2x1 Mux Using Gates
2. Implementation of a Mailbox by Allocating Memory
3. Implementation and Testing of Semaphore for a Simple DUT
4. Implementation of Scoreboard for a Simple DUT

d. Activities

Students shall be given mini project on Complete design model using System Verilog.

e. Learning Resources (for both Theory and Laboratory)

Text Books

1. Chris Spears., 2006. *System Verilog for Verification - a Guide to Learning The Testbench Language Features*, 2nd Edition, Springer.
2. Bergeron, J., 2012. *Writing testbenches: functional verification of HDL models*. Springer Science & Business Media.

References

1. Vijayaraghavan, S. and Ramanathan, M., 2005. *A practical guide for SystemVerilog assertions*. Springer Science & Business Media.
2. Bergeron, J., 2007. *Writing testbenches using SystemVerilog*. Springer Science & Business Media.
3. Stojcev, M., 2006. System Verilog for Design: A Guide to Using System Verilog for Hardware Design and Modeling Hardcover, S. Sutherland, S. Davidman, P. Flake, Kluwer Academic Publishers, Norwell, MA (2004), pp. 374, plus XXVIII, euro 119, ISBN: 1-4020-7530-8.

LIST OF EQUIPMENT FOR A BATCH OF 30 STUDENTS:

S.No.	Description of Equipment	Quantity Required
1.	PCs with Icarus Verilog / Verilator / Xilinx Vivado or any other Equivalent software	15 Nos