Johnson Amalraj
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## CAREER OBJECTIVE

Experienced VLSI Design & Verification Engineer with a proven record of accomplishment of success in designing and verifying complex integrated circuits. With over 7 years of industry experience, I am seeking a challenging role in an innovative semiconductor company where I can apply my ability in VIP development and SOC verification by advanced verification methodologies. Skilled in developing efficient testbenches, executing functional and formal verification, and ensuring compliance with industry standards. Committed to delivering high-quality designs and collaborating effectively with cross-functional teams to achieve project goals.

## SUMMARY OF EXPERIENCE

- Working as ASIC Design Verification Engineer for 7 Years.
- Hands on experience in developing Verification IP using SV and UVM from Scratch.
- Having good understanding in Verification flow with System Verilog and UVM.
- Experience in developing test plan, writing test cases and development of testbenches using SV and UVM.
- Having good understanding and experience in Verification based on the functional coverage and assertion.
- Having ability to work as a team to achieve targets.
- Having good debug knowledge in FPGA/ASIC Verification environment.
- Having sound knowledge in Retimer (based on PCIe Protocol), LPDDR's, DDR's, JTAG, SPI and MIPI A-PHY protocols.
- Having basic knowledge in MIPI MPHY protocol.

## PROFESSIONAL EXPERIENCE

- **VLSI Technical Lead** at **Wipro Limited,** Bengaluru from 05-May-2021 – Present
- **Verification Engineer** at **SmartDV Technologies India Private Limited,** Bengaluru from 02-Jan-2017 to 04-May-2021
- **Internship** as **Trainee Verification Engineer** at **SmartDV Technologies India Private Limited,** Bengaluru from 01-Sep-2016 to 31-Dec-2016.

## TECHNICAL SKILLS

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| **Programming languages** | System Verilog, Verilog, C |
| **Methodology** | Universal Verification Methodology |
| **Simulation Tool** | Cadence NC, Questa, Synopsys VCS |
| **Script languages** | Perl, Python |
| **Version Control** | SVN, Git |
| **Bug Management** | Mantis, Redmine |
| **Operation System** | Windows, Linux, Mac |

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**PROJECT EXPERIENCE**

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| **PROJECT NAME** | CASTOR32G<br>(EM4 Core CPU verification along with Retimer PCIe based protocol, SPI and JTAG) |
| **ROLE** | VLSI Technical Lead B3 - WIPRO |
| **TEAM SIZE** | 24 |
| **DURATION** | 2Years 4 Months (as of Sep 2023) (Currently working) |
| **CLIENT** | Kandou Bus |

**Accomplishments:**

- Verified the EM4 Core CPU instructions, C-SV & SV-C handshake mechanism, all IP interrupt mechanism.
- Verified the register access of all interconnected IPs with CPU instructions.
- Verified the T2T SPI with CPU instructions and write read operations for multi tile and single tile configurations.
- Verified the T2T access and JTAG Daisy chain connections.
- Verified the JTAG with CPU instructions and verified the debug mode operations with JTAG for all interconnected IPs.
- Developed the C test cases for the SPI and JTAG register access.
- Added the coverage support for both SPI and JTAG access by CPU.
- Verified the Retimer features connected in between PCIe based RC and EP VIP.
- Responsible for the Retimer IP Verification at Block and Full Chip level.
- Verified the interrupts and retimer features on both Block and Full chip levels.
- Verified the Avery compliance test cases for RPCS DUT.
- Verified the RPCS registers through the EM4 CORE.
- Debugged and reported critical bugs in JTAG and RPCS.
- Verified the different scenarios like JTAG and SPI as Master.
- Having good understanding of customer requirement and done the test bench updates.
- Developed testbenches and test cases to verify the features of JTAG, T2T SPI and Retimer.
- Verified the RTL registers set for Retimer, JTAG and T2T SPI.
- Developed the test plan for the Retimer Verification.
- Developed the Coverage and assertion environment as a part of verification.
- Worked with team members and guiding them for their debugs and queries.
- Worked on the multiple phases of test bench releases.

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| **PROJECT NAME** | LPDDR5 |
| **ROLE** | Verification Engineer - SmartDV |
| **TEAM SIZE** | 5 |
| **DURATION** | 12 Months |
| **CLIENT** | Invecas, Sankalpsemi |

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**Accomplishments:**

- Developed the LPDDR5 Verification IP test bench from scratch.
- Added the major supports like write, read, refresh and power down.
- Added the timing checks and test cases related to timing checks.
- Added the support for mode registers.
- Added the trainings like WCK2CK training and command bus training.
- Added the Write-X and RDQS support.
- Added the burst sequences support for different commands.
- Added the support for initialization process.
- Worked in various latency types.
- Debugged customer related queries and adding support for their requirements.

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| **PROJECT NAME** | LPDDR4 |
| **ROLE** | Verification Engineer - SmartDV |
| **TEAM SIZE** | 5 |
| **DURATION** | 12 Months |
| **CLIENT** | Invecas, Qualcomm, Sankalpsemi |

**Accomplishments:**

- Verified the supports like initialization, write levelling and command bus training.
- Added the test cases to improve the functional coverage.
- Worked in dual channel memory and added test cases to verify the supports.
- Verified the command set operation for CAS_2.
- Worked in LPDDR4Y, LPDDR4C and LPDDR4X supports.
- Verified the data mask and data bus inversion supports.
- Worked in different burst length commands.
- Worked with customers to clarify their queries and requirements.

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| **PROJECT NAME** | MIPI A-PHY |
| **ROLE** | Senior Verification Engineer - SmartDV |
| **TEAM SIZE** | 4 |
| **DURATION** | 8 Months |
| **CLIENT** | Product Development |

**Accomplishments:**

- Developed the A-PHY Verification IP test bench from scratch.
- Added the linkup and link down support.
- Added the protocol checks related to timings and serial interface.
- Added the checker related to source and sink transactions.
- Added the callback and functional coverage support.

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- Having knowledge in ACMD registers.
- Added test bench and test cases to verify all functionalities.

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| **PROJECT NAME** | DDR4, DDR3 |
| **ROLE** | Verification Engineer - SmartDV |
| **TEAM SIZE** | 4 |
| **DURATION** | 6 Months |
| **CLIENT** | Product Development |

**Accomplishments:**

- Verified all major supports as per specification.
- Verified the Denali DDR's model with our own developed code.
- Worked in functional coverage to improve.
- Developed test plan and added test cases to verify all functionalities.

**HONORS AND AWARDS**

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| **Award Name** | League of superheroes |
| **Organization & Project** | WIPRO - CASTO32G |
| **Description** | Awarded 3 times for Exemplary Contribution to the project |

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| **Award Name** | 3 Cheers |
| **Organization & Project** | WIPRO - CASTOR32G |
| **Description** | Awarded 3 times for the good interactions with Customers |

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| **Award Name** | Best Employee of Month |
| **Organization & Project** | SmartDV - LPDDR5 |
| **Description** | Awarded 2 times for the commitment's accomplishment |

**ACADEMIC QUALIFICATION**

- **BE** in **Electronics and Communication Engineering** studied at Kamaraj College of Engineering and Technology (2012-2016), Virudhunagar with CGPA of 7.7.
- **HSC (+2)** studied at Nadar Higher Secondary School (2012), Kovilpatti with an overall aggregate of 90.9%.
- **SSLC (10$^{th}$)** studied at E.V.A Vallimuthu High School (2010), Kovilpatti with an overall aggregate of 92.2%.