Pre-Lab 3

ALU_demo

KEY[2:0]

key and select matching bitwise

HEX_decoder
H0

SW[3:0]   HEX
           [6:0]

HEXD
- displays B

select[2:0]

ALU m0

SW[7:4] A[3:0]

fbrca a1

A   S
4'b0001 B
1'b0   Cin   cout

4

3

HEX_decoder
H1

4'b0   4   SW   HEX
             [3:0] [6:0]

7

HEX1[6:0]

HEX1[6:0] must be
equivalent to
7'b1000000
thus displaying 0

SW[3:0] B[3:0]

fbrca a2

A   S
B
1'b0   Cin   cout

4

B

HEX_decoder
H2

4   SW[3:0]   HEX
               [6:0]

select
[2:0]

000

HEX 2
- displays A

001

A+B using verilog
code

8

010

HEX_decoder
H3

4'b0   4   SW[3:0]   HEX
                      [6:0]

7

HEX3 [6:0]

HEX3[6:0] must be
equivalent to
7'b1000000
thus displaying O

ALUout

B

ALUout

A XOR B for lower bits
A OR B for upper bits

8

011

1 if any of the bits are high
0 if none of the bits are high

8

100

A for most significant
B for least significant.

8

101

* The default value for
ALUout is 8'b00000000.

HEX_decoder
H4

ALUout [3:0]   4   SW[3:0]   HEX
                            [6:0]

HEX4
displays
ALUout [3:0]

HEX_decoder
H5

ALUout[7:4]   4   SW[3:0]   HEX
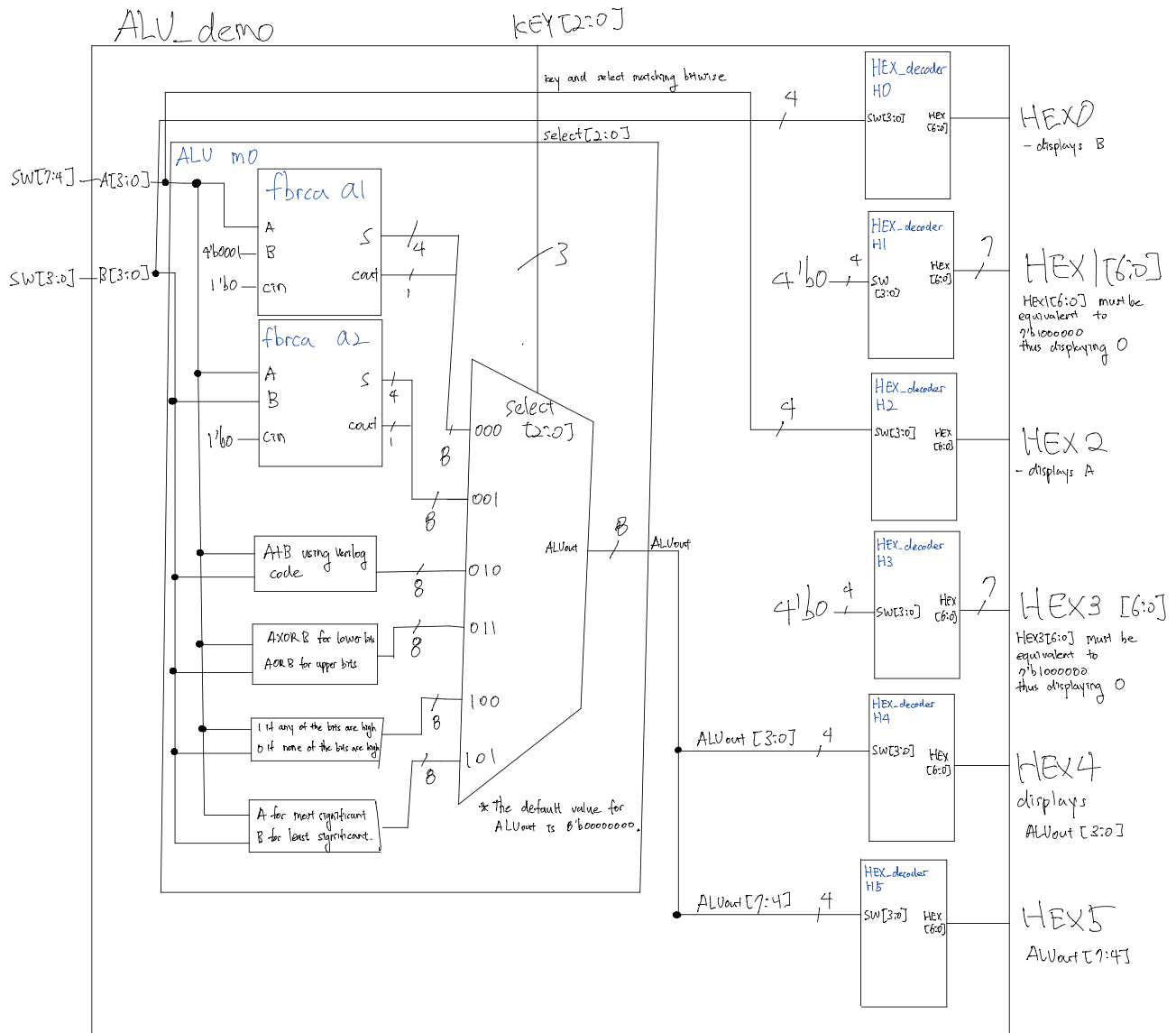   [6:0]

HEX5
ALUout [7:4]

- Note that fbrca = Four Bit Ripple Carry Adder.
- A, B matches to SW[7:4] and SW[3:0] bitwise respectively.