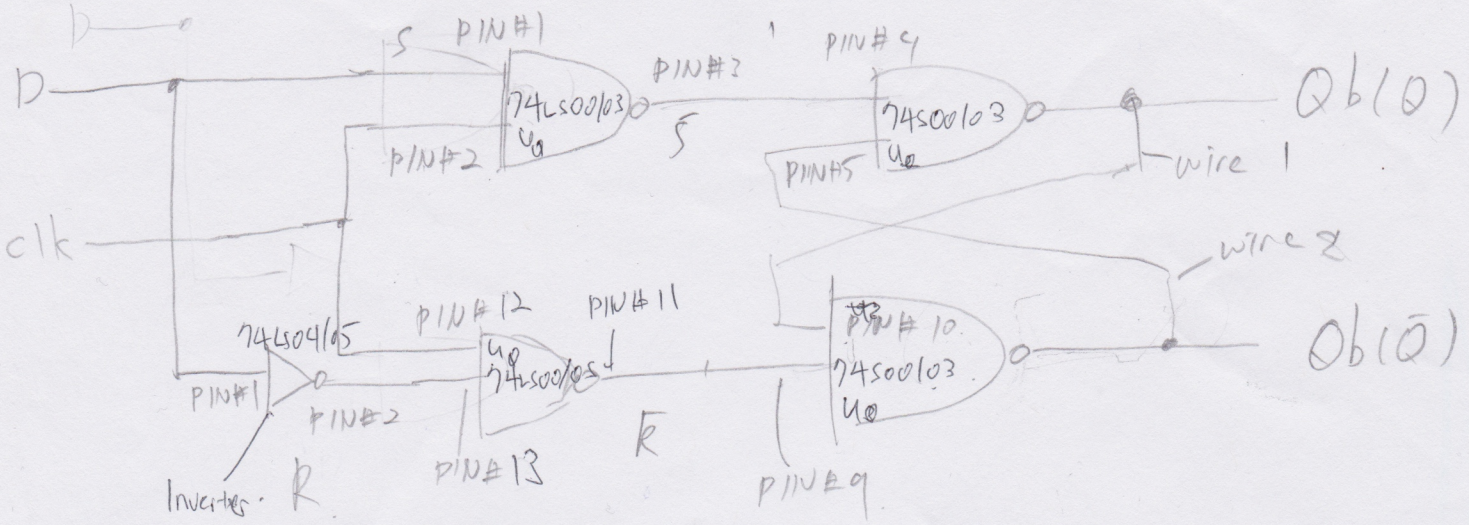
Pre-lab Part 1.



clk	D	Q_{n+1}	
0	x	Q_n	
1	0	0	→ S=0 R=1
1	1	1	→ S=1 R=0.

↳ This can be accomplished by one NAND gate and one NOT gate.

4. we know from SR latches that, SR latches have outputs that are different only when S and R are complement to each other.
Therefore, D-latches are born to arbitrarily make SR inputs to be different.
Furthermore, when clk is first set to 0 both $\bar{S}$ and $\bar{R}$ will be 1. Then, after, both outputs enter NAND gates for each, the result of NAND gates will be
Once the wires are set to 0 → Q(Q) and Qb($\bar{Q}$) are fixed regardless of the value of D.
Therefore, not the first to be tested.