- Chapter 6:
- Analogue-to-Digital Converters and Digital-to-Analogue Converters

Analogue-to-digital converters and Digital-to-Analogue converters

- Problems:

  Analogue signals cannot be interfaced directly to a digital system like a microprocessor or a PC.

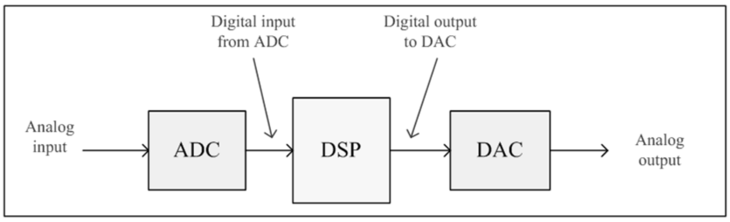
  Similarly, digital signals cannot be interfaced directly to an analogue system.

- Solutions:

  To solve this problem we need some means to convert and analogue signal to a digital signal and vice versa.

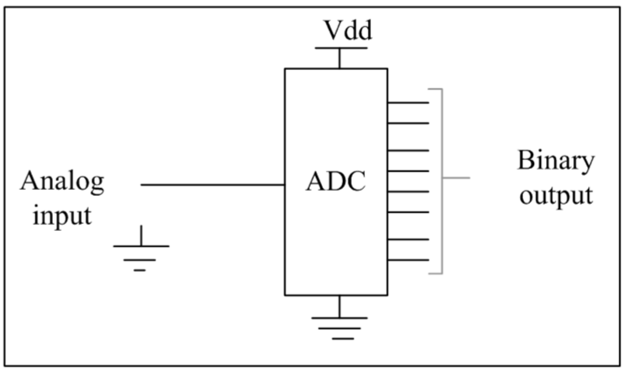
  These are achieved by using Analogue to Digital Converters (ADC) and Digital to Analogue Converters (DAC)

DSP System



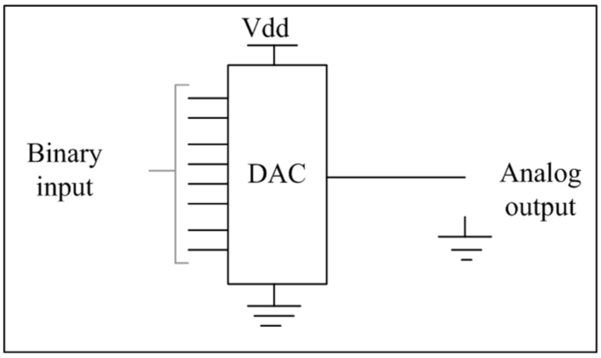
Analogue to Digital and Digital to Analogue conversions 3

Analogue to Digital Converter



Analogue to Digital and Digital to Analogue conversions 4

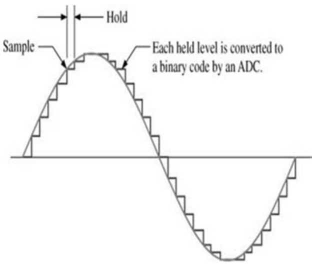
Digital to Analogue Converter



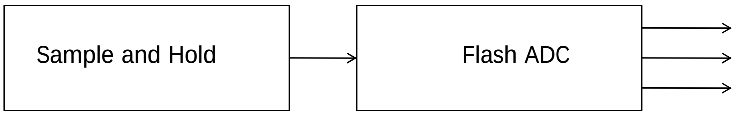
Part 1: Analogue to digital converters

- Flash ADC
- Digital Ramp ADC
- Successive Approximation ADC

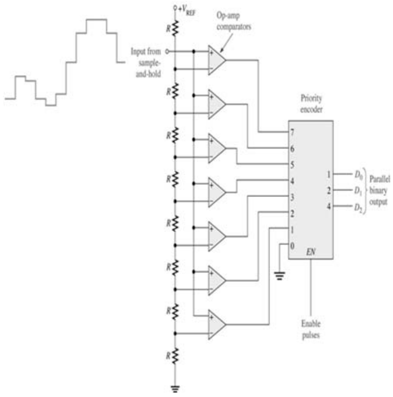
Flash ADC



Flash ADC also known as Parallel ADC



Flash ADC or Parallel ADC



Principle of operation: The input is compared to a set of reference voltages simultaneously

1. Fastest ADC
2. Consume a lot of power.
3. Low resolution

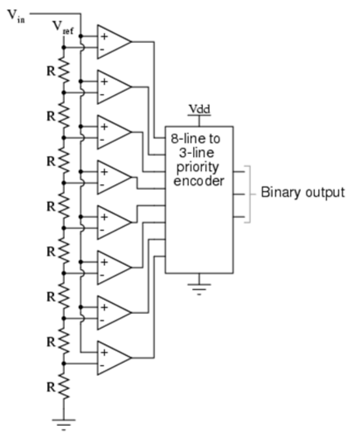
Priority encoder

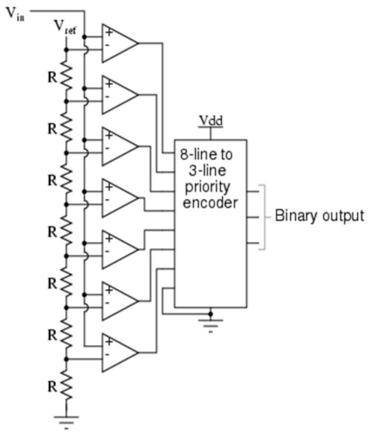
The true table for an 8 to 3-bit priority encoder.

X = don't care

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

Flash ADC or Parallel ADC



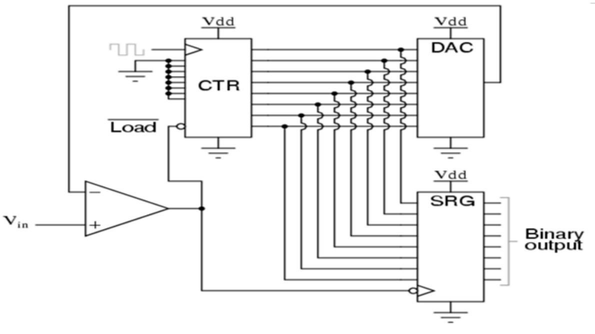


Flash ADC or Parallel ADC

Advantages	Disadvantages
■ Very fast	1. Needs many comparators. (8 comparators for 3-bit ADC) (255 comparators for 8-bit ADC) 2. Expensive 3. Large power consumption

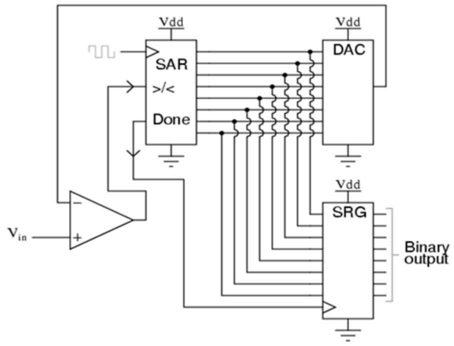
Digital Ramp ADC

The ADC is built from a DAC as DACs are easier to design



Successive Approximation ADC, SAR ADC

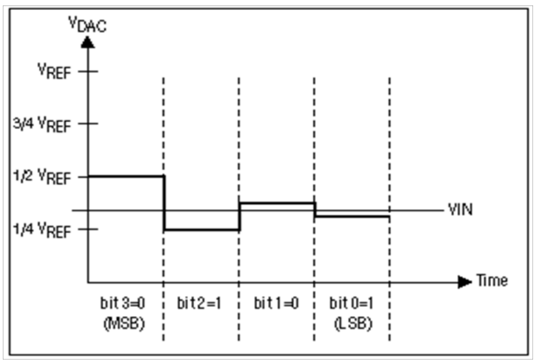
1. Improvement from the RAMP ADC.
2. The main difference is the improvement of the counter which is replaced by a successive approximation Register



Applications:

1. Medium-to-high-resolution applications.
2. SAR ADCs most commonly range in resolution from 8- to 16-bits and provide low power consumption as well as a small form factor

Operation of the SAR ADC



bit 3	bit 2	bit1	bit 0
0	0	0	0
0	1	0	0
0	1	0	0
0	1	0	1

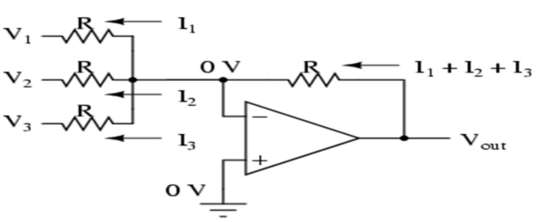
Note: the successive approximation ADC is much faster than the RAMP ADC, since the counter does not reset to zero for every conversion.

Part 2: Digital to Analogue converters

- R/2nR DAC
- PWM DAC

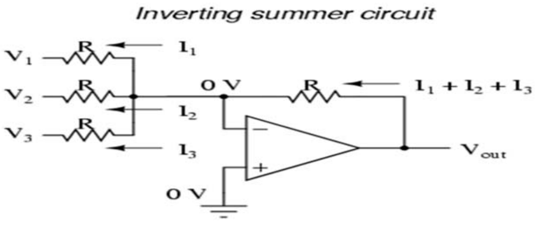
R/2nR DAC

Inverting summer circuit



$$V_{out} = -(V_1 + V_2 + V_3)$$

R/2nR DAC



$$V_{out} = -(V_1 + V_2 + V_3)$$

Eg:

If D1 = 1, D2 = 0, D3= 0 then Vout =-V

If D0 = 0, D2 = 1, D3= 0 then Vout =-V

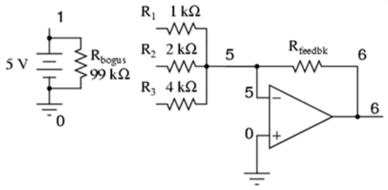
Therefore 100 or 010 or 001 give the same results.

Is this acceptable?

R/2nR DAC

- The solution is to modify the circuit as shown below:

Vout= - (D3 + D2/2 +D1/4) Vref



MSB LSB	Vout
000	0
001	-1/4
010	-2/4
011	-3/4
100	-1
101	-5/4
110	-6/4
111	-7/4

Note: The Resistors R should be very precise

- End of Chapter