



# *Digital System Design*

## **N16 ADFP Synthesis Guidelines**

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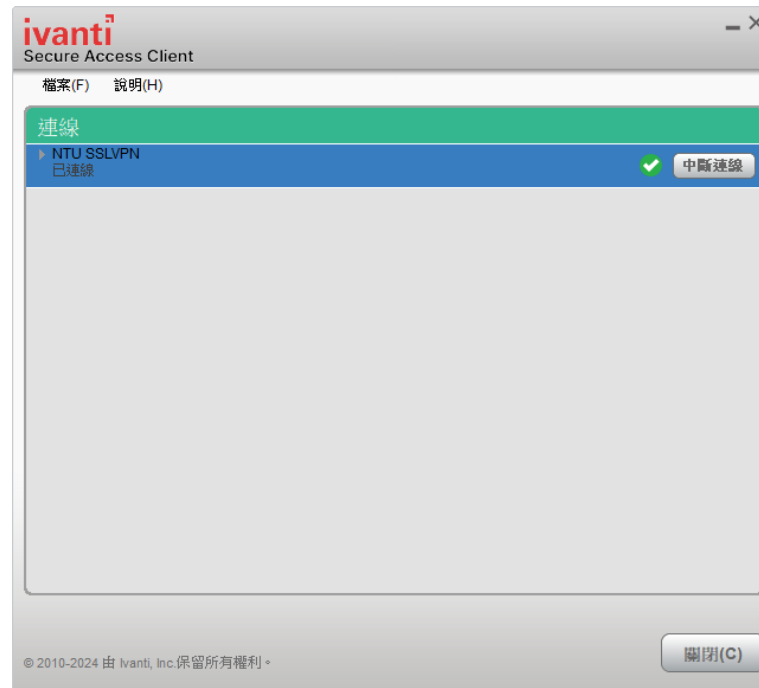
## Outline

- ❖ Workstation Connection
- ❖ Synthesis with N16 ADFP



## VPN

- ❖ Download Ivanti Secure Access Client and set up the connection to NTU VPN Server
- ❖ Follow the steps of [NTU SSL VPN Services](#)





## VPN

- ❖ Make sure you connect to NTU VPN while using ADFP workstation, **even if you are under the NTU network**



# Remote Desktop Connection

- ❖ Open browser and connect to 140.112.33.156
- ❖ Don't change the password



## 你的連線不是私人連線

攻擊者可能會嘗試從 140.112.33.156 竊取你的資訊 (例如密碼、郵件或信用卡資訊)。進一步瞭解這項警告

NET::ERR\_CERT\_AUTHORITY\_INVALID

💡 開啟強化防護，即可享有 Chrome 最強大的安全防護機制

隱藏詳細資料

返回安全網頁

伺服器無法證明其屬於 140.112.33.156 網域；其安全性憑證未取得你電腦作業系統的信任。這可能是因為設定錯誤，或有人篡改了你的連線所致。

繼續前往 140.112.33.156 網站 (不安全)



# Remote Desktop Connection

❖ Type “cb” to source the license

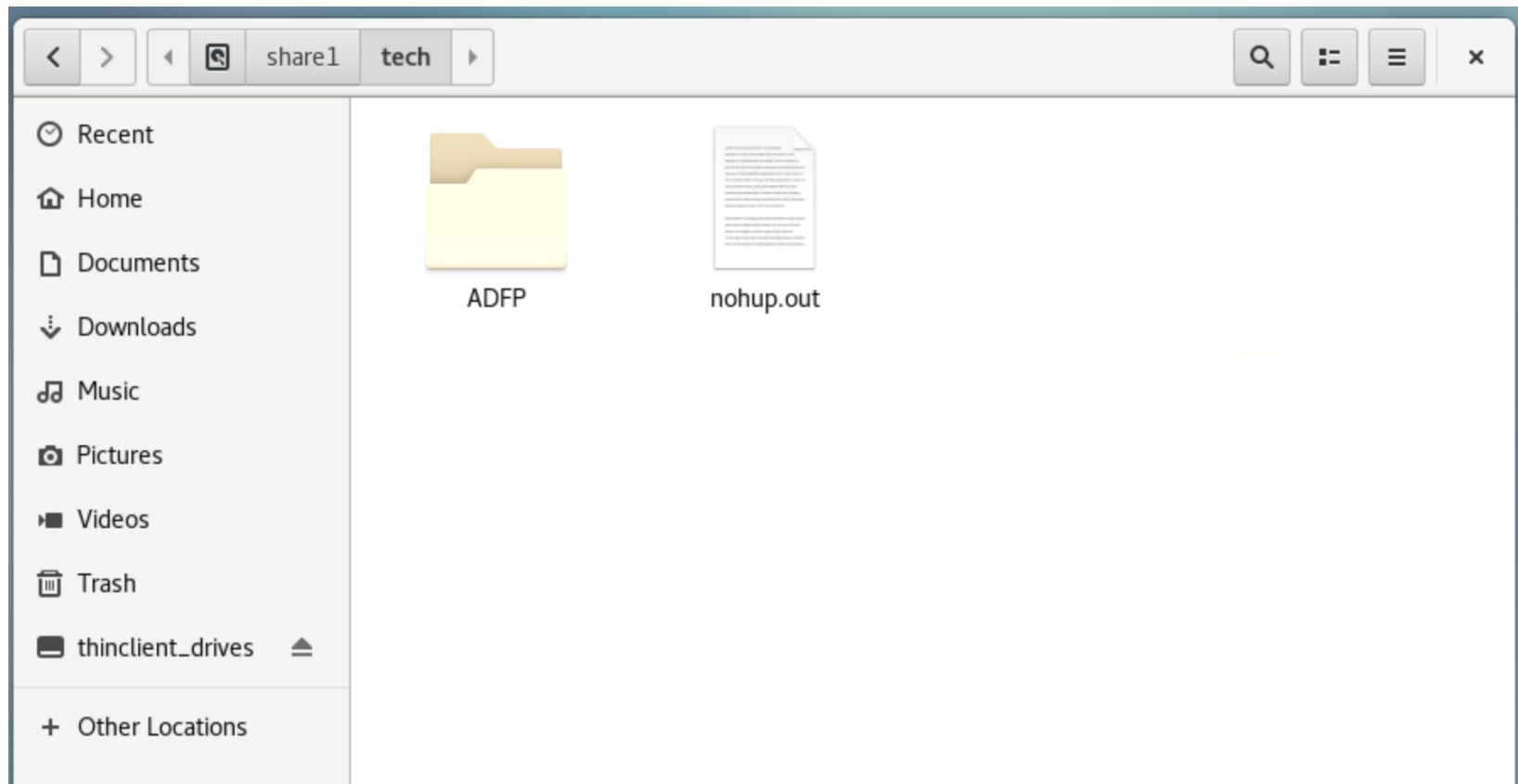
A screenshot of a terminal window titled 'dsd028@dsd-10:~'. The window has a menu bar with 'File', 'Edit', 'View', 'Search', 'Terminal', and 'Help'. The terminal content shows a list of available options for sourcing a license, followed by the execution of the 'cb' command and a series of version settings for various tools.

```
dsd028@dsd-10:~  
File Edit View Search Terminal Help  
=====   
= Available Options:   
= 1. Type [fc] for Full-Custom jobs   
= 2. Type [cb] for Cell-Based jobs   
=====   
[dsd028@dsd-10 ~]$ cb  
set INNOVUS version: INNOVUS_20.15.000/ (default)  
set ICADVM version: ICADVM_18.10.130/ (default)  
set PEGASUS version: PEGASUS_21.20.000/ (default)  
set QUANTUS version: QUANTUS_21.11.000/ (default)  
set SSV version: SSV_21.12.000/ (default)  
set SPECTRE version: SPECTRE_19.10.322/ (default)  
set synthesis version: 2022.12-sp6/ (default)  
set verdi version: 2022.06/ (default)  
set vcs version: 2022.06 (default)  
set lc version: 2022.12-sp6/ (default)  
set primetime version: 2019.03-sp5-1/ (default)  
set icc2 version: 2022.12-sp6/ (default)  
set icvalidator version: 2021.06-sp2/ (default)  
set star-rcxt version: 2019.12-sp5-3/ (default)  
set spyglass version: 2022.06/ (default)  
[dsd028@dsd-10 ~]$
```



## ADFP Library

❖ ADFP library: /share1/tech/ADFP





## Upload Files to Workstation

❖ Download and install [FileZilla](#)

### Quick download links

**Download  
FileZilla Client**

All platforms

**Download  
FileZilla Server**

All platforms

Pick the client if you want to transfer files. Get the server if you want to make files available for others.





# Setup the Site Manager

❖ Select File > site manager





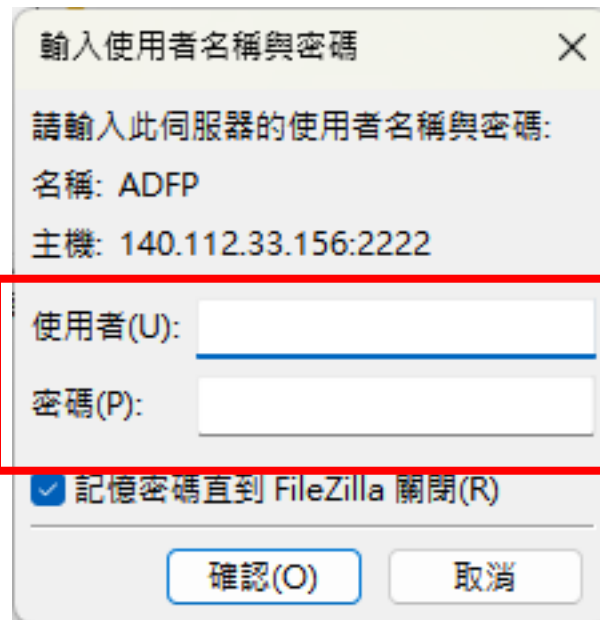
# Setup the Site Manager

❖ Create a new site named ADFP





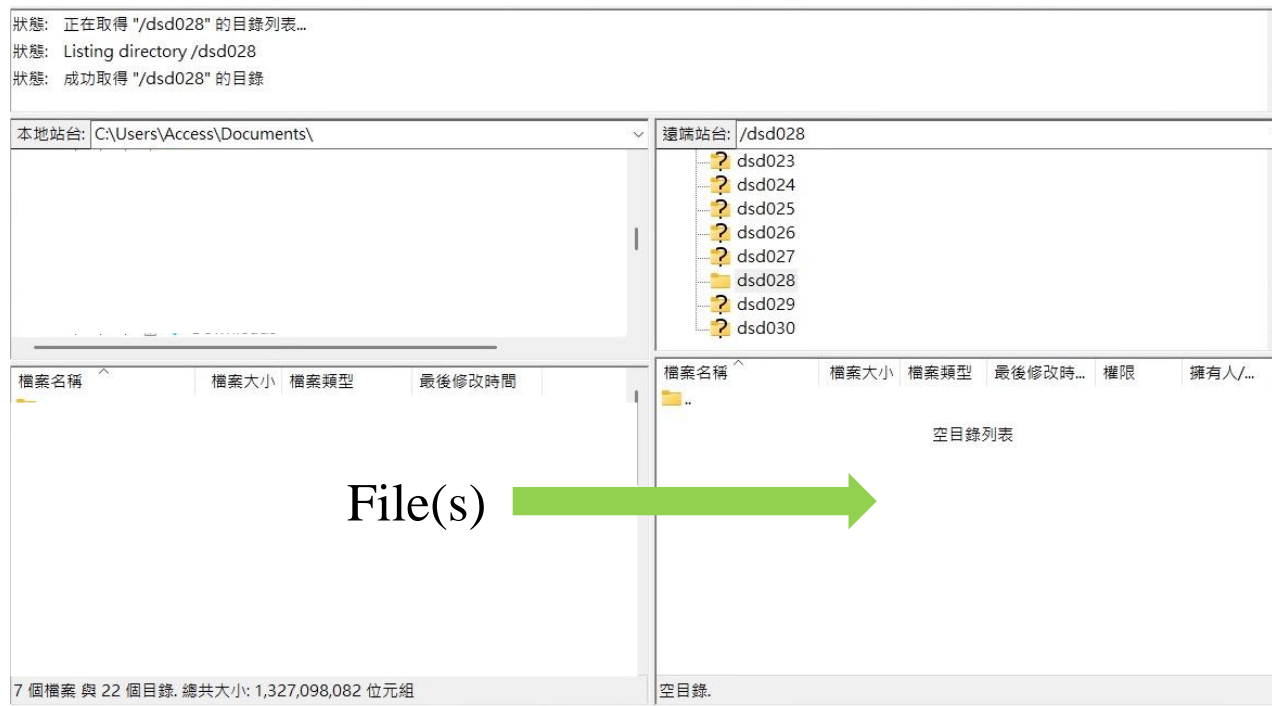
# Connect to the Site





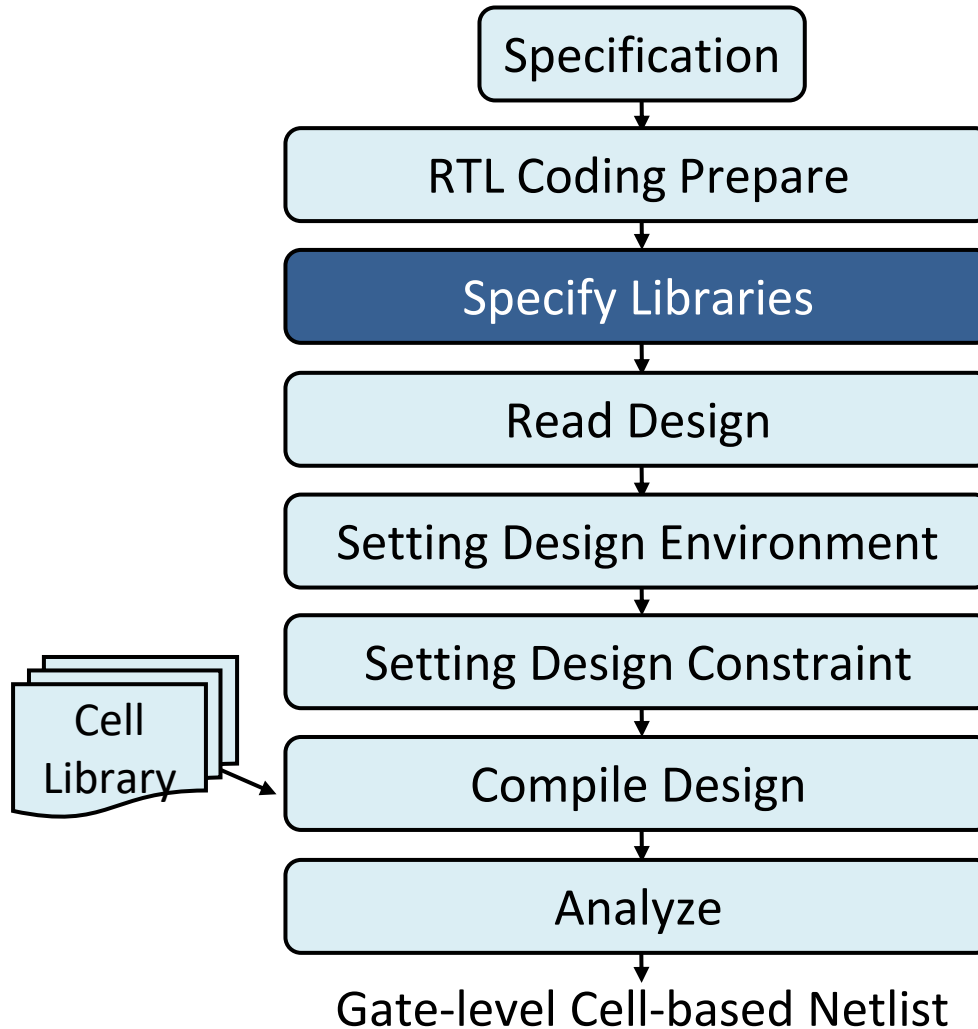
# Upload Files

- ❖ Drag the file(s) to the right-hand side
- ❖ `cp /homework/dsd/[dsd0xx]/[filename] ~/`





## Synthesis with ADFP





# Synthesis with ADFP

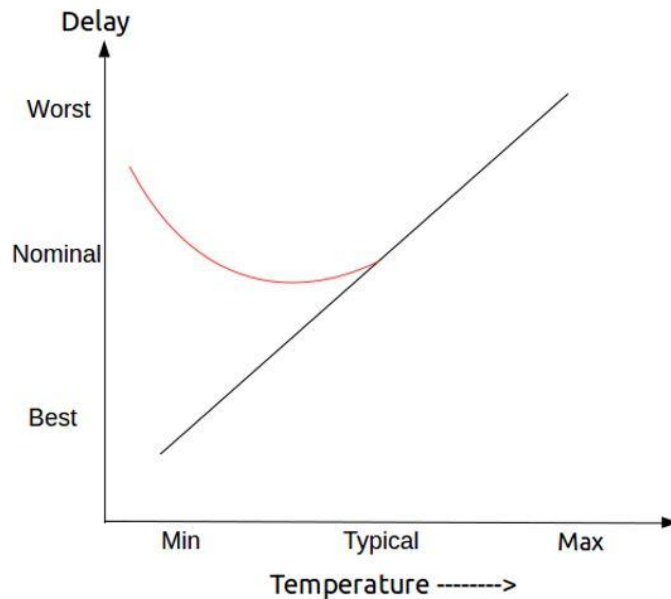
In 0.13 $\mu$ m: slow.db / fast.db

```
set target_library "N16ADFP_StdCellff0p88v125c_ccs.db \
N16ADFP_StdCellff0p88vm40c_ccs.db \
N16ADFP_StdCellss0p72v125c_ccs.db \
N16ADFP_StdCellss0p72vm40c_ccs.db \
N16ADFP_StdCelltt0p8v25c_ccs.db \
N16ADFP_StdIOff0p88v1p98v125c.db \
N16ADFP_StdIOff0p88v1p98vm40c.db \
N16ADFP_StdIOss0p72v1p62v125c.db \
N16ADFP_StdIOss0p72v1p62vm40c.db \
N16ADFP_StdIOtt0p8v1p8v25c.db \
N16ADFP_SRAM_ff0p88v0p88v125c_100a.db \
N16ADFP_SRAM_ff0p88v0p88vm40c_100a.db \
N16ADFP_SRAM_ss0p72v0p72v125c_100a.db \
N16ADFP_SRAM_ss0p72v0p72vm40c_100a.db \
N16ADFP_SRAM_tt0p8v0p8v25c_100a.db \
"
```



# Temperature Inversion

- ❖ In advanced technology, Cell delay increases in low temperature
- ❖ When T decrease, both  $\mu_n$  and  $V_t$  increase
- ❖  $V_{gs}$  is smaller in advanced technology



$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$$



# Design Environment

- ❖ Net delay provided by wire load model is not accurate
- ❖ No wire load model in ADFP

- 1 set\_input\_delay
- 2 set\_output\_delay
- 3 set\_drive
- 4 set\_load
- 5 set\_operating\_conditions
- 6 ~~set\_wire\_load\_model~~







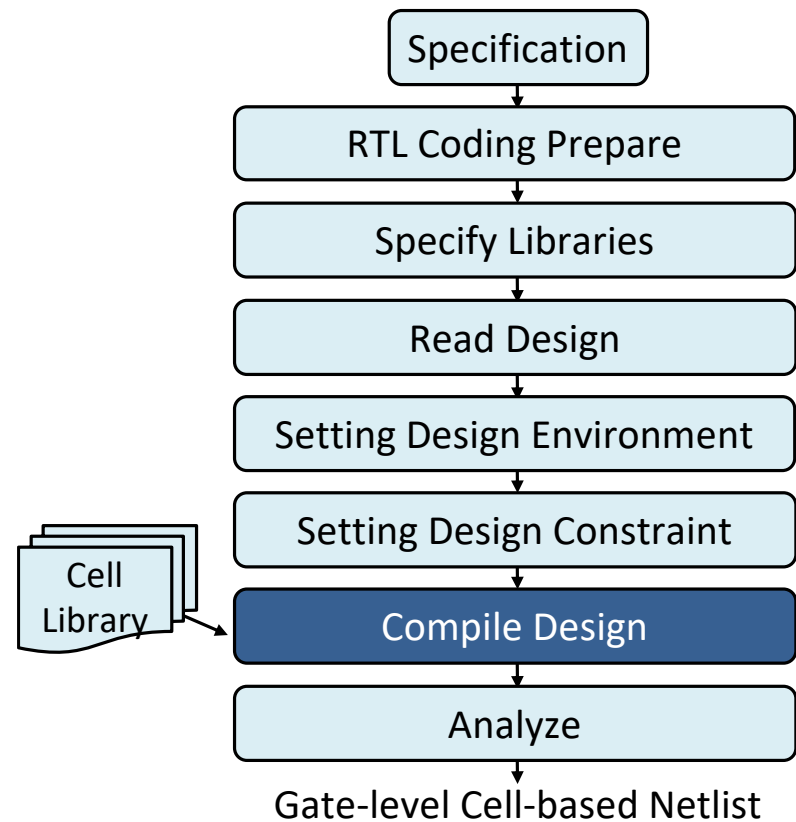
# Compile Design

- ❖ May still have hold time violations after compile\_ultra

compile\_ultra

+

compile -inc





# Compile Design

## ❖ No preset pin in ADFP register

```
always @(posedge clk or posedge rst) begin
    if (rst) begin
        in_a_buffer <= 1;
    end
    else begin
        in_a_buffer <= in_a_buffer_nxt;
    end
end
```

```
CRND1BWP10P90LVT U20 ( .I(13C_11), .ZN(1110) ),
\**FFGEN** in_a_buffer_reg_0_ ( .next_state(n9), .clocked_on(clk),
    .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
        net434), .Q(in_a_buffer[0]), .QN(n20) );
\**FFGEN** in_b_buffer_reg_0_ ( .next_state(in_b[0]), .clocked_on(clk),
    .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
        net434), .Q(in_b_buffer[0]) );
TIELBWP20P90LVT U33 ( .ZN(net434) );
```



## Compile Design

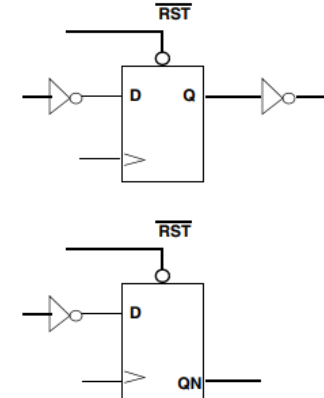
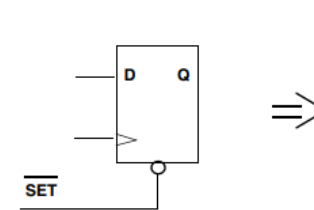
❖ Set the option or use compile\_ultra

set compile\_seqmap\_enable\_output\_inversion true

```
CRND1BWP10P90LVT U20 ( .I(13C_n), .ZN(n10) ),
\**FFGEN** in_a_buffer_reg_0_ ( .next_state(n9), .clocked_on(clk),
    .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
        net434), .Q(in_a_buffer[0]), .QN(n20) );
\**FFGEN** in_b_buffer_reg_0_ ( .next_state(in_b[0]), .clocked_on(clk),
    .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
        net434), .Q(in_b_buffer[0]) );
TIELBWP20P90LVT U33 ( .ZN(net434) );
```



```
DFCNQND1BWP16P90LVT out_reg_0_ ( .D(n1), .CP(clk), .CDN(n12), .Q(out[0]) ),
DFCNQND1BWP16P90LVT in_b_buffer_reg_0_ ( .D(n14), .CP(clk), .CDN(n12), .QN(
    in_b_buffer[0]) );
DFCNQND1BWP16P90LVT in_a_buffer_reg_0_ ( .D(n30), .CP(clk), .CDN(n12), .QN(
    in_a_buffer[0]) );
CKND1BWP16P90LVT U15 ( .I(enable), .ZN(n13) );
```





**Thanks! Feel free to  
ask me any  
questions!**

