Digital System Design

N16 ADFP Synthesis Guidelines

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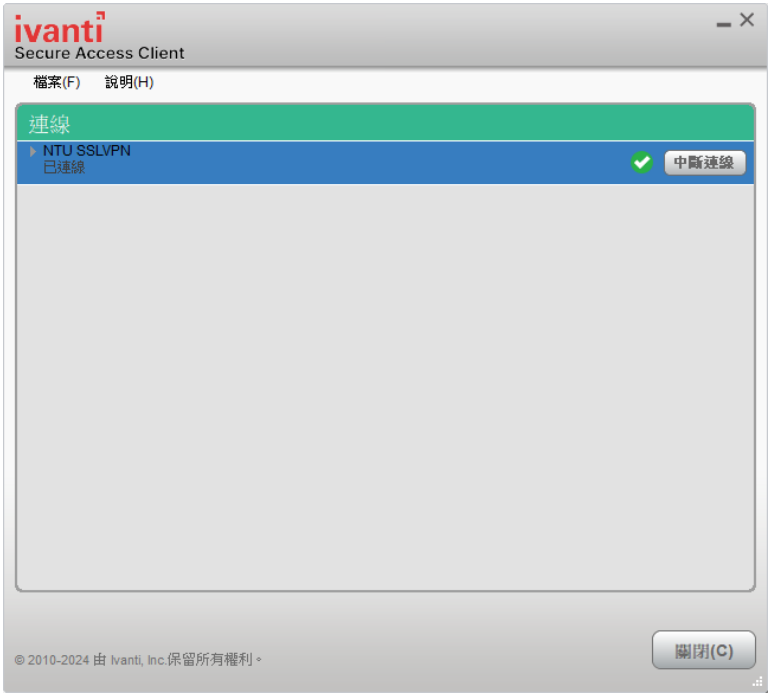
Outline

- Workstation Connection
- Synthesis with N16 ADFP

VPN

- Download Ivanti Secure Access Client and set up the connection to NTU VPN Server
- Follow the steps of NTU SSL VPN Services

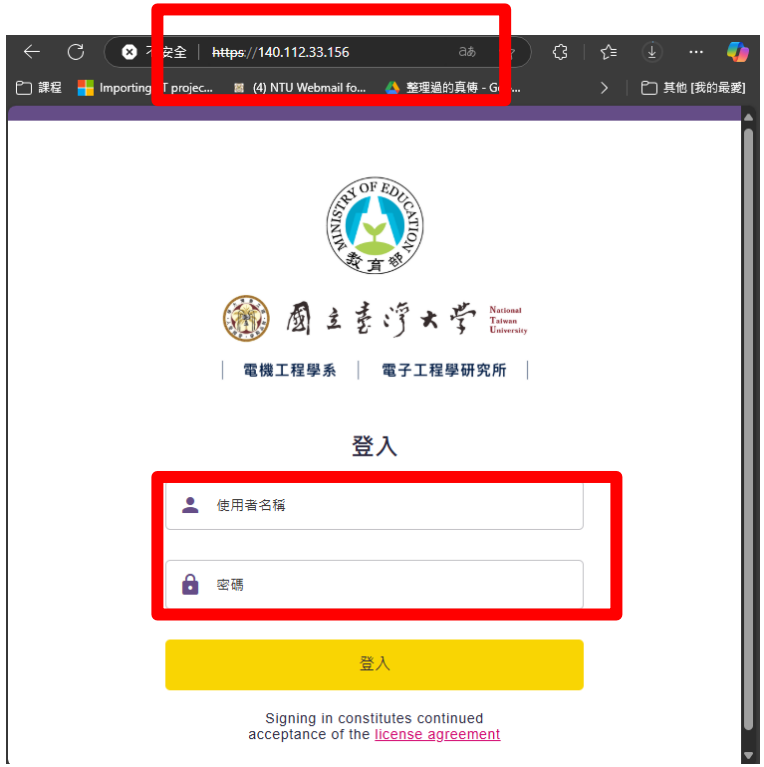


VPN

- Make sure you connect to NTU VPN while using ADFP workstation, **even if you are under the NTU network**

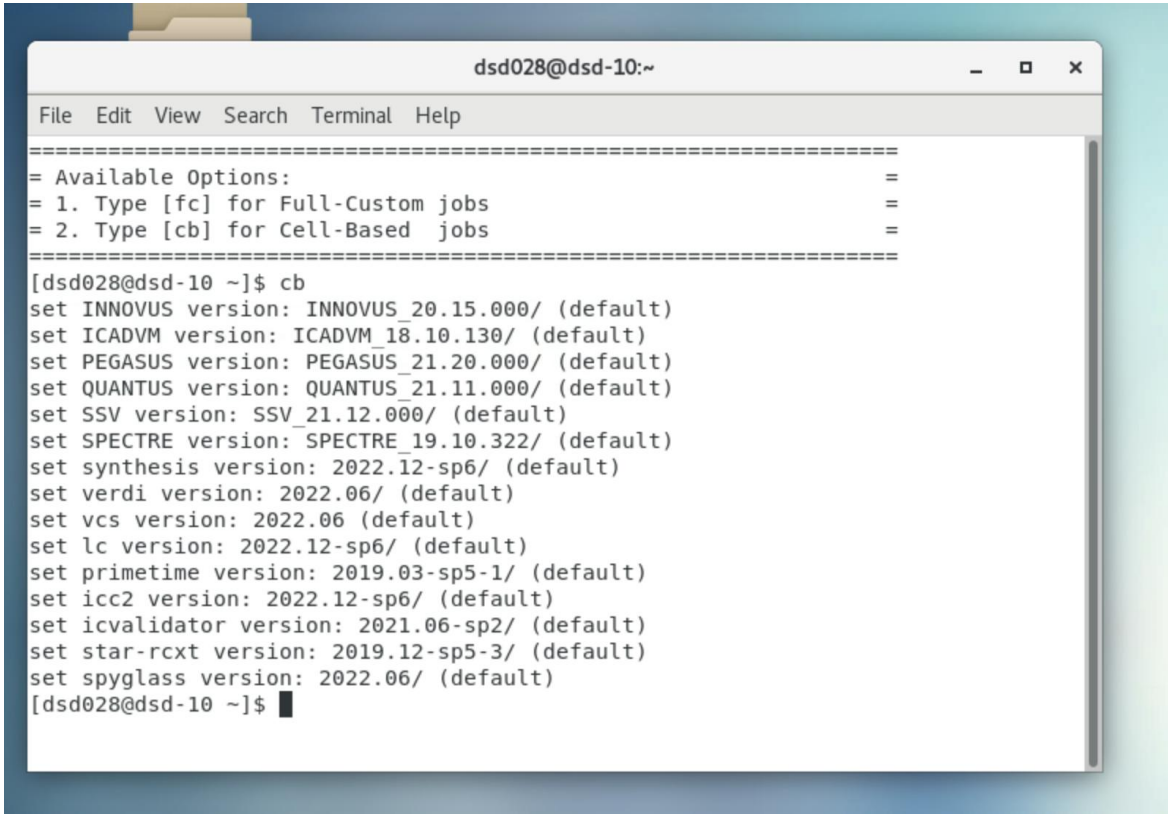
Remote Desktop Connection

- Open browser and connect to 140.112.33.156
- Don't change the password



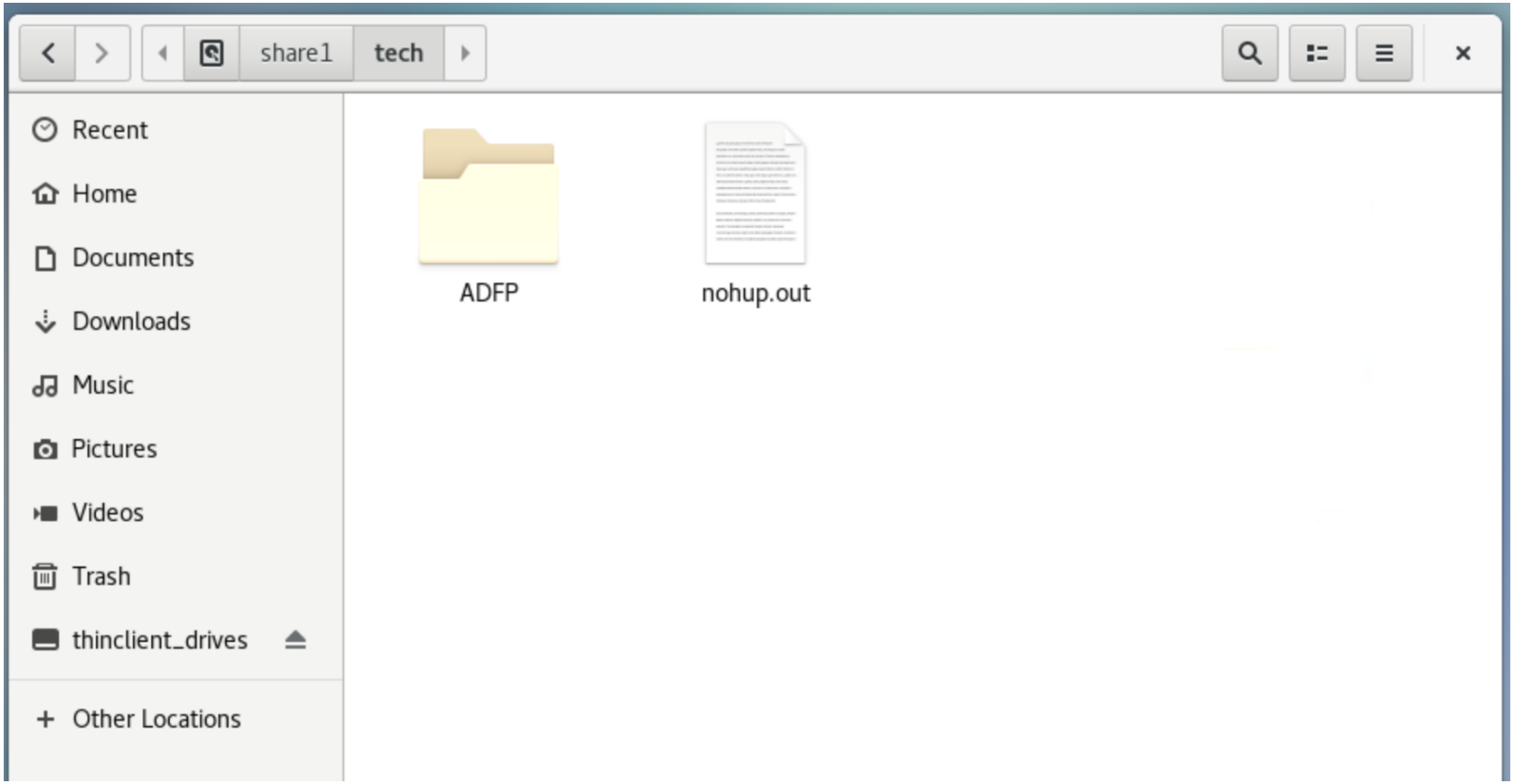
Remote Desktop Connection

- Type “cb” to source the license



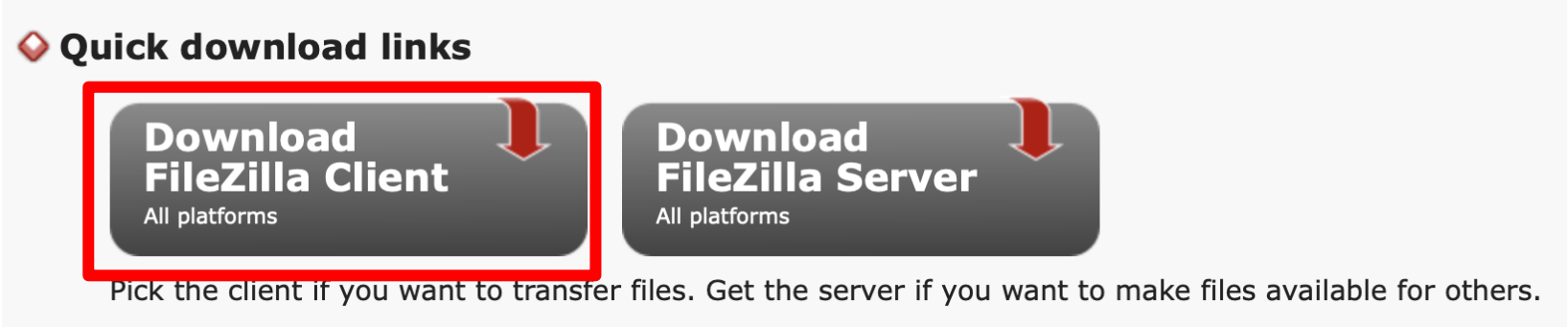
ADFP Library

- ADFP library: /share1/tech/ADFP



Upload Files to Workstation

- Download and install FileZilla



Setup the Site Manager

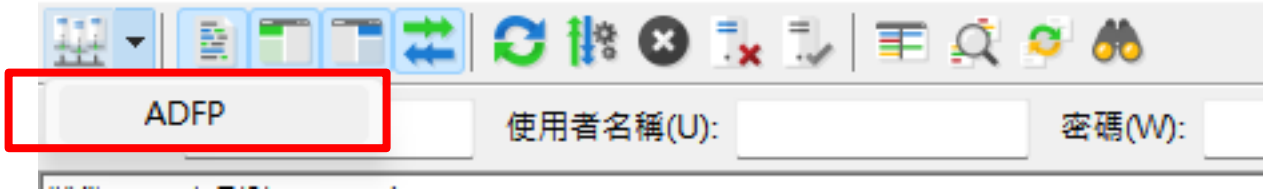
- Select File > site manager

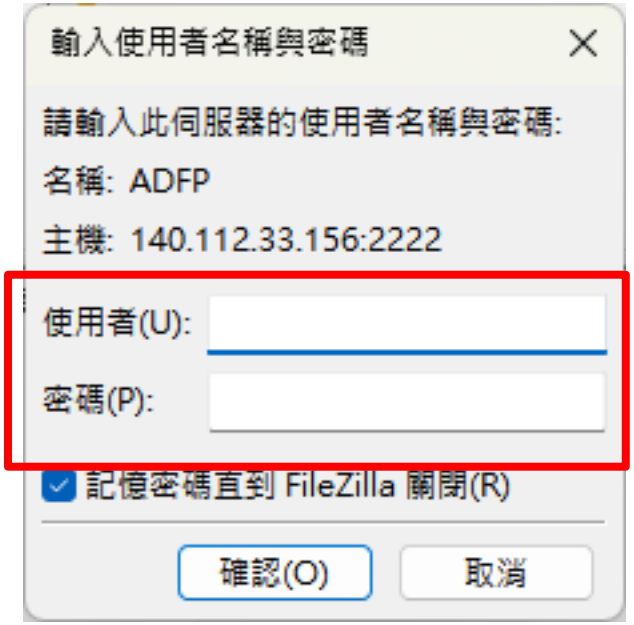
Setup the Site Manager

- Create a new site named ADFP

Protocol: SFTP
Host: 140.112.33.156
Port: 2222

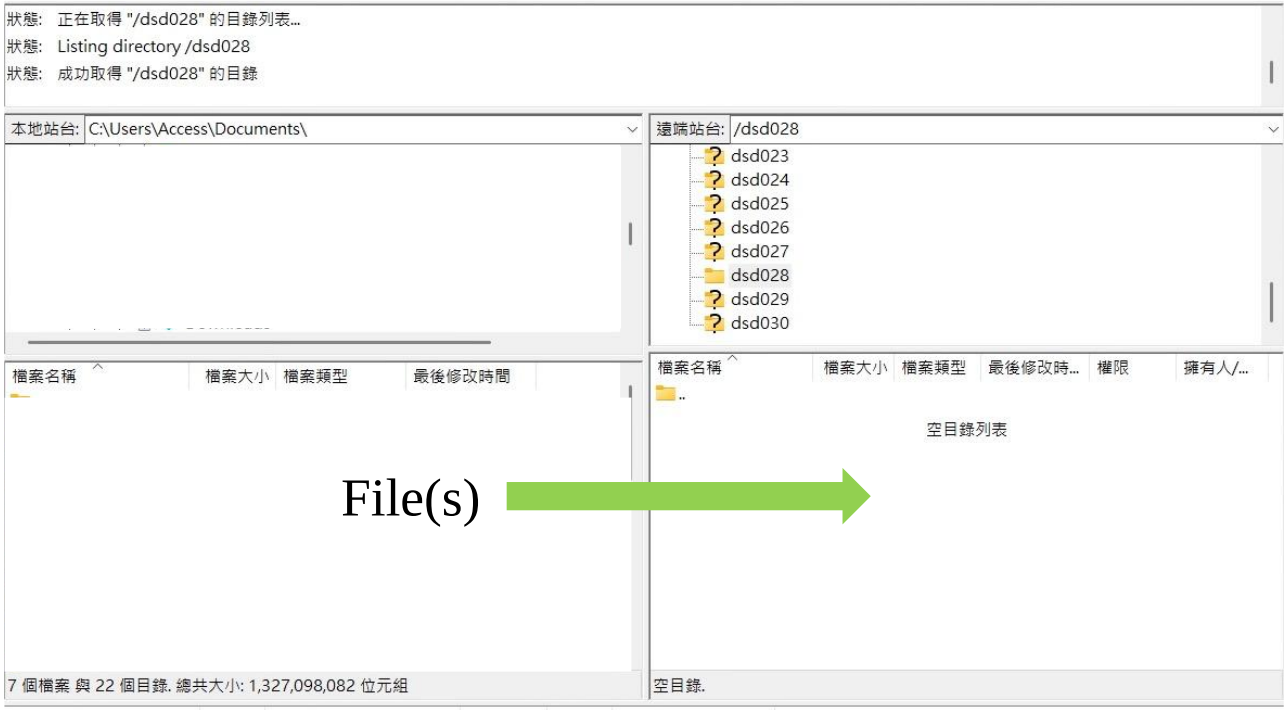
Connect to the Site



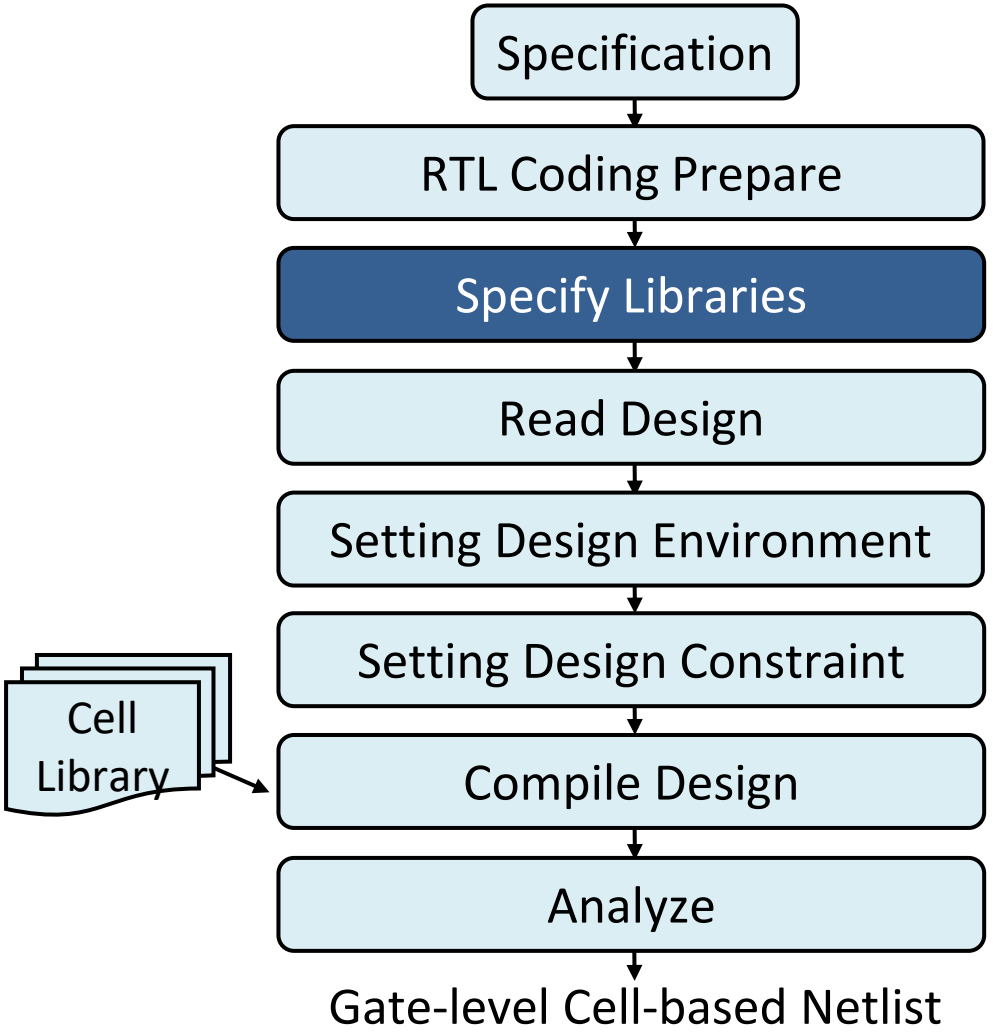


Upload Files

- Drag the file(s) to the right-hand side
- cp /homework/dsd/[dsd0xx]/[filename] ~/



Synthesis with ADFP



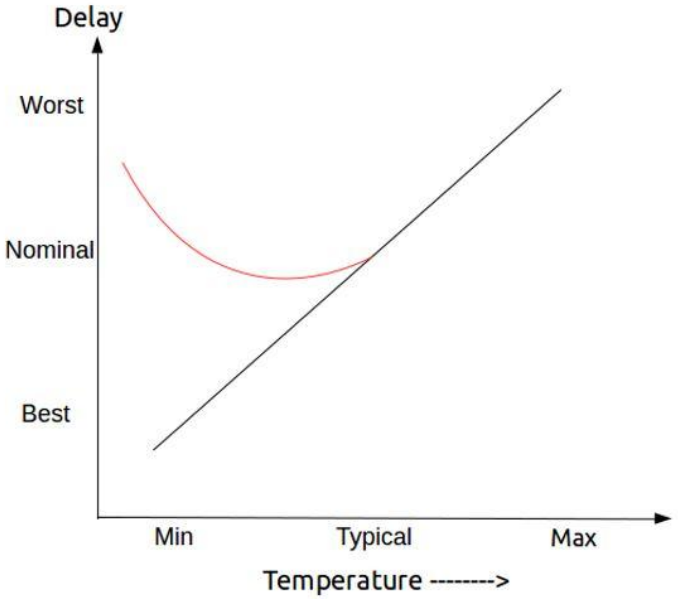
Synthesis with ADFP

In 0.13μm: slow.db / fast.db

```
set target_library "N16ADFP_StdCellff0p88v125c_ccs.db \
                    N16ADFP_StdCellff0p88vm40c_ccs.db \
                    N16ADFP_StdCellss0p72v125c_ccs.db \
                    N16ADFP_StdCellss0p72vm40c_ccs.db \
                    N16ADFP_StdCelltt0p8v25c_ccs.db \
                    N16ADFP_StdIOff0p88v1p98v125c.db \
                    N16ADFP_StdIOff0p88v1p98vm40c.db \
                    N16ADFP_StdIOss0p72v1p62v125c.db \
                    N16ADFP_StdIOss0p72v1p62vm40c.db \
                    N16ADFP_StdIOtt0p8v1p8v25c.db \
                    N16ADFP_SRAM_ff0p88v0p88v125c_100a.db \
                    N16ADFP_SRAM_ff0p88v0p88vm40c_100a.db \
                    N16ADFP_SRAM_ss0p72v0p72v125c_100a.db \
                    N16ADFP_SRAM_ss0p72v0p72vm40c_100a.db \
                    N16ADFP_SRAM_tt0p8v0p8v25c_100a.db \
                    "
```

Temperature Inversion

- In advanced technology, Cell delay increases in low temperature
- When T decrease, both μ_n and V_t increase
- V_{gs} is smaller in advanced technology

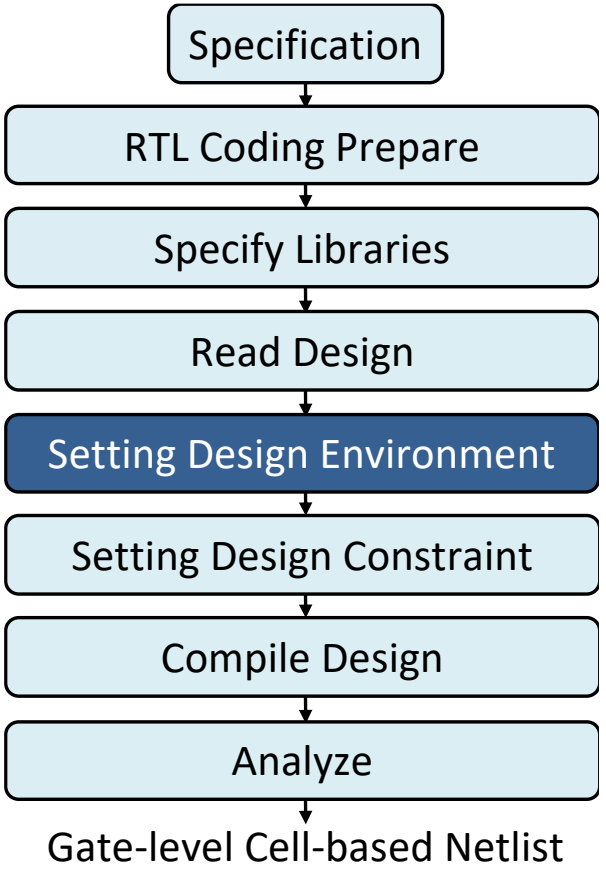


$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{gs} - V_t\right)^2$$

Design Environment

- Net delay provided by wire load model is not accurate
- No wire load model in ADFP

1. set_input_delay
2. set_output_delay
3. set_drive
4. set_load
5. set_operating_conditions
6. ~~set_wire_load_model~~



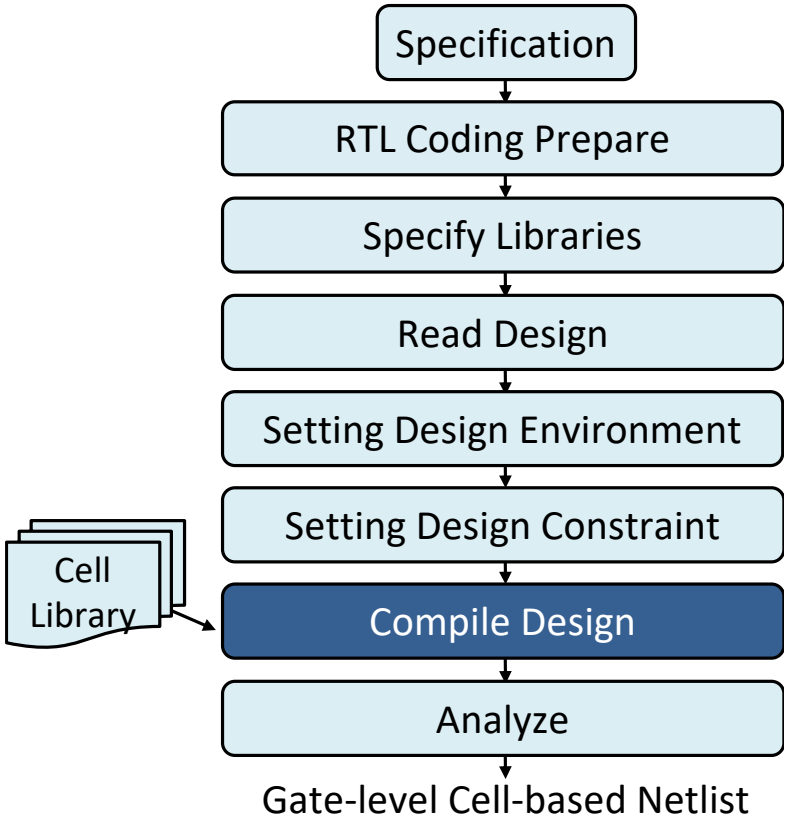
Compile Design

- May still have hold time violations after compile_ultra

```
compile_ultra
```

+

```
compile -inc
```



Compile Design

- No preset pin in ADFP register

```
always @(posedge clk or posedge rst) begin
    if (rst) begin
        in_a_buffer <= 1;
end
    else begin
        in_a_buffer <= in_a_buffer_nxt;
    end
end
```

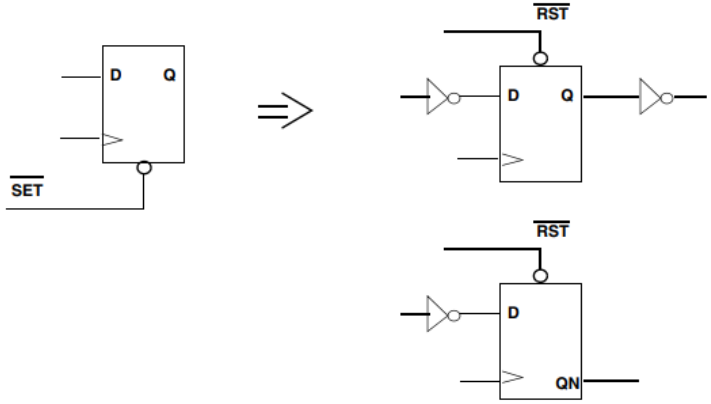
```
CKNDIBWP16P90LVT U28 ( .I(rst_n), .ZN(n18) );
\**FFGEN**  in_a_buffer_reg_0_ ( .next_state(n9), .clocked_on(clk),
      .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
      net434), .Q(in_a_buffer[0]), .QN(n20) );
\**FFGEN**  in_b_buffer_reg_0_ ( .next_state(in_b[0]), .clocked_on(clk),
      .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
      net434), .Q(in_b_buffer[0]) );
TIELBWP20P90LVT U33 ( .ZN(net434) );
```

Compile Design

- Set the option or use compile_ultra

```
set compile_seqmap_enable_output_inversion true
```

```
\**FFGEN**  in_a_buffer_reg_0_ ( .next_state(n9), .clocked_on(clk),
      .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
      net434), .Q(in_a_buffer[0]), .QN(n20) );
\**FFGEN**  in_b_buffer_reg_0_ ( .next_state(in_b[0]), .clocked_on(clk),
      .force_00(net434), .force_01(net434), .force_10(rst_n), .force_11(
      net434), .Q(in_b_buffer[0]) );
TIELBWP20P90LVT U33 ( .ZN(net434) );
```




```
DFCNQND1BWP16P90LVT in_b_buffer_reg_0_ ( .D(n14), .CP(clk), .CDN(n12), .QN(
      in_b_buffer[0]) );
DFCNQND1BWP16P90LVT in_a_buffer_reg_0_ ( .D(n30), .CP(clk), .CDN(n12), .QN(
      in_a_buffer[0]) );
```

Thanks! Feel free to ask me any questions!