

The USART ISP interface is implemented on the following pins:

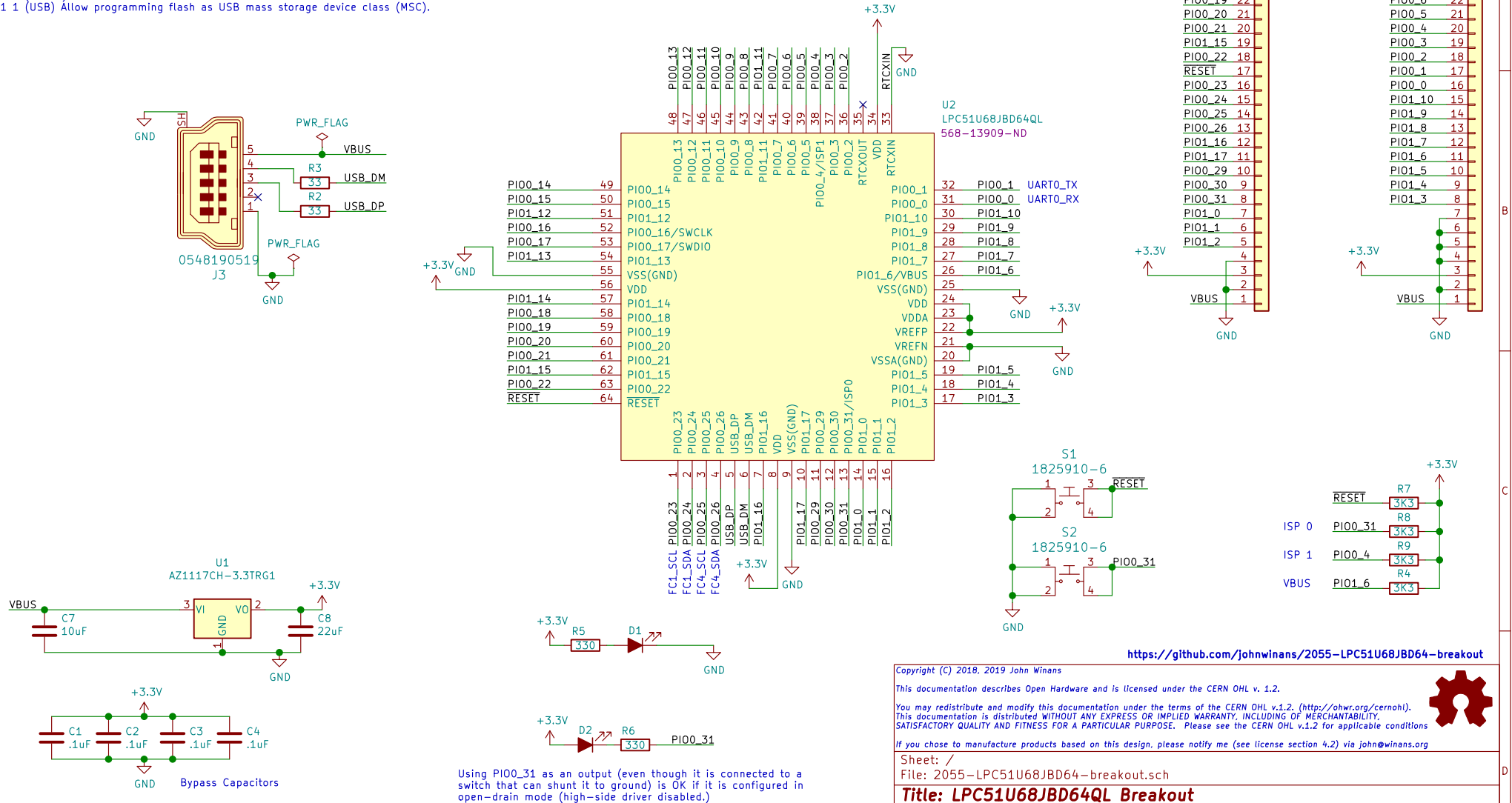
- PIO0\_0 for receive
- PIO0\_1 for transmit

The USB interface is implemented on the following pins:

- PIO1\_6 for VBUS
- USB0\_DP for USB D+
- USB0\_DM for USB D-

(ISP0/PIO0\_31) (ISP1/PIO0\_4) (VBUS/PIO1\_6)

1 x x (FLASH) ISP is bypassed. The device boots from flash if valid user code is detected.  
0 0 x (I2C/SPI) The first valid probe message on I 2 C of Flexcomm Interface 3.  
0 1 0 (USART) Part enters ISP via the USART of Flexcomm Interface 0.  
0 1 1 (USB) Allow programming flash as USB mass storage device class (MSC).



<https://github.com/johnwinans/2055-LPC51U68JBD64-breakout>

Copyright (C) 2018, 2019 John Winans

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.2.

You may redistribute and modify this documentation under the terms of the CERN OHL v.1.2. (<http://ohwr.org/cernohl>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.2 for applicable conditions

If you chose to manufacture products based on this design, please notify me (see license section 4.2) via [john@winans.org](mailto:john@winans.org)

Sheet: /  
File: 2055-LPC51U68JBD64-breakout.sch

**Title: LPC51U68JBD64QL Breakout**

Size: A4	Date: 2019-07-05
KiCad E.D.A. kicad 5.1.3-ffbf9f2284ubuntu18.04.1	Rev: 3a
	Id: 1/1