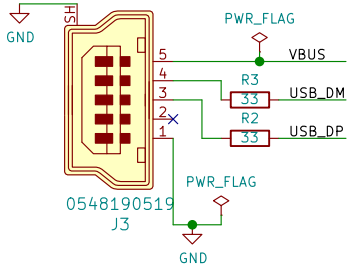
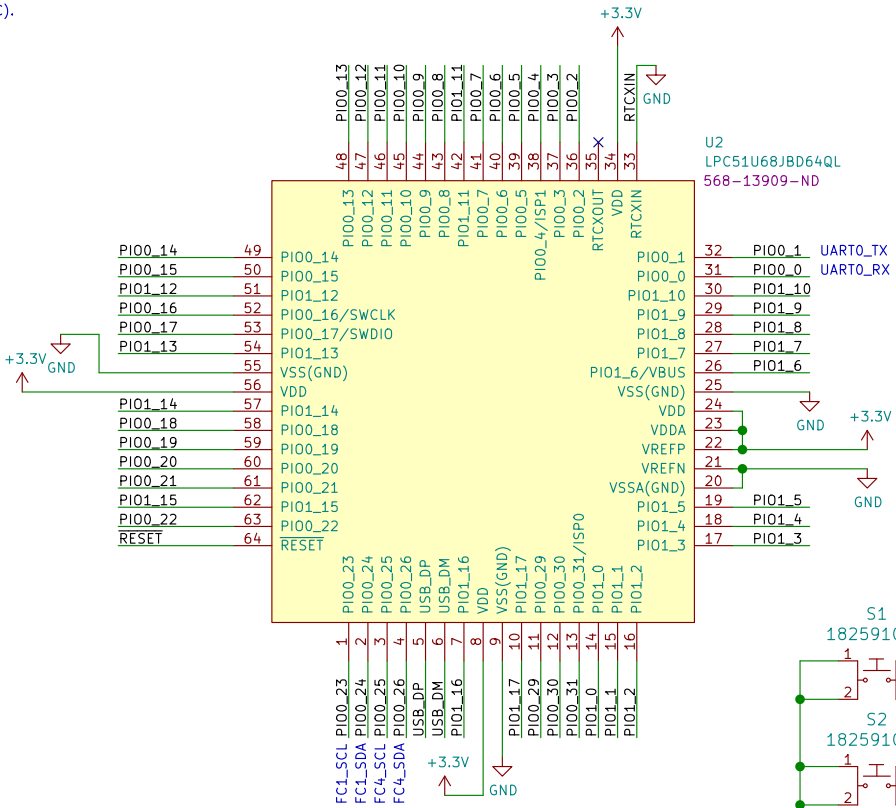
The USART ISP interface is implemented on the following pins:
- PIO0_0 for receive
- PIO0_1 for transmit

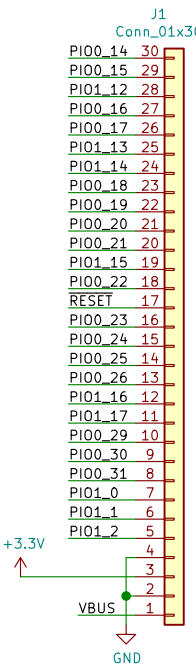
The USB interface is implemented on the following pins:
- PIO1_6 for VBUS
- USB0_DP for USB D+
- USB0_DM for USB D

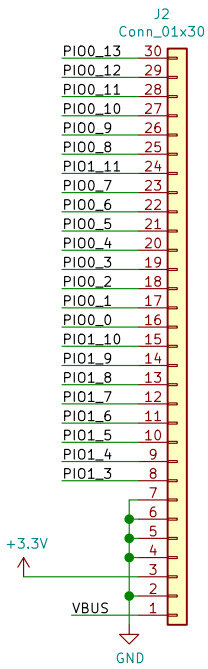
(ISP0/PIO0_31) (ISP1/PIO0_4) (VBUS/PIO1_6)

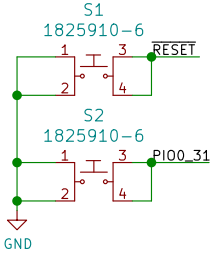
1 x x (FLASH) ISP is bypassed. The device boots from flash if valid user code is detected.
0 0 x (I2C/SPI) The first valid probe message on I 2 C of Flexcomm Interface 1 or SPI of Flexcomm Interface 3.
0 1 0 (USART) Part enters ISP via the USART of Flexcomm Interface 0.
0 1 1 (USB) Allow programming flash as USB mass storage device class (MSC).

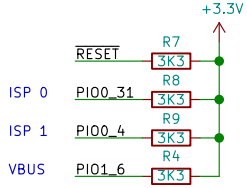


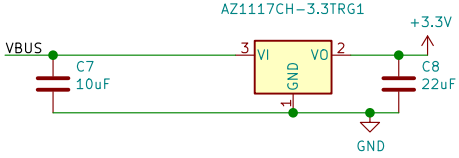


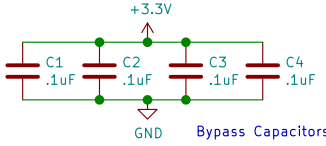


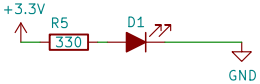


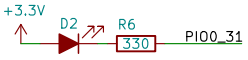












Using PIO0_31 as an output (even though it is connected to a switch that can shunt it to ground) is OK if it is configured in open-drain mode (high-side driver disabled.)

https://github.com/johnwinans/2055-LPC51U68JBD64-breakout

Sheet: /
File: 2055-LPC51U68JBD64-breakout.sch

Title: LPC51U68JBD64QL Breakout

Size: A4	Date: 2019-07-05	**Rev: 3**
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