McGill University

ECSE 335

Microelectronic Labs

4 - Buffer Stage (Prelab)

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4.1 Preparation

As shown in Figure 1.1, both circuits designed need to be interfaced for correct operation by some kind of an interface circuit, or buffer circuit. The purpose of this circuit is to ensure minimal loading of the gain stage and proper DC biasing of both stages. The latter is particularly important as the DC level of the gain stage's output and the output stage's input must be kept the same as when they were tested individually. In this section, you must design a transistor based circuit which will accomplish this function. Notice that, thanks to this circuit, the output stage will not require the input biasing circuit of Figure 3.3.

4.1.1 Determine the design specifications of the circuit which you believe are required for proper operation of the operational amplifier. Be sure to have a logical reasoning as to why each specification you decide upon is required. Some common design specifications are: Bandwidth, gain, input resistance, output resistance, input DC insensitivity, input maximal swing, and output maximal swing.

The following design specifications are required for the proper operation of the operational amplifier.

- **Bandwidth:** Since the buffer is designed to be an interface and not the actual amplifier, it should not delimit the bandwidth of the amplifier. Hence, the bandwidth of the buffer stage should be smaller than the bandwidth of the amplifier.

- **Gain:** The buffer stage should have a unity gain of 0dB.

- **Input Resistance:** The input resistance of the buffer stage should be greater than the output resistance of the differential amplifier, hence greater than $9.06M\Omega$.

- **Output Resistance:** The output resistance of the buffer stage should be lower than the input resistance of the output stage.

- **Input DC Insensitivity:** A decoupling capacitor at the input node should be added in order to bias the circuit to a specific DC voltage insensitive to noise.

- **Input Maximal Swing:** The input maximal swing should be larger than the maximum output of the differential amplifier of 600mV.

- **Output Maximal Swing:** Since the AB output stage has a 10 V/V gain and a 6V peak-to-peak output, the maximal output swing should be 600mV.

4.1.2 Based on the design specifications you have decided upon, create a circuit capable of meeting these specs and, if necessary, modify the specifications slightly if you deem them ultimately unattainable. Determine the component values and explain the functioning of your interface circuit. Provide a schematic of the design.

A Darlington pair could be used to obtain a high input impedance buffer stage.

Set the bias current according to:

$$R_{in} = \beta^2(r_e + R_{EE}) = 100 * 100(V_t/I_e + R_{EE}) > 9.06M\Omega$$

$$V_t/I_e + R_{EE} > 906M\Omega$$

Choose R_{EE} such that the DC output bias is set to -4V:

$$[0 - (-1.4) - (-4)]/0.25m = 10k\Omega$$

Using the result of R_{EE} :

$$I_e < (100 * 100 * 0.25)/(106000) = 2.3mA$$

$$I_e = 0.25mA \rightarrow r_e = V_t/I_E = 100\Omega$$
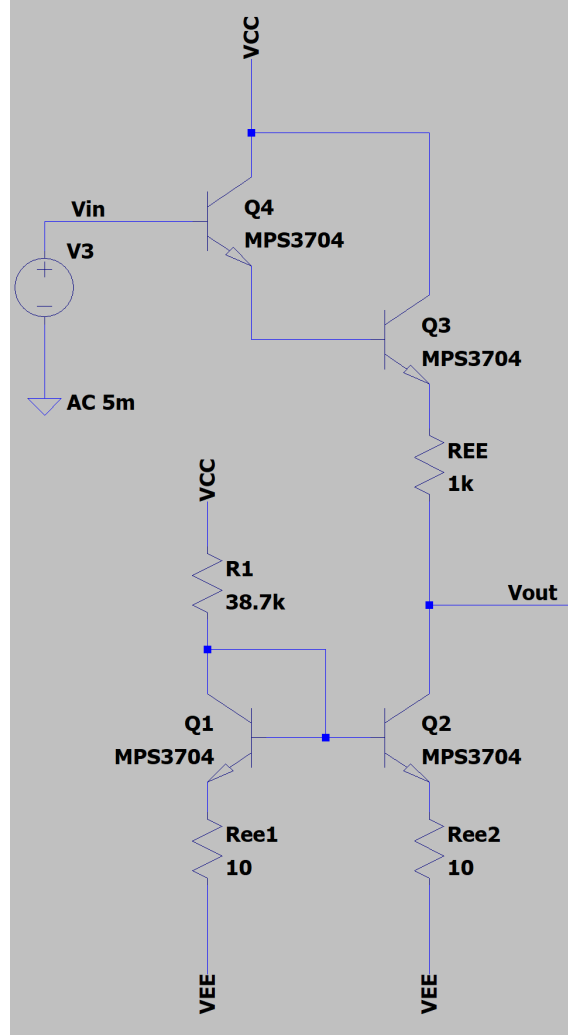
$$R_1 = (10 - 0.3)/0.00025 - 10 = 38.7k\Omega$$

Figure 1: Buffer Stage Schematic

Note that R_{ee1} and R_{ee2} heats sinks are added to prevent thermal runaway.

4.1.3 Determine the input and output resistances of the circuit.

$R_{in} = \beta^2(R_{EE} + r_e) = 100 * 100 * (10000 + 100) = 101M\Omega$

$R_{out} = (r_{o3}||r_{e3} + R_{EE}) = r_{e3} + R_{EE} = 100\Omega + 10k\Omega$

4.1.4 Plot the time domain output of the circuit to an input which is comparable to the maximum expected differential amplifier output.

In the first lab, a simulation was already created for the output hence the input to the buffer stage will be the same plot.
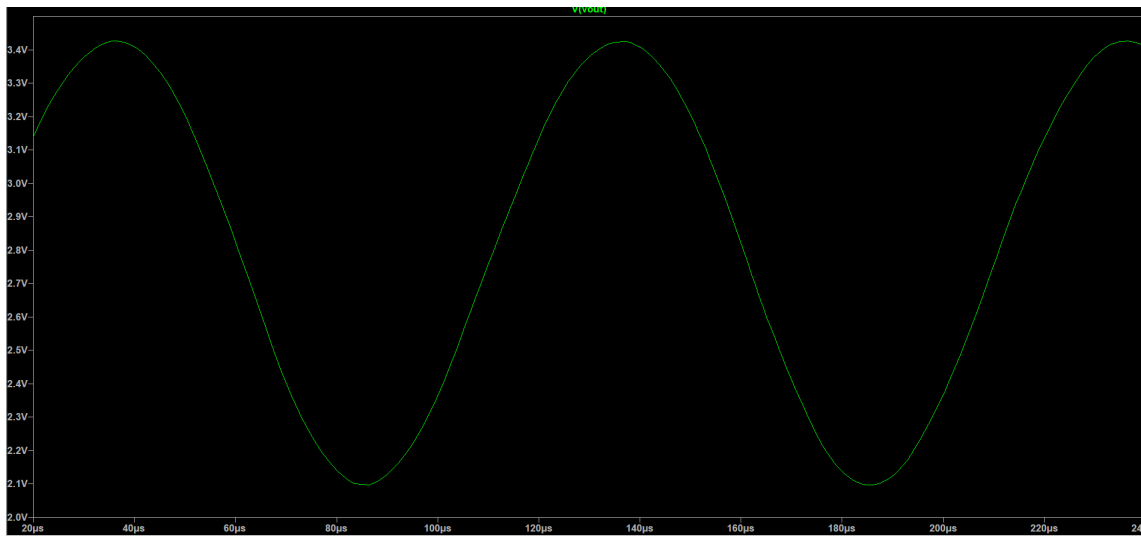

Figure 2: Input of buffer circuit

4.1.5 Plot the frequency response of the circuit. Ensure that the parasitic capacitors are accounted for.

Figure 3: Frequency Response

We can see that the frequency response gives the expected gain of 0dB.

4.1.6 Plot the voltage transfer curve of the circuit. Document the maximal output and input ranges.

Figure 4: Voltage Transfer Curve

As shown in the plot, the maximum output voltage ranges from approximately -5 to 4.1V with a corresponding maximum input range from -3.9 V to 4.1 V.

3.1.7 Comment of the advantages and disadvantages of your design.

The advantages of the design are:

- It has a large bandwidth.
- It has a unity gain.
- It is simple to implement.

The disadvantages of the design are:

- It consumes a lot of power because it is still consuming current without any input running through.
- R_{EE} has to be limited to a certain number since too high a resistance will cause unwanted loading at the output.