

CONFIDENTIAL B

MEDIATEK

MT2503 Design Notice

V1.3



Agenda

- What is MT2503
(Difference with MT6261+MT3333) --- page 003
- Design Notice - MT2503_Baseband --- page 009
- Design Notice - MT2503_RF --- page 139
- Design Notice - MT2503_GPS --- page 189
- Design Notice - MT2503_Bluetooth --- page 198
- Design Notice - MT2503_FM_Receiver --- page 209

Change History

Version	Date	Description
V0.1	2015.10.22	1 st release
V0.2	2015.11.05	<ul style="list-style-type: none">•Page 6: Set Varname(gpio_lcm_rst_pin) in DCT for LCM reset of pin M14(SIM2_SRST)•Page 7: Remove 2-step download description (MT2503 default use 1-step download)
V1.0	2015.12.09	<ul style="list-style-type: none">•Page 4/11/12 : Add thickness=1.0mm•Page 8 : Add notice for GPS interface•Page 10/11 : Remove double keypad•Page 19 : Update JTAG pin mapping•Page 23 : Cheng title to "MT2503_Baseband keypad"•Page 24 : MT2503 is not suitable for extend keypad design, please design traditional keypad•Page 135 : Change the pin C5 description (remove ATV)•Remove page of "Distance between TXM and crystal" in page 177 of V0.2•Remove page of "Sky77569 2-L PCB Layout Suggestion" in page 172 of V0.2•Remove page of "Stack Up (2 Layer)" in page 157 of V0.2•Page 143 : Remove ATV co-clock•Page 143/145/147 : Modify BPI connection notice•Page 144 : Add R3019 in pin D5 (EXT_CLK_SEL)•Page 151 : Fix typo of FREF pin name, remove ATV co-clock•Page 161 : Remove 2-L layout suggestion
V1.1	2015.12.18	<ul style="list-style-type: none">•Page 23~Page29 :Add GPIO Select guide in design notes
V1.2	2016.02.02	<ul style="list-style-type: none">•Page191: Add MT2503 GPS Schematic design notice•Page206: Add MT2503 BLE Solution Notice
V1.3	2016.05.10	<ul style="list-style-type: none">•Page121:change charge BJT DC Gain value (beta should be between 60~100)



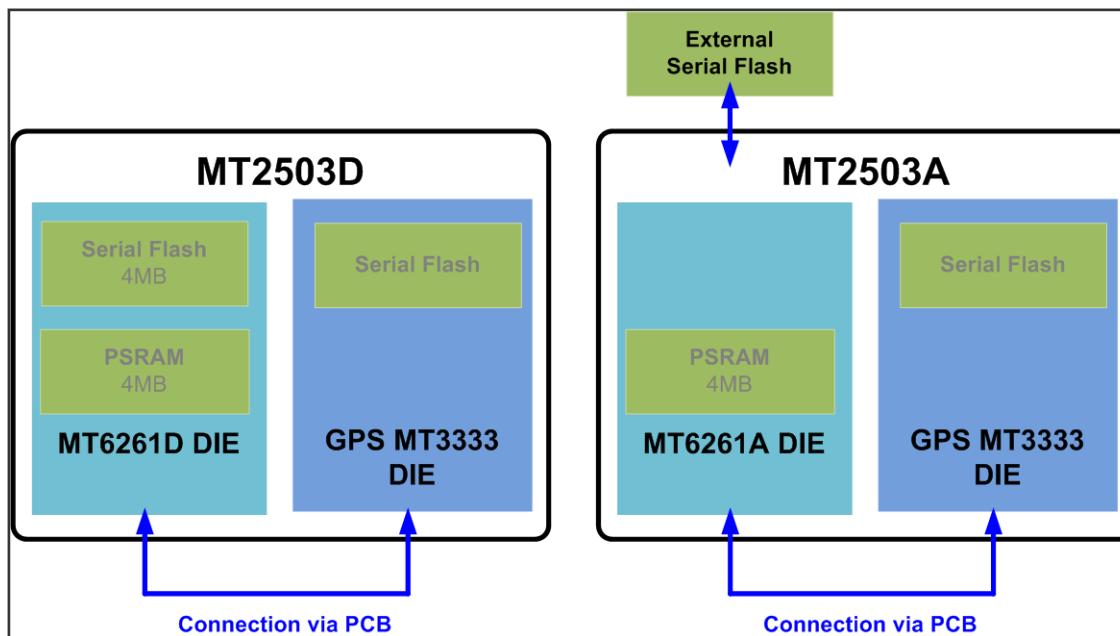
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What is MT2503 (Difference with MT6261+MT3333)



What is MT2503

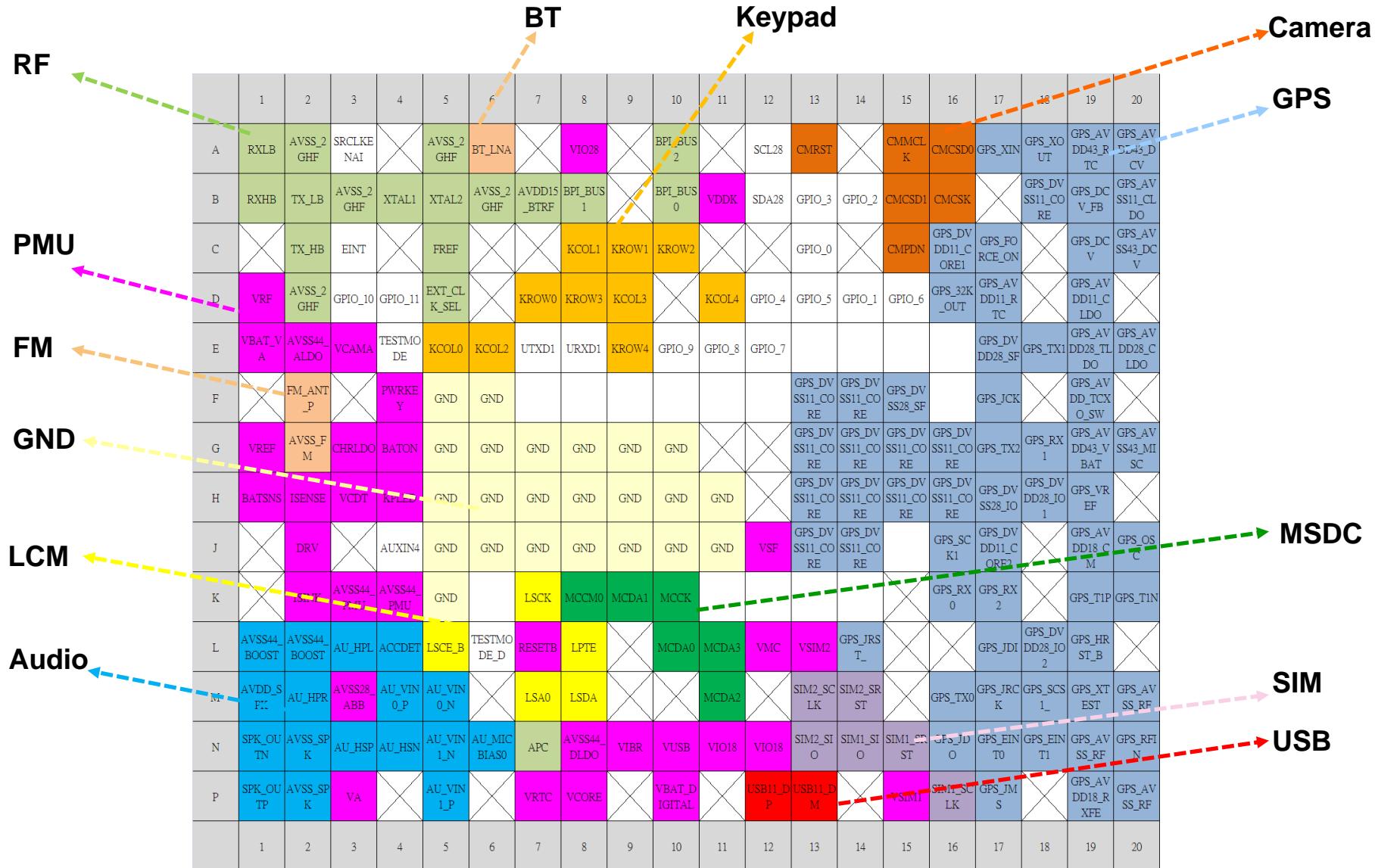
- MT2503 = SiP(System in Package) of MT6261 and MT3333
 - Refer to following diagram
 - MT2503 **de-feature** the internal **class-K** audio amplifier
(MT2503 only support internal class-AB audio amplifier)
 - MT2503 **remove LSRSTB (GPIO45) pin**
 - Then, MT2503 **optimize the SiP ballmap** (refer to next page)



- Package:**
- 8.4*6.2 mm²
 - Thickness=1.0mm
 - 215 ball count
 - 0.4 mm pitch
 - VFBGA

- MT2503D : With 4MB serial flash
- MT2503A : Use external serial flash

What is MT2503 - Ballmap

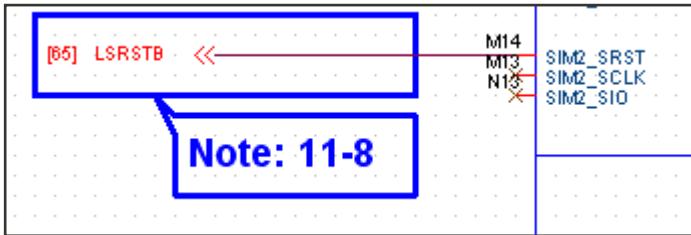


LCM reset pin

- MT2503 have no "LCM reset pin", please use pin M14(SIM2_SRST) to be LCM reset signal.
 - The SIM2_SRT power domain=1.8V, and LCM power domain=1.8V
 - Set Varname(gpio_lcm_rst_pin) in DCT, then DCT will use SIM2_SRST to control LCM reset

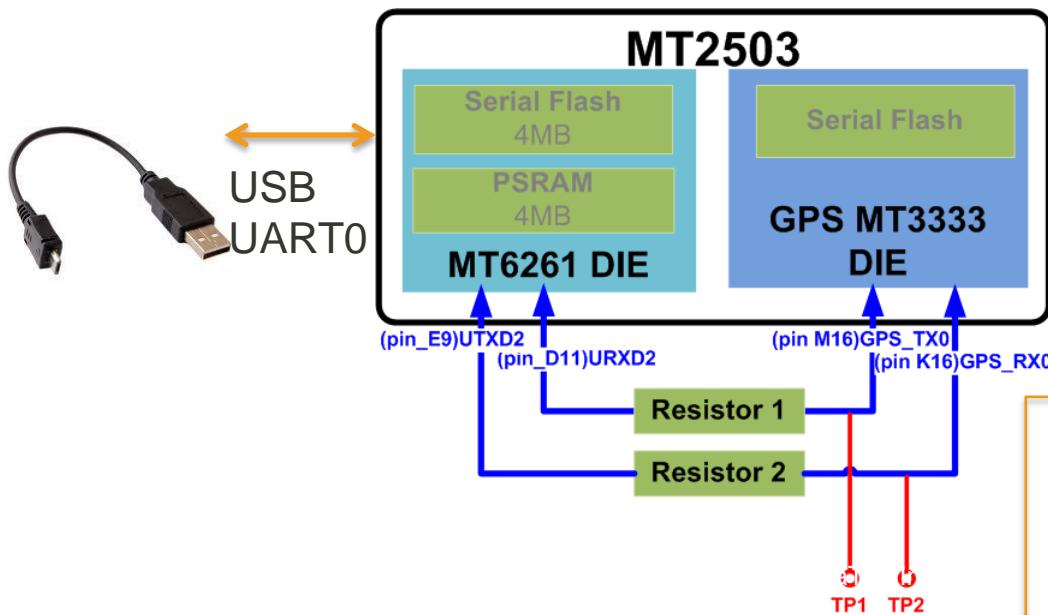
	GPIO Setting	GPO Setting	EINT Setting	PWM Setting	ADC Setting	KEYPAD Setting	PMIC Setting									
	Def.Mode	M0	M1	M2	M3	M4	In...	In...	R0	R1	D...	In	Out	INV	O...	VarName1
GPIO41	0:GPIO41	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	gpio_lcm_rst_pin							

- If you need dual SIM and LCM function, please contact MEDIATEK



1-step Download

- MT2503 default use 1-step download : download MT6261 bin and MT3333 bin simultaneously
 - As downloading, connect download cable to USB or UART0



Resistor 1/2 : 0 ohm
TP1 /TP2 :Don't care
Just reserved for debug

GPS Interface Notice

- Please follow reference design to choose the interface between MT6261 and MT3333.
- Don't change those pins of KCOL4/KROW4/KROW3/KROW2 for GPS control
- If you change those interface, system have high risk for download and normal power on.

MT6261	MT3333	Direction of MT6261	Note
KCOL4 (pin D11)	GNSS_UART_TX (pin M16)	INPUT	Don't change to other pin
KCOL3 (pin D9)	GNSS_TXIND (pin E18)	INPUT	
KROW4 (pin E9)	GNSS_UART_RX (pin K16)	OUTOUT	Don't change to other pin
KROW3 (pin D8)	GPS_32K (pin A17)	OUTOUT	Don't change to other pin
KROW2 (pin C10)	GPS_LDO_EN (to external LDO of enable)	OUTOUT	Don't change to other pin

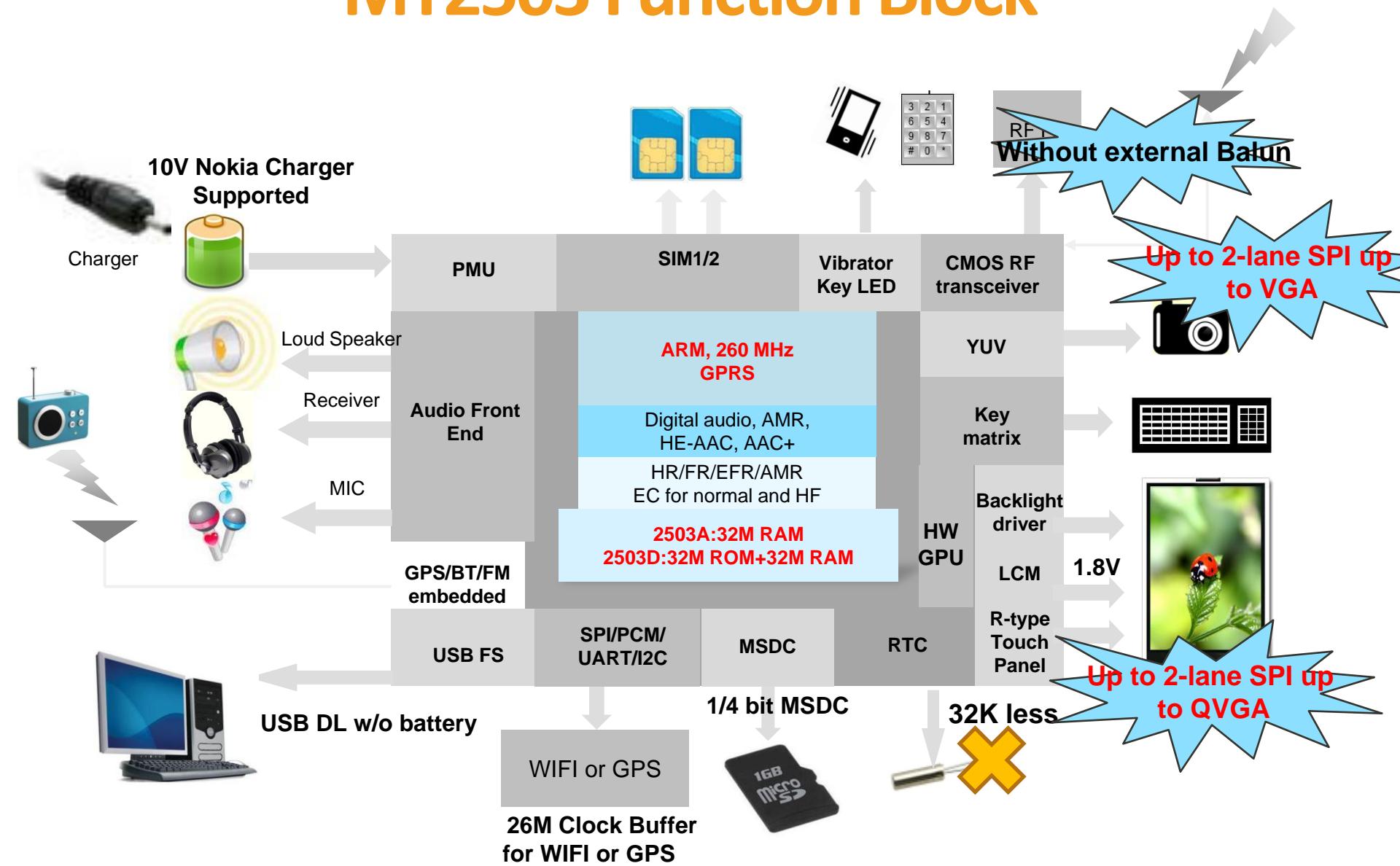


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Design Notice - MT2503_Baseband



MT2503 Function Block



Snapshot of MT2503 (1/3)

Processor :

- ARM7EJ-S 260 MHz

PMU :

- PMU/R-type TP/Backlight driver/ Vib driver
 - PMU integrate 12 LDO
 - R-type controller
 - PMU support 1 channel current sink for serial LED of LCD backlight
 - Class AB audio AMP
 - Support 2 SIM interface
 - PMU support 1 channel for KEYPAD LED .
 - Support RTC Less

Memory :

- MT2503A : ex SF (please check QVL)
- MT2503D : SIP 32Mb Serial Flash up to 133Mhz .
- Booting from Serial Flash
- **Stack up 32Mb PSRAM up to 133MHz**

Multimedia :

- **Dedicate serial 1.8 LCM interface**
- **LCD resolution up to QVGA**
- Support Serial camera
- **Camera resolution VGA**

Connectivity :

- USB 1.1 FS (12 Mbps)
- 5 x5 keypad
- BT / FM / GPS embedded
- BT 3.0 Integrated + 2.1 EDR

Modem:

- GSM/GPRS
Quad Band, TX/RX VAMOS
- Integrated RF transceiver ,
single-end SAW less

Snapshot of MT2503 (2/3)

Audio:

- Integrated max 0.8W high power Class AB speaker amplifier

Speech:

- Support FR/HR/EFR/AMR speech codec

Data storage:

- 4 bit memory card interface with dedicate LDO (Max:3.3)
- Support SD2.0 / SDIO1.1

Package:

- 8.4*6.2 mm²
- Thickness=1.0mm
- 215 ball count
- 0.4 mm pitch
- VFBGA

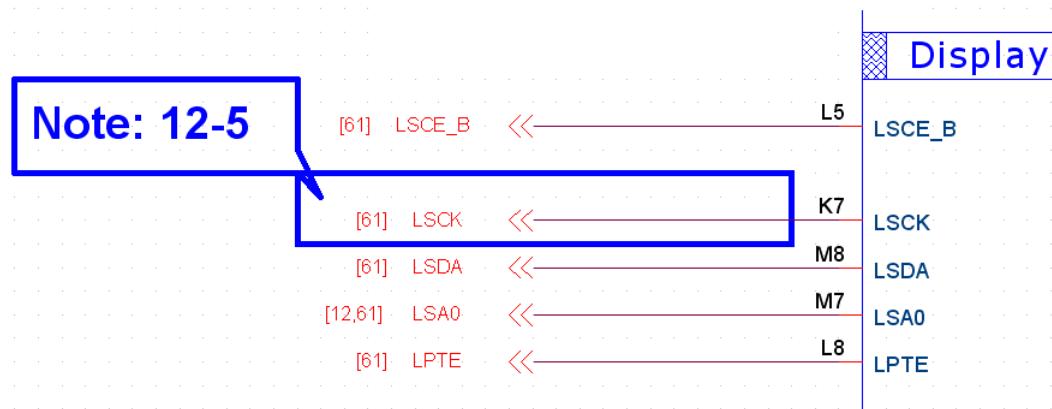
Snapshot of MT2503 (3/3)

Chip Feature List		MT2503
MODEM	EDGE RX	/
MCU System	RISC	ARM7EJ-S
	Speed	260Mhz
Serial NOR Flash	Supply voltage	3V/1.8V
	Speed	78/104/133MHz
LCM	Resolution	QVGA(serial)
Camera	Pixel	VGA YUV(serial)
Audio AMP	Out power	Class AB, 0.8W(HW spec)
Package	Dimension	BGA 8.4x 6.2 (Thickness=1.0mm)
	Ball	215
PCB	Layer	4
	Trace	4/4

MT2503 HW Pin (1/3)

Pin name	Pin out	Pull down	Pull high 10K to VIO18
LSCK	K7	Normal mode	Test mode

- Don't reserve any pull-up circuit in LSCK

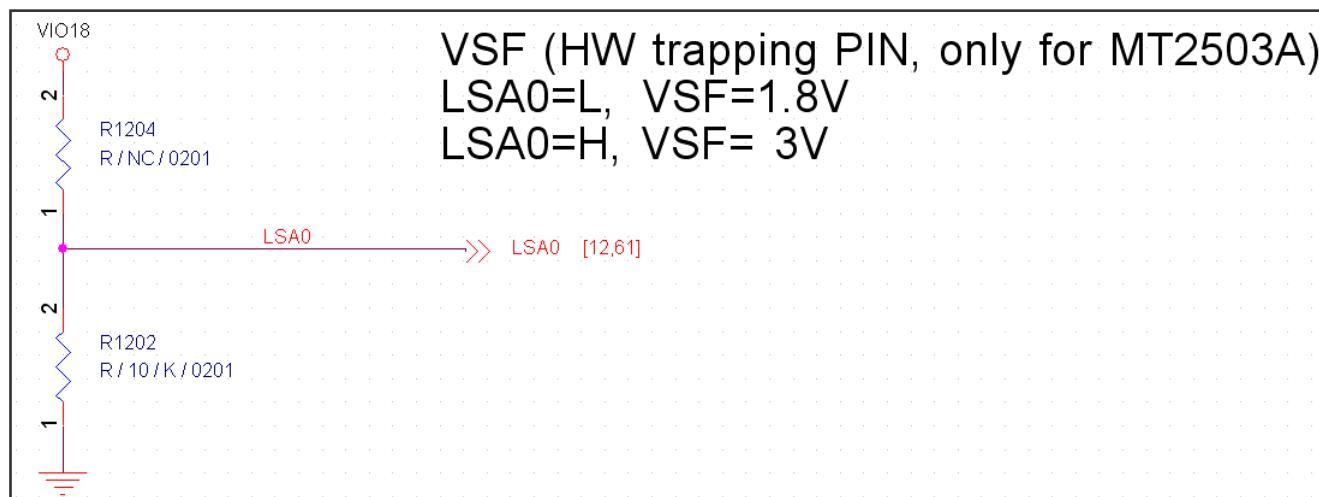


- For normal usage, please configure above pins to be “Normal mode”.
 - All pins must follow, otherwise system may not download or boot-up
- For Security Enable, please contact MTK support window

MT2503 HW (Pin 2/3)

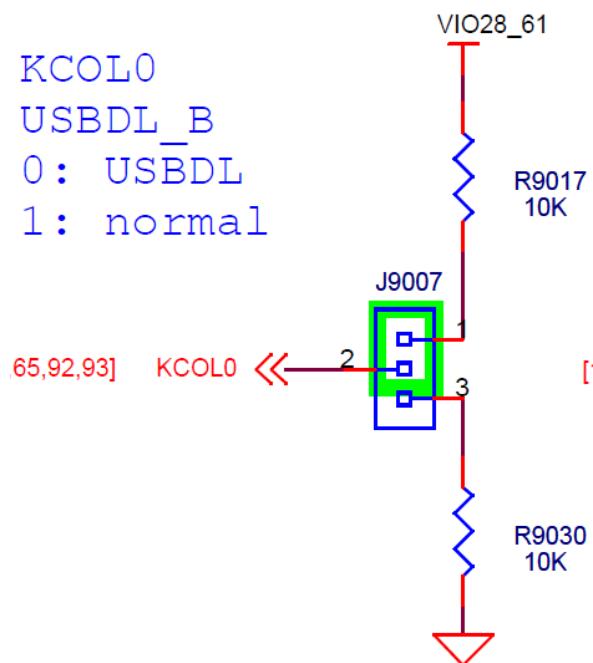
Pin name	Pin out	3V Serial flash booting	1.8V Serial flash booting
LSA0	M7	Pull high 10K to VIO18	Pull down 10K to GND

- MT2503A needs external flash, so LSA0 Pin(M7) should choose pull-up or pull-down circuit according to flash power domain.
- MT2503D has built-in flash, so LSA0 Pin does not need pull-up or pull-down circuit.



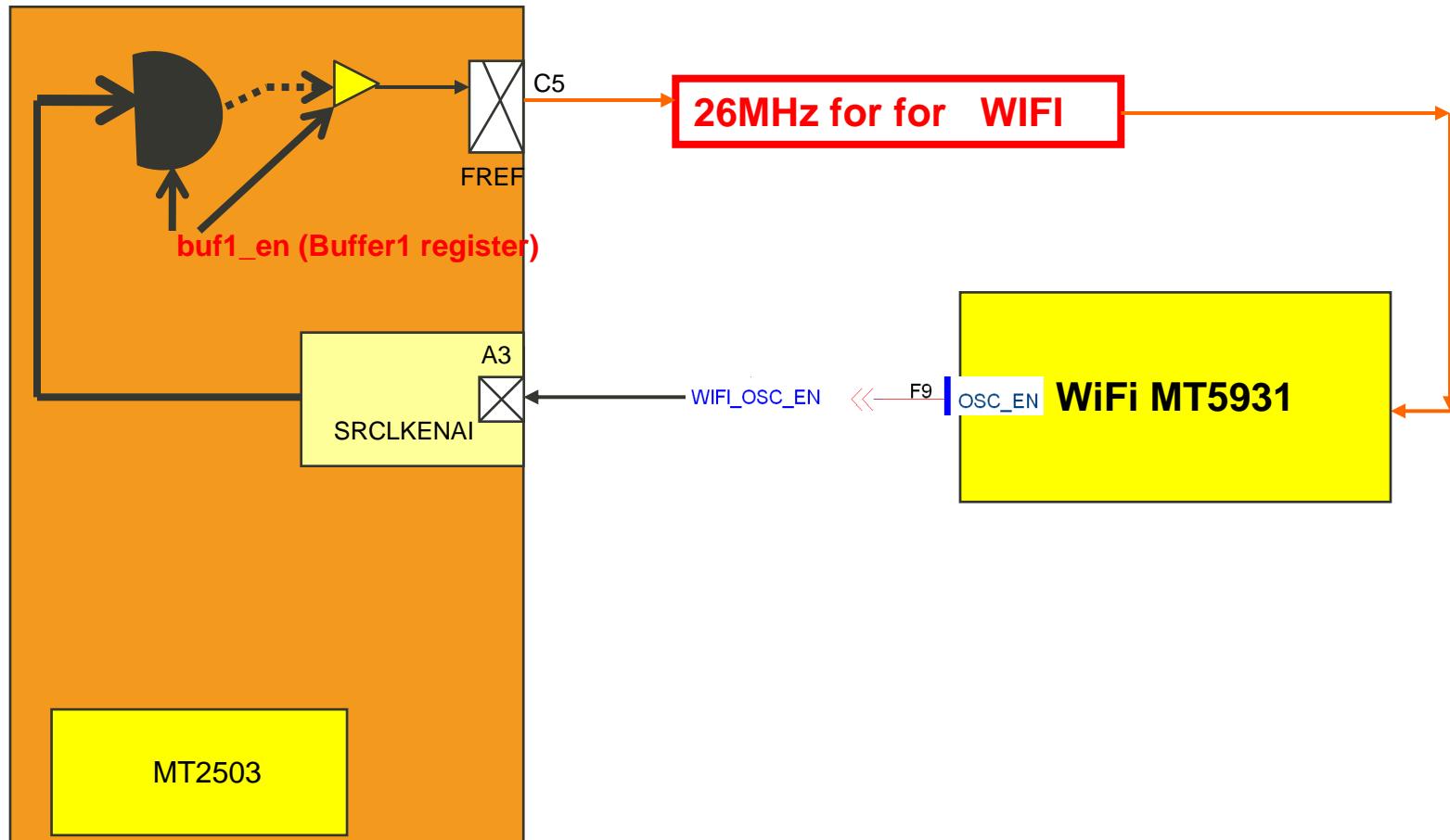
MT2503 HW Pin (3/3)

Pin name	Pin out	USB download mode	Normal boot up mode
KCOL0	B13	Pull down 10K to GND	Pull high 10K to VIO28



MT2503 - SRCLKENAI

- Used as 26MHz clock provided from MT2503.



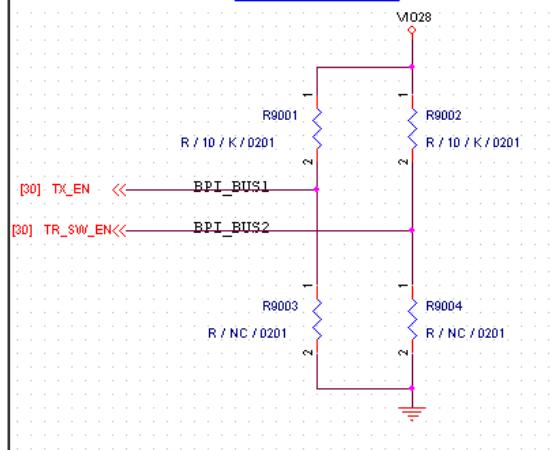
MT2503 - JTAG (1/2)

JTAG trapping	BPI_BUS1	BPI_BUS2
X	LOW	LOW
KEYPAD out	LOW	HIGH
CAM out	HIGH	HIGH

- MT2503 JTAG MUX in Camera & Keypad by HW trapping
- For selection, please choose pull-high or pull-down resistor with 10K

AP JTAG Trapping

Note: 90-1

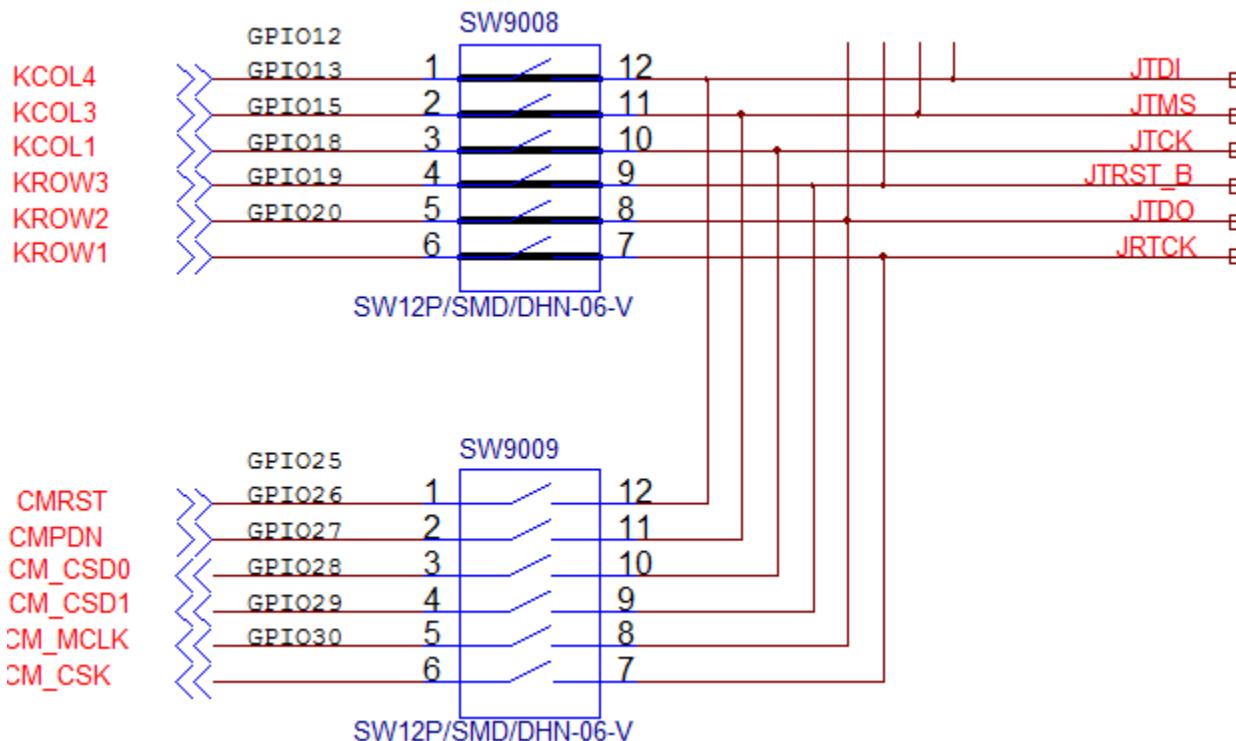


Schematic design notice of "90_DEBUG_IO" page.

Note 90-1: 1. Refer to "MT6261 design notice" for JTAG option
 (1)BPI_BUS1=L, BPI_BUS2=L, then JTAG=N/A
 (2)BPI_BUS1=L, BPI_BUS2=H,
 then JTAG=KROW1/KROW2/KROW3/KCOL1/KCOL3/KCOL4
 (3)BPI_BUS1=H, BPI_BUS2=H,
 then JTAG=CMRST/CMRDN/CMCSD0/CMCSD1/CMMCLK/CMCSK

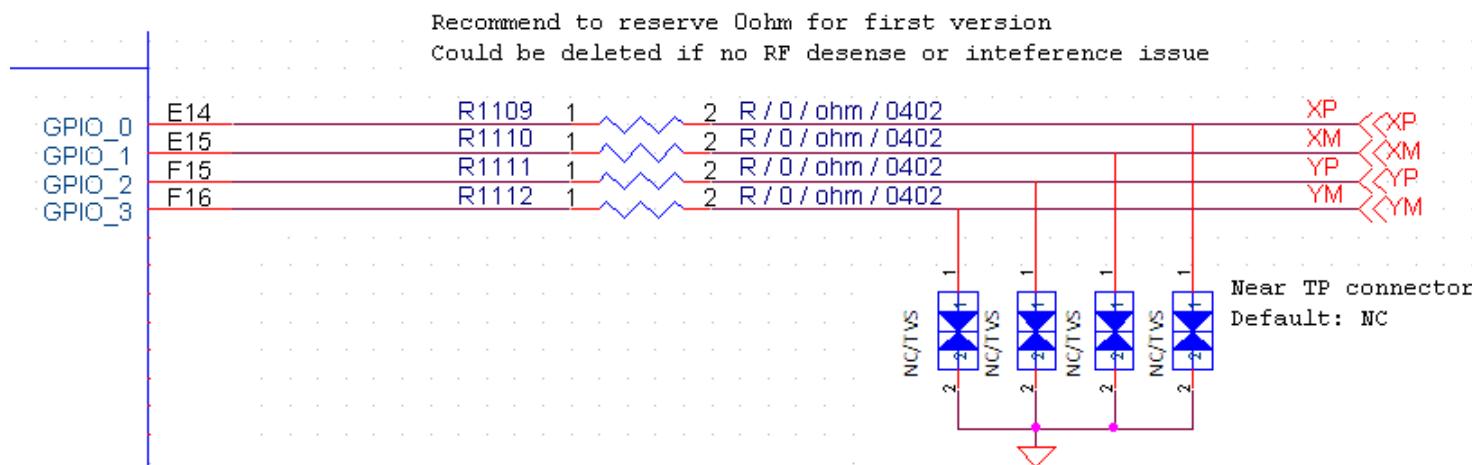
MT2503 - JTAG (2/2)

Please reserve test point on **Keypad / Camera** interface, please refer to PINMUX table
(MT2503_GPIO_Formal_Application_Spec.xlsx)



RTP

- Recommend to reserve 0ohm and varistor in the first version.
- For RF de-sense issue, replace 0ohm with adequate beads.
- For ESD issue, mount adequate varistor. The capacitance of varistor should be less than 100pF.
- These components can be removed in later version to save BOM cost.



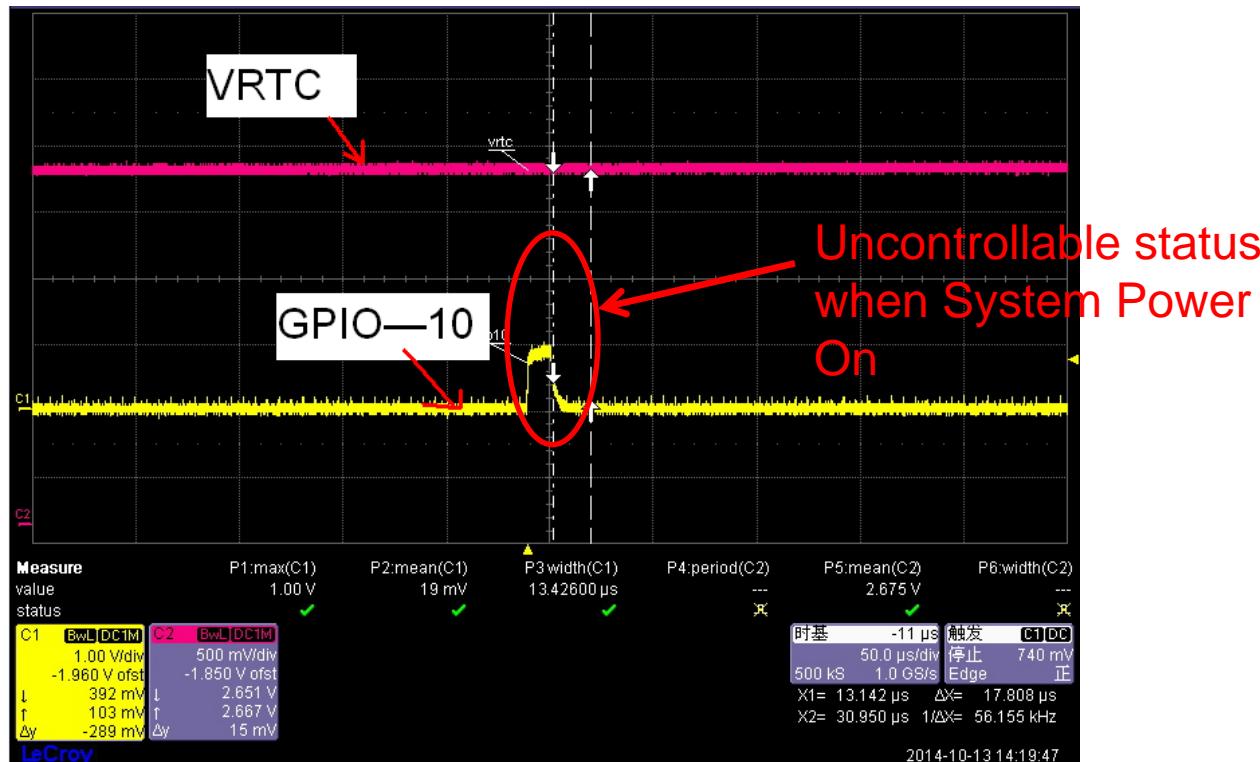
AGPIO

- **AGPIO on RF pin ,which will be used for EINT and GPIOs**
 - 2 among of the 4 pins serve as only input (EINT/SRCLKENAI)
 - Voltage 2.8V power domain
 - **GPIO_10=AGPIO54≠GPIO10**
 - **GPIO_11=AGPIO55≠GPIO11**

Power domain	Pin Name	Default mode	Mode 0	Mode 1	Mode 2
2.8	EINT	AGPI52	AGPI52		EINT23
2.8	SRCLKENAI	AGPI53	AGPI53	SRCLKENAI	EINT24
2.8	GPIO_10	AGPIO54	AGPIO54		
2.8	GPIO_11	AGPIO55	AGPIO55		

AGPIO

- AGPIO on RF pin ,there are some limit when use it as GPIO function
 - **GPIO_10and GPIO_11 have a uncontrollable status when battery insert, so don't use AGPIO to control sensitive device**



Design Notice – GPIO Selection

Design Notice – GPIO selection for HW design (1/4)

1. Pull-Up / Pull-Down selection :

- Choose GPIO with suitable PU/PD after reset state for application
- DO NOT use GPIO with default pull up enable(PU after HW reset) as enable signal

2. Power domain of IO supply selection :

- Choose GPIO with suitable power domain of IO supply for your own application
- Please check the power domain of each GPIO you choose

3. Please choose suitable GPIO for peripheral IC :

- Please choose GPIOs with matched direction, pull-up/pull-down, data inversion, data output, gpio mode after reset state for peripheral IC application

4. There are two groups of special IO pad (with R0 R1 setting) in MT2503 which can change different pull resistor for different application

- KCOL0~KCOL4 , KROW0~KROW4

URXD:

CMPDN/CMCSD0/CMCSD1/CMMCLK

MCCK/MCCM0/MCDA0/MCDA1/MCDA2/MCDA3

LSRSTB/LSCE_B/LSCK/LSDA/LSA0/LPTE

RESETB

Design Notice – GPIO SW driver setting (Drv_Tool) (2/4)

After enable “InPull En”, you can **change the PU/PD value** by changing “InPull SelHigh”.

“OutHigh” can **change the default output level**.
(Only valid when GPIO is **output** mode)

“InPull En” can **enable/disable PU/PD**, then
GPIO can be set as the PU/PD when SW
doing GPIO initiate.

	Def....	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	InPull En	InPull SelHigh	R0	R1	Def...	In	Out	INV	OutHigh
GPIO0 2:XP		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								
GPIO1 2:XM		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								
GPIO2 2:YP		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								
GPIO3 2:YM		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>								
GPIO4 NC																				
GPIO5 NC																				
GPIO6 NC																				
GPIO7 NC																				
GPIO8 NC																				
GPIO9 NC																				
GPIO10 1:U1RXD		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

“R0 R1”, you can **change diff. R0 R1 combination** for diff. pull resistor value. Only special pad

Design Notice – Examples 1 (3/4)

GPIO Setting | GPO Setting | EINT Setting | PWM Setting | ADC Setting | KEYPAD Setting | PMIC Setting

	Def...	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	InPull En	InPull SelHigh	R0	R1	Def.Dir	In	Out	INV	Out.
GPIO9 0:GPIO9		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO10 0:GPIO10		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO11 0:GPIO11		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>								<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>		IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO12 0:GPIO12		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>		IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO13 0:GPIO13		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>		IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO14 0:GPIO14		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>		IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO15 0:GPIO15		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>		<input checked="" type="checkbox"/>		IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

In above example :

GPIO11 will be PU in input mode

GPIO12 will be Hi-Z in input mode

GPIO13 will be PU-36K Ohm in input mode

GPIO14 will be PU-1200K Ohm in input mode

GPIO15 will be PU-36K/1200K Ohm in input mode

special IO pad (with R0 R1 setting)

GPIO Setting | GPO Setting | EINT Setting | PWM Setting | ADC Setting | KEYPAD Setting | PMIC Setting

	Def...	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	InPull En	InPull SelHigh	R0	R1	Def.Dir	In	Out	INV	Out.
GPIO9 0:GPIO9		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO100:GPIO10		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO110:GPIO11		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO120:GPIO12		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO130:GPIO13		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>			<input checked="" type="checkbox"/>	IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO140:GPIO14		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>				IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
GPIO150:GPIO15		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>								<input checked="" type="checkbox"/>			<input checked="" type="checkbox"/>	IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

In above example :

GPIO11 will be PD in input mode

GPIO12 will be Hi-Z in input mode

GPIO13 will be PD-36K Ohm in input mode

GPIO14 will be PD-1200K Ohm in input mode

GPIO15 will be PD-36K/1200K Ohm in input mode

special IO pad (with R0 R1 setting)

Design Notice – Examples 2 (4/4)

	Def.Mode	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	InPu...	InPu...	R0	R1	Def.Dir	In	Out	INV	OutHigh
GPIO12 0:GPIO12	✓	✓	✓								✓					OUT	✓	✓		✓
GPIO13 0:GPIO13	✓	✓	✓								✓					OUT	✓	✓		✓
GPIO14 0:GPIO14	✓	✓	✓								✓					OUT	✓	✓		✓
GPIO15 0:GPIO15	✓	✓	✓								✓					OUT	✓	✓		✓

special IO pad (with R0 R1 setting)

In above example :

GPIO12 will be **High** in output mode

GPIO13 will be **Low** in output mode

GPIO14 will be **High** in output mode

GPIO15 will be **Low** in output mode

Design Notice – appendix

KCOL0-4(对应pin number为GPIO12~GPIO16):

InPull SelHigh	R1	R0	Weak Pull up/down state
打勾	0	0	Disable both resistors
打勾	0	1	PU-36K ohm
打勾	1	0	PU-1200K ohm
打勾	1	1	PU-36K//1200K ohm
不勾	0	0	Disable both resistors
不勾	0	1	PD-36K ohm
不勾	1	0	PD-1200K ohm
不勾	1	1	PD-36K//1200K ohm

KROW0-4((对应pin number为GPIO17~GPIO21)):

InPull SelHigh	R1	R0	Weak Pull up/down state
打勾	0	0	Disable both resistors
打勾	0	1	PU-36K ohm
打勾	1	0	PU-1K ohm
打勾	1	1	PU-36K//1K ohm
不勾	0	0	Disable both resistors
不勾	0	1	PD-36K ohm
不勾	1	0	PD-1K ohm
不勾	1	1	PD-36K//1K ohm

Design Notice – appendix

URXD:

CMPDN/CMCSD0/CMCSD1/CMMCLK
MCCK/MCCM0/MCDA0/MCDA1/MCDA2/MCDA3
LSRSTB/LSCE_B/LSCK/LSDA/LSA0/LPTE
RESETB

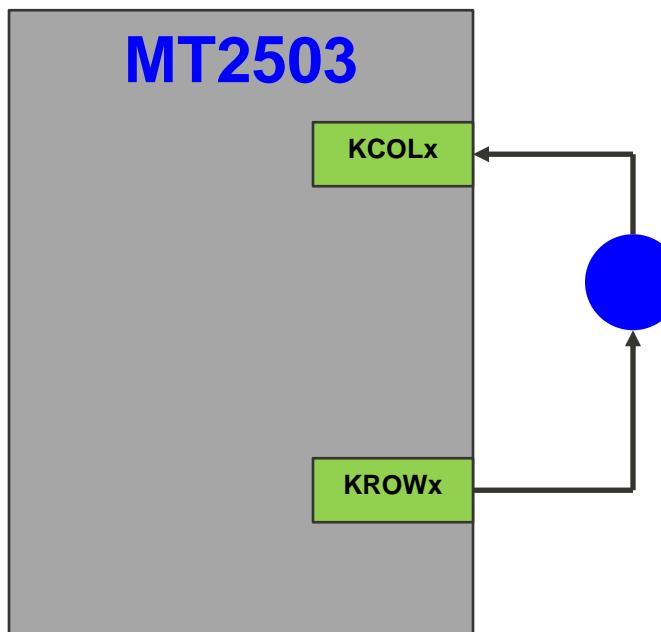
InPull SelHigh	R1	R0	Weak Pull up/down state
打勾	0	0	Disable both resistors
打勾	0	1	PU-47K ohm
打勾	1	0	PU-47K ohm
打勾	1	1	PU-23.5K ohm
不勾	0	0	Disable both resistors
不勾	0	1	PD-47K ohm
不勾	1	0	PD-47K ohm
不勾	1	1	PD-23.5K ohm

MT2503_Baseband keypad

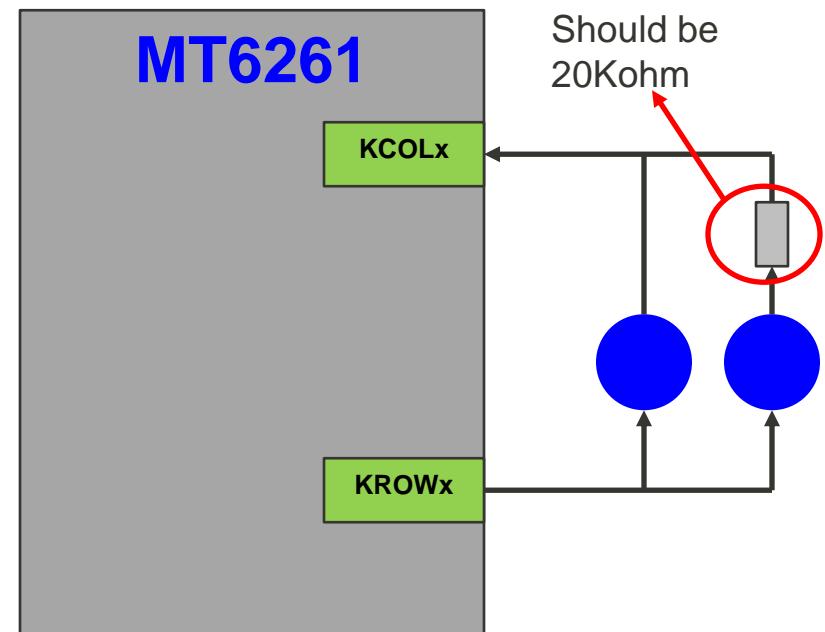
Keypad design notes (HW)

- MT2503 is not suitable for extend keypad design, please design traditional keypad in MT2503

Traditional key pad



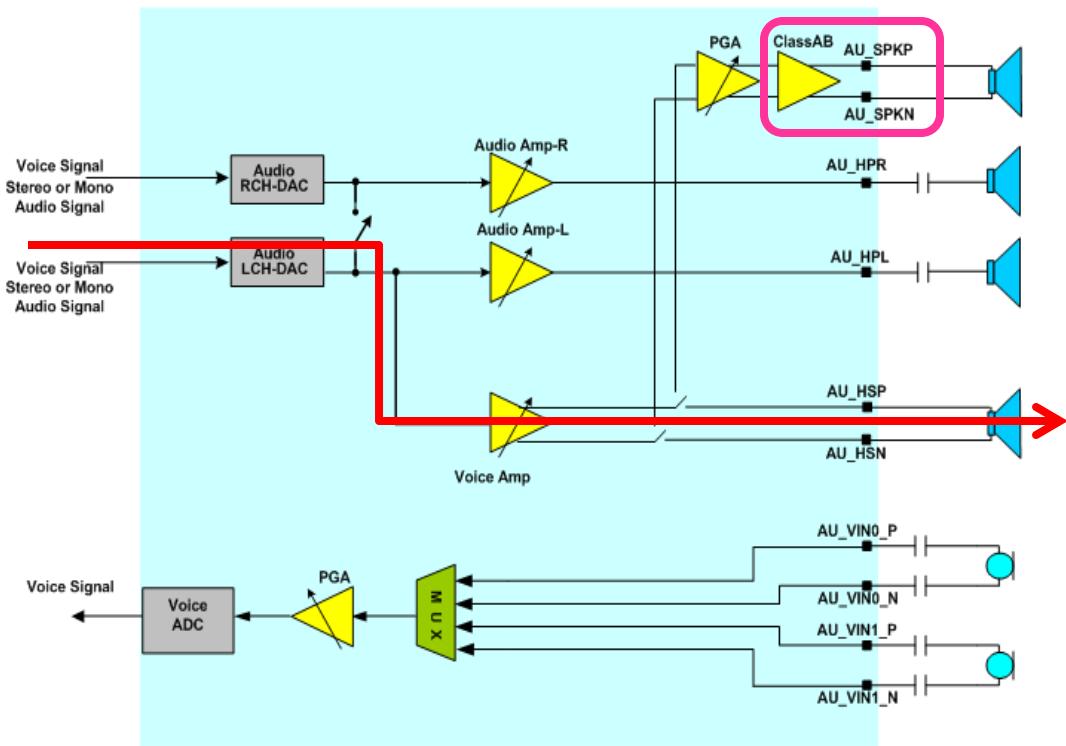
Extend keypad
(not suitable for MT2503)



MT2503_Baseband Audio/Speech

Design Notice – Audio & Speech

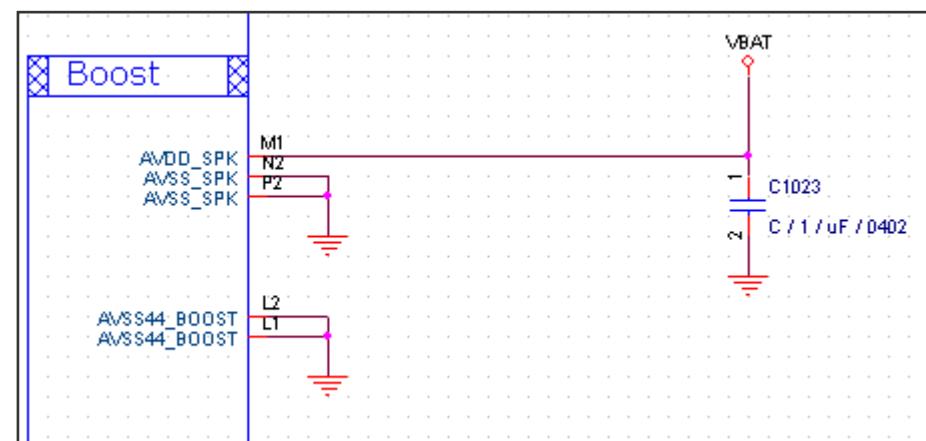
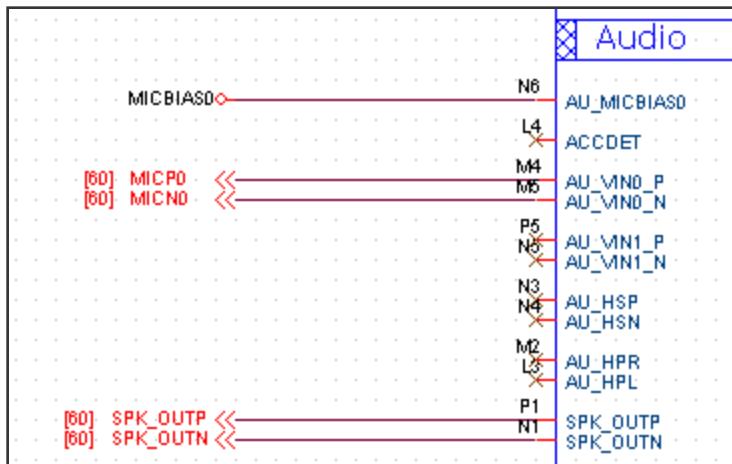
AFE structure of MT2503 DL and UL path



1. Voice buffer and speaker signal path
 - MT2503 voice buffer is share with MP3_L channel DAC
2. MT2503 Speaker amp support class AB

Design Notice – Audio & Speech

- NC the corresponding pin if the function is unused.
- AVDD_SPK (M1) internal audio power must connect to VBAT, cannot NC.
- External audio amp input signal can be supplied by AU_HPL.
- Internal class-AB amp can drive 2-in-1 speaker



Design Notice – Audio & Speech

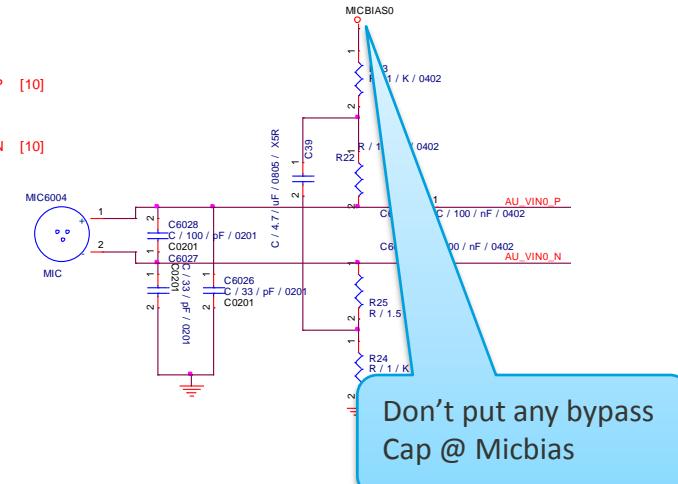
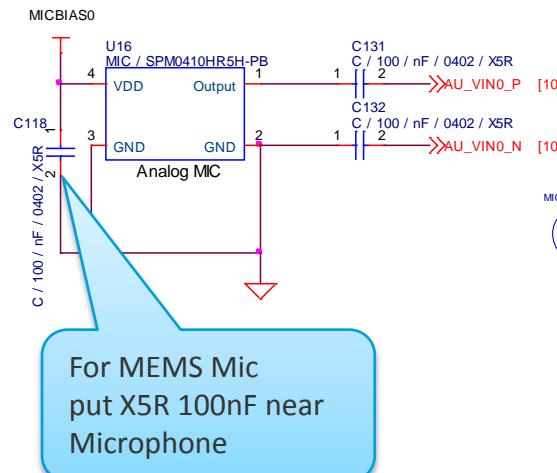
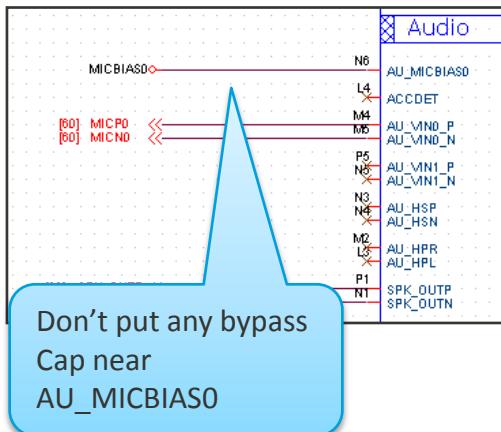
▪ Gain table of MT2503

		MT2503
AC/ DC coupled		AC coupled
MIC	Gain range (dB)	-20 ~ +43
	Gain per step	1dB / 4
	Engineer mode range	0 ~ 252
	MicBias	1 ball
Voice buffer	Gain range (dB)	-22 ~ 8 dB
	Gain per step	2dB/16
	Engineer mode range	0 ~ 240
Audio buffer	Gain range (dB)	-29 ~ 11 dB
	Gain per step	2dB / 8
	Engineer mode range	0 ~ 160
SPK AMP	AMP Type	Class-AB
	Gain range (dB)	-6 / 6 / 12dB
	Output power @ 3.7V, 8ohm, 1% THD	0.8W
I2S	Master Input	V
	Master Output	V
	Slave Input	X
	Slave Output	X

Design Notice – Audio & Speech

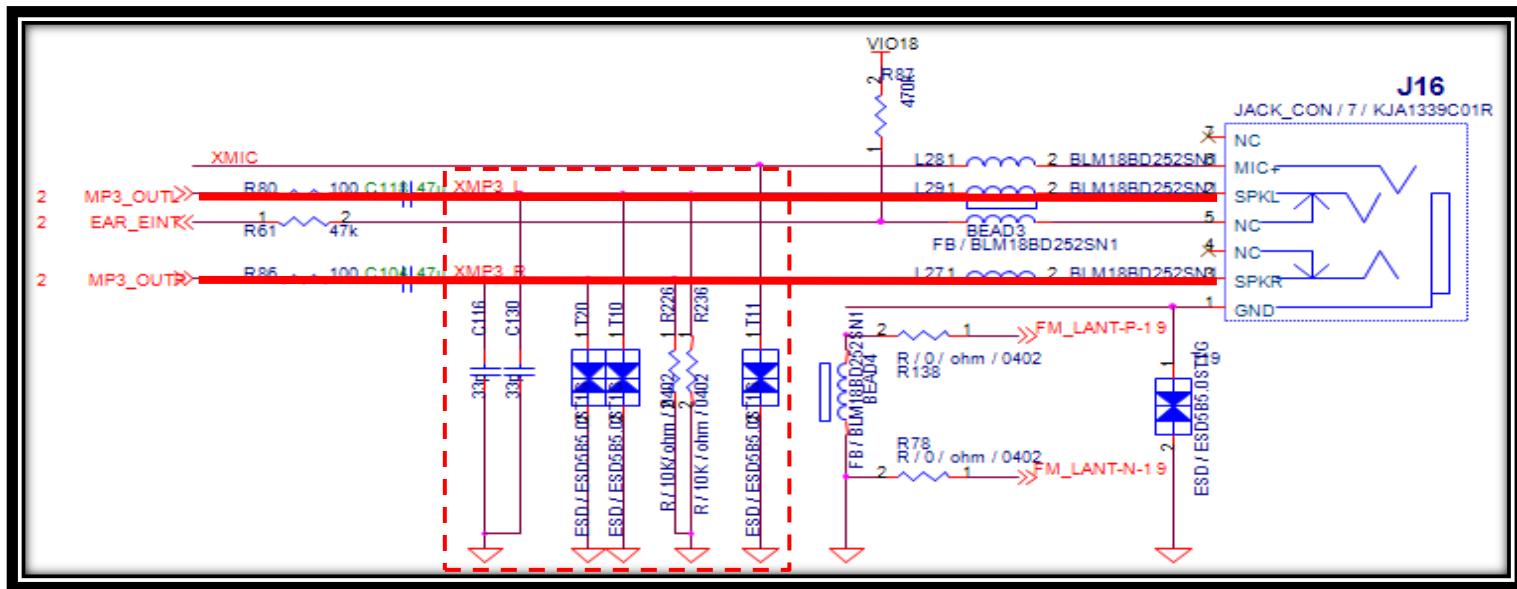
AU_MICBIAS0 bypass cap range

Mic type	MEMS Mic	ECM Mic
Application (Total Capacitor @ AU_MICBIAS0)	X5R 100nF near microphone	Don't put any cap
Allowed total Capacitance Range (include Cap tolerance)	50nF~150nF	Less than 0.1nF



Design Notice – Audio & Speech

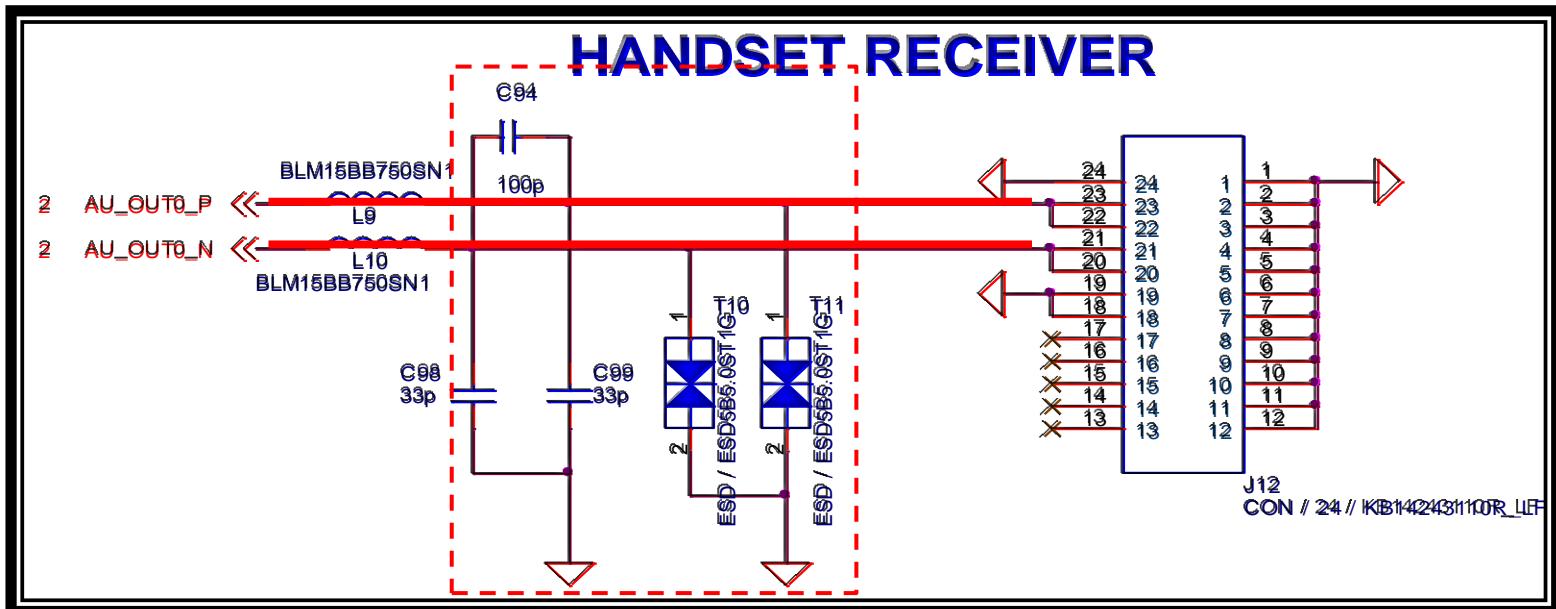
- The **MAXIMUM** allowable **Cap load** at AU_HPR and AU_HPL (**audio buffer**) should be **smaller than 250pF**
 - The cap of the **ESD** component and **Cap** for **TDD** noise should be counted in
 - Caution:** The HPR/ HPL is **not used** for FM antenna any more



Design Notice – Audio & Speech

- The **MAXIMUM** allowable **Cap load** between AU_HSP and AU_HSN (**voice buffer**) should be **SMALL** than **250pF**
 - The cap of the **ESD** component and **Cap** for **TDD** noise should be counted in

Total Cap load between HSP/ HSN = C94 + (C98 + C99 + T10 + T11) / 2

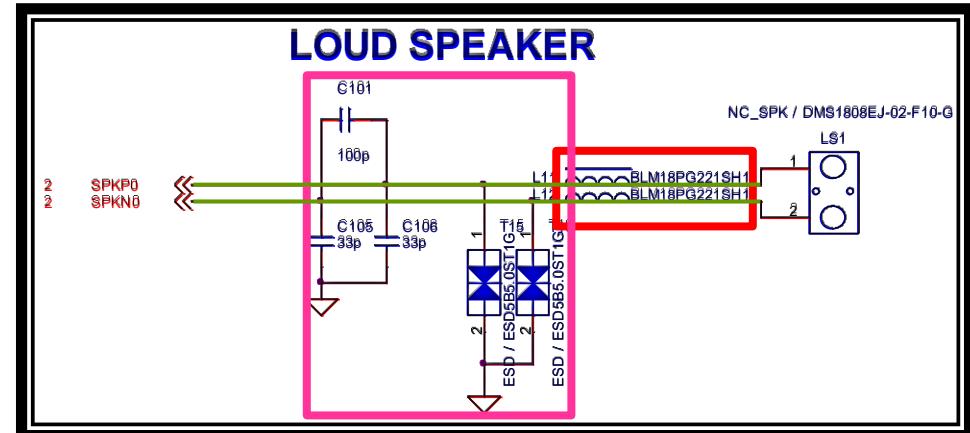


Design Notice – Audio & Speech

Internal Audio Amplifier

- Schematic and layout suggestion
 - Bead with **power line spec** is recommend for **EMI/EMS** purpose
 - The **MAXIMUM** allowable **Cap load between SPK_OUTP/SPK_OUTN** should be **SMALL** than **330pF**
 - The **ratio** of Length over width (**L/W**) should be less than **100** to min. the **trace LOSS**, and should be routed in **DIFF. PAIR** and **SHIELD** by GND

Vendor	P/N	Rdc(ohm)	Rate current(mA)
Murata	BLM18PG221SH1	0.1	1400
	BLM15PD800SN1	0.07	1500
	BLM18KG221SN1	0.05	2200
	BLM18KG331SN1	0.08	1700
	BLM18SG221TN1	0.04	2500
	BLM18SG331TN1	0.07	1500
	BLM18EG221SN1	0.05	2000
TDK	MPZ1608S221A	0.05	2200
	MPZ1608S331A	0.08	1700
	MPZ1608Y221B	0.1	1500

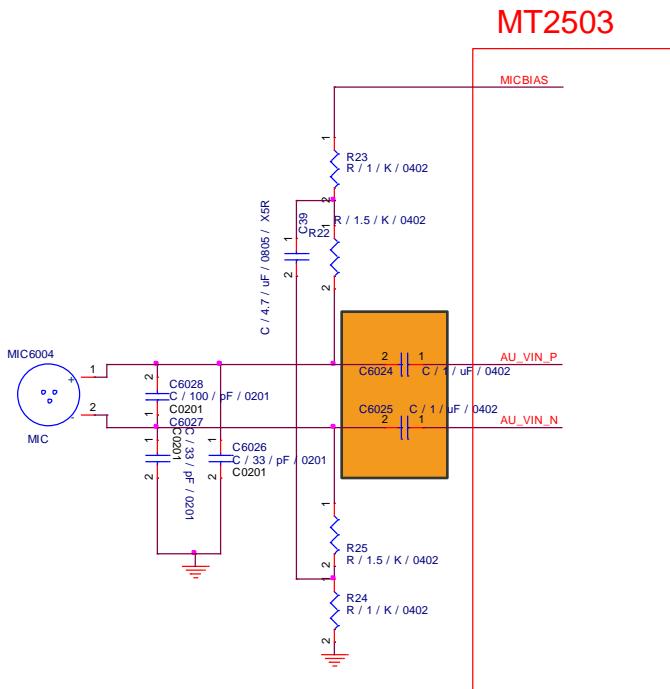


Mic Configuration

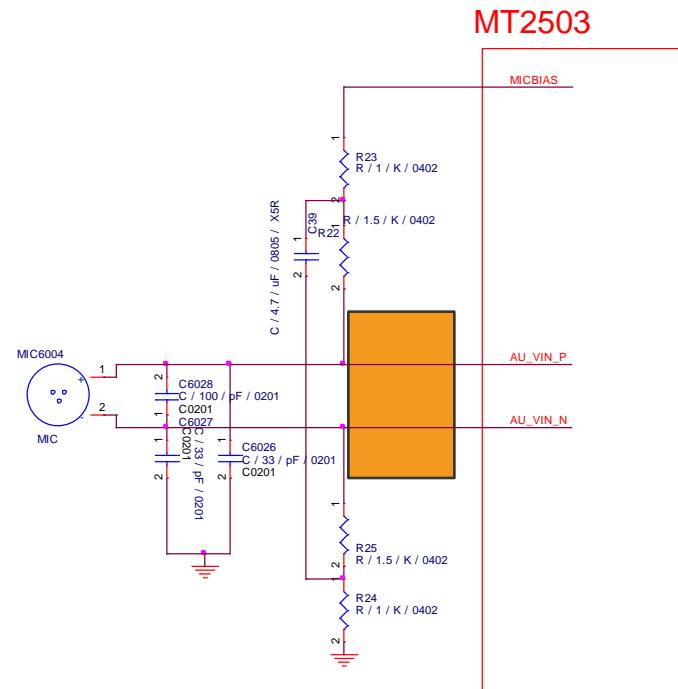
- Traditional (ACC) mode / Low cost mode mic selection
 - \custom\audio\project_BB\audcoeff.c
 - Main mic
 - const unsigned char mic0_type_sel = 0;
 - 0:Traditional mode (Performance similar to MT6261)
 - 1:Low cost mode (Noise level increase a little than Traditional mode)
 - Earphone mic
 - const unsigned char mic1_type_sel = 0;
 - 0:Traditional mode (Performance similar to MT6261)
 - 1:Low cost mode (Noise level increase a little than Traditional mode)
 - Build command: m c,r custom audio

Application Schematic Normal mode - ECM Mic

Traditional mode



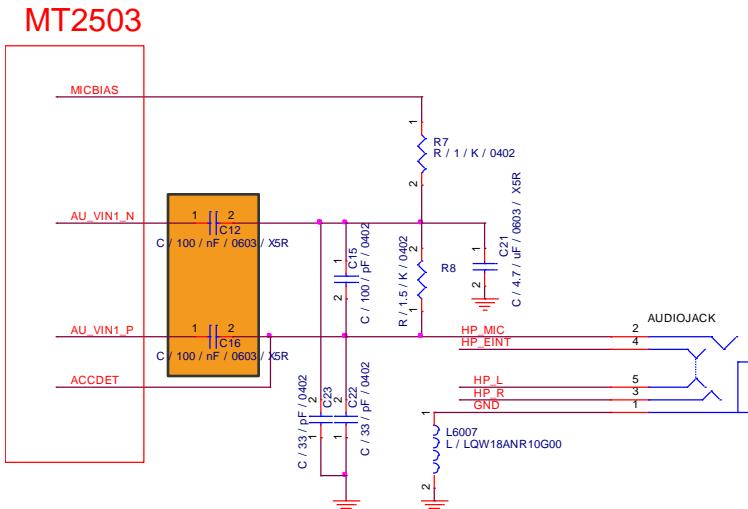
Low cost mode



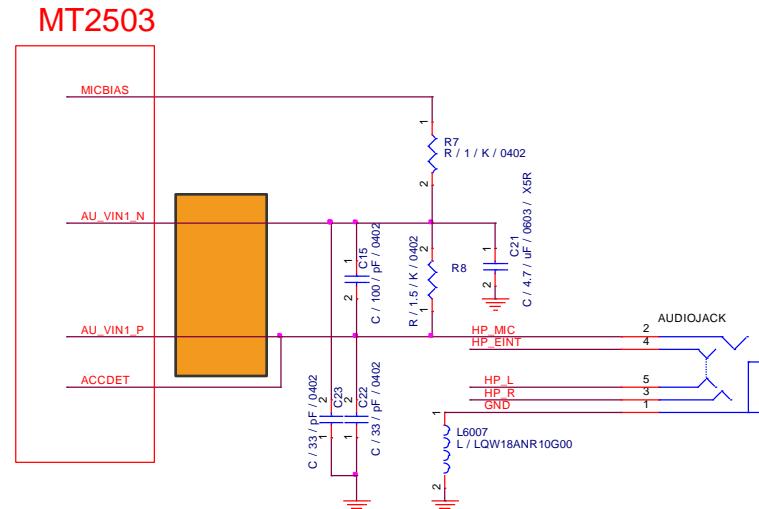
Could short the DC Block Capacitor for cost saving

Application Schematic Headset mode

Traditional mode



Low cost mode



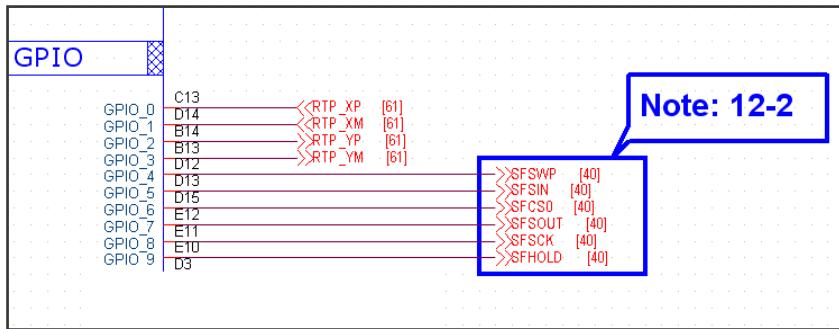
Could short the DC Block Capacitor for cost saving

MT2503_Baseband Serial Flash

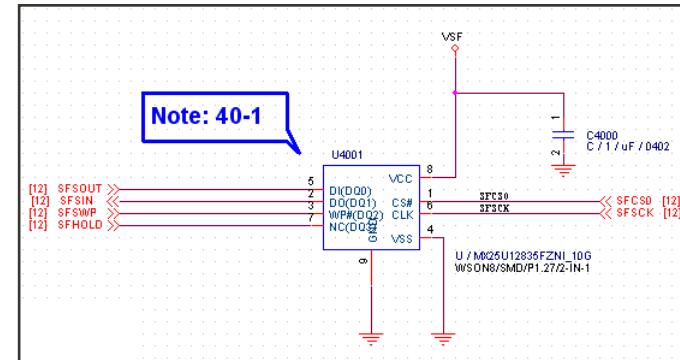
Design Notice – SFI (1/5)

- For MT2503A , external serial flash is required.
- SFI schematic:
 - Only support one serial flash.
 - Please connect SF pins according to SF interface table.

SFI controller.



Serial flash device.



SF interface table:

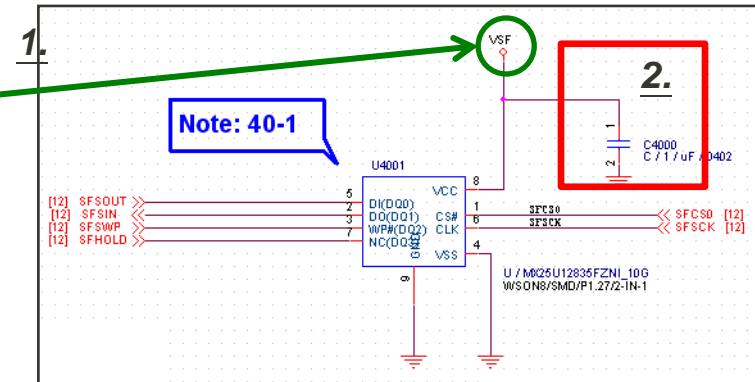
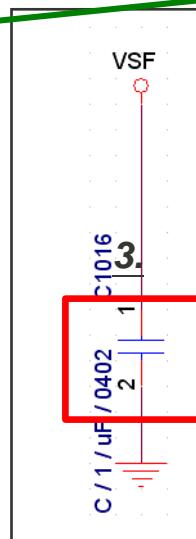
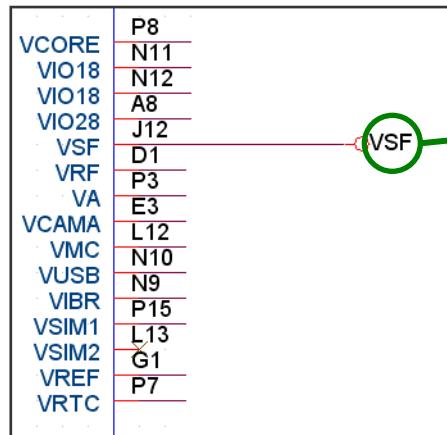
	MT2503	Serial flash
Interface	SFSOUT	SQI_DI
	SFCS0	SQI_CS#
	SFSIN	SQI_DO
	SFSCK	SQI_CLK
	SFHOLD	SQI_HOLD
	SFSWP	SQI_WP#

Design Notice – SFI (2/5)

SFI schematic:

1. The power domain of serial flash device is SF
 2. 1uF capacitor must be placed **as close to serial flash device as possible.**
 3. 1uF capacitor must be placed **as close to VSF_LDO as possible.**
- ※ MT2503 support 3V and 1.8V serial flash. VSF output 3V or 1V8 by using HW trapping pin(LSA0).

PMU
output



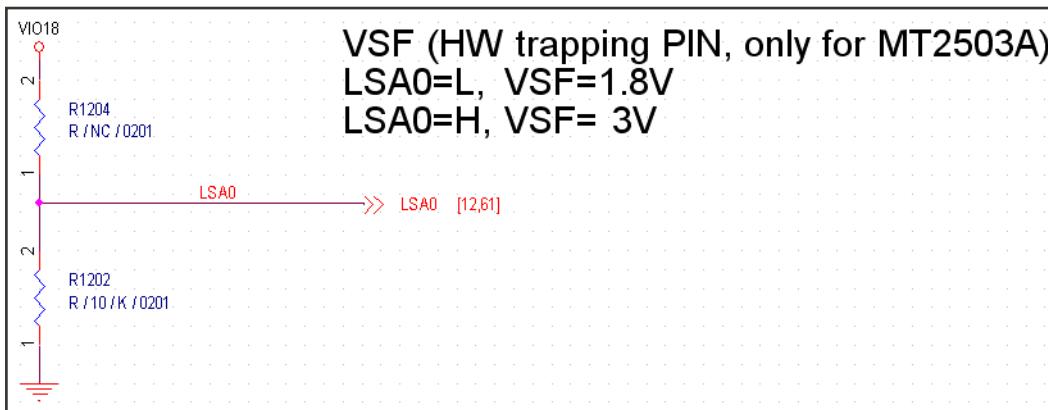
1uF cap close to
serial flash.

1uF cap close to
VSF_LDO.

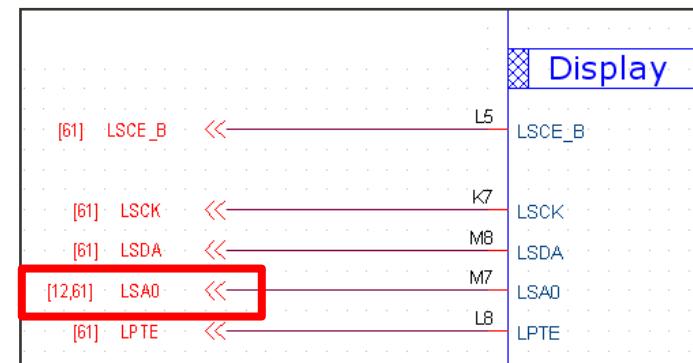
Design Notice – SFI (3/5)

4. If using 3V serial flash, please trap LSA0 pin to VIO18 with pull up resistor (10K ohm) and Vsf will output 3V.
5. If using 1.8V serial flash, please trap LSA0 pin to GND with pull low resistor (10K ohm) and Vsf will output 1.8V.

	LSA0 pin	VSFoutput	Device support
<u>4.</u>	Pull high	3V	3V serial flash device
<u>5.</u>	Pull low	1.8V	1.8V serial flash device



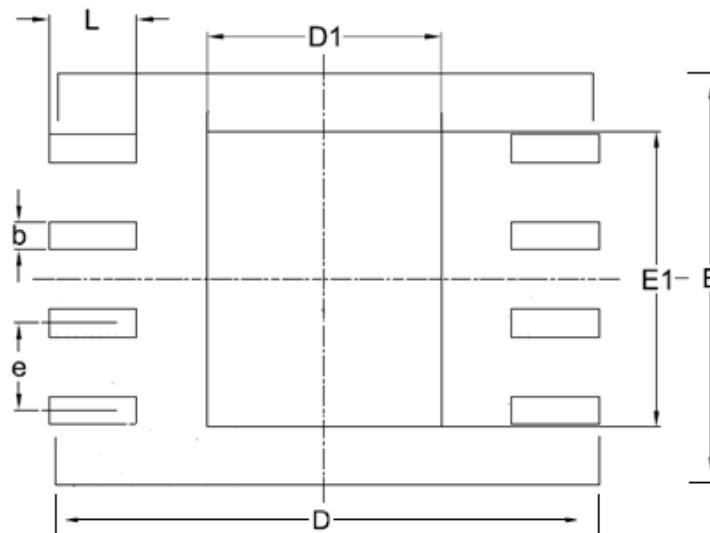
HW trapping pin: LSA0 pin



Design Notice – SFI (4/5)

- **Compatible footprint**

To compatible with WSON 5*6, TSOP and WSON 8*6 with reduced central pad package, please use the recommended footprint as below.

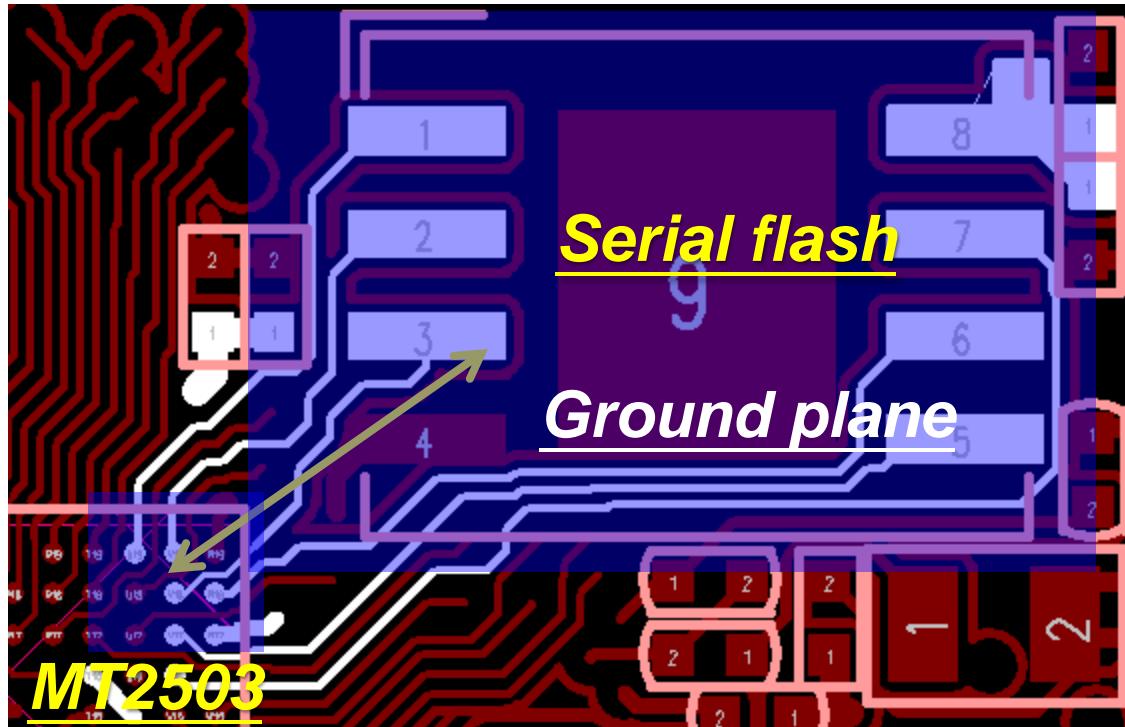


Symbol	D	E	D1	E1	b	e	L
Unit: mm	8.00	6.00	3.40	4.30	0.60	1.27	1.95

※ Note : When you're using serial flash with WSON 8*6 package, please confirm with vendor if it is reduced central pad version.

Design Notice – SFI (5/5)

- Serial flash device should be placed **as close to MT2503 as possible**.
- All traces of serial flash device **should be routed in the same layer**.
- There should be a ground plane beneath the serial flash device and QPI traces of MT2503. (**Nice to have**)

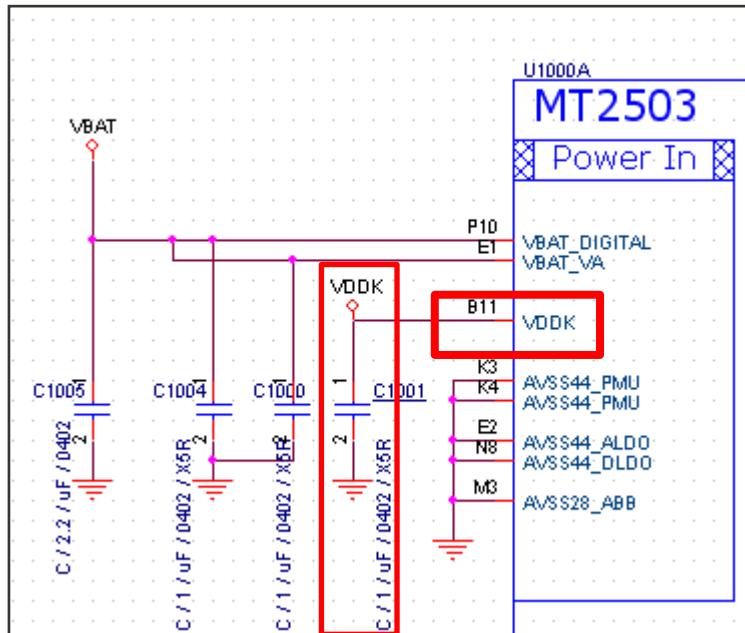


EMI design notice

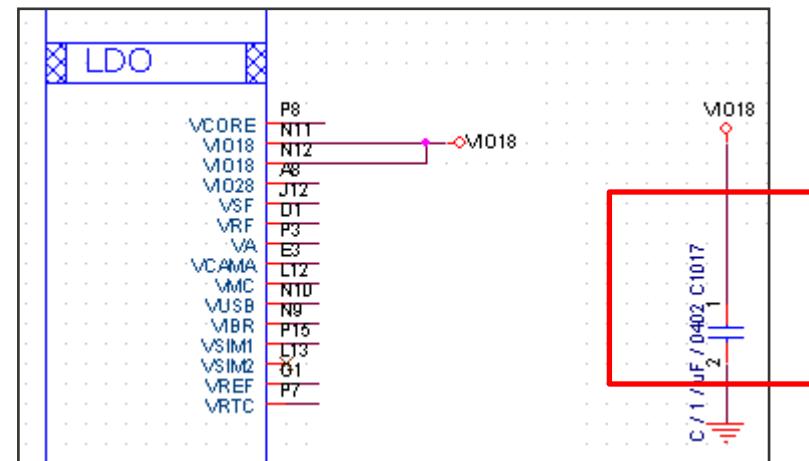
■ EMI schematic:

1. The power source for Internal PSRAM is VDDK & VIO18.
2. 1uF capacitor for VDDK must be placed as close to BB chip as possible.
3. 1uF capacitor for VIO18 must be placed as close to BB chip as possible.

1. Internal PSRAM power source



2. 1uF cap close to BB



3. 1uF cap close to BB

MT2503_Baseband LCM

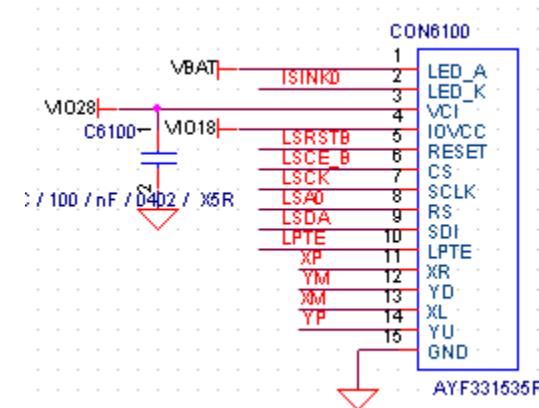
LCM Design Note – Overview

- Display Resolution
 - Support up to QVGA (Serial)(320*240)
- Interface
 - Supports serial 3/4 wire SPI interface
 - Dedicate serial 1.8 LCM interface
- IO Power
 - Support 1.8V IO level LCM – IO Power domain is VIO18

LCM Design Note – Serial Interface

- LCM LPTE(FMARK/F_Sync), please connect to BB LPTE(pin L8) for reserve
- SW default Close TE function, so if you have HW connect , please open TE function(SYNC_LCM_SUPPORT =True)

MT2503 (Pin definition)		LCM side
LSDA	M8	SDI
LSA0	M7	RS
LSCK	K7	SCLK
LRSTB	M14 (SIM2_SRST)	RESET
LSCE_B	L5	CS
LPTE	L8	FMARK / F_Sync



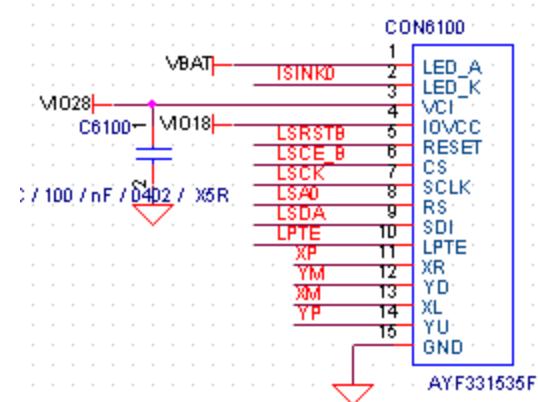
Layout Notice – SPI Interface

▪ Placement

- LCM analog power (VCI) bypass cap should be close to LCM
- LCM IO power (IOVDD) bypass cap should be close to LCM
- EMI filter used for LCM control signal or databus capacitor loading suggest under 30pF

▪ Layout

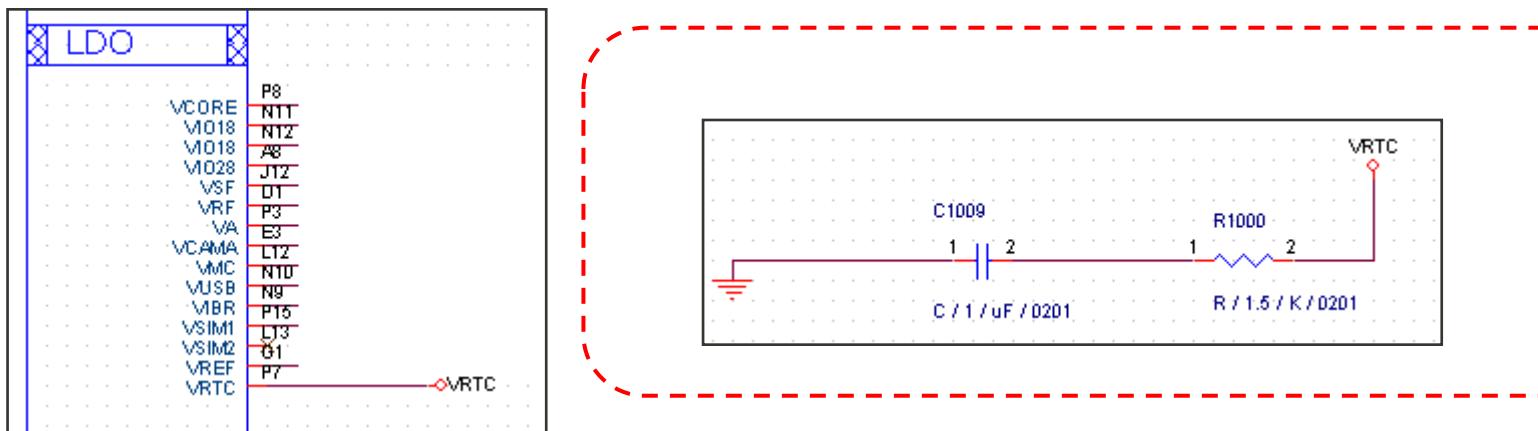
- SPI signal should be shielded by GND
- Backlight Power trace (ISINK) keep at least 6mil over



MT2503_Baseband RTC

Design Notice – RTC

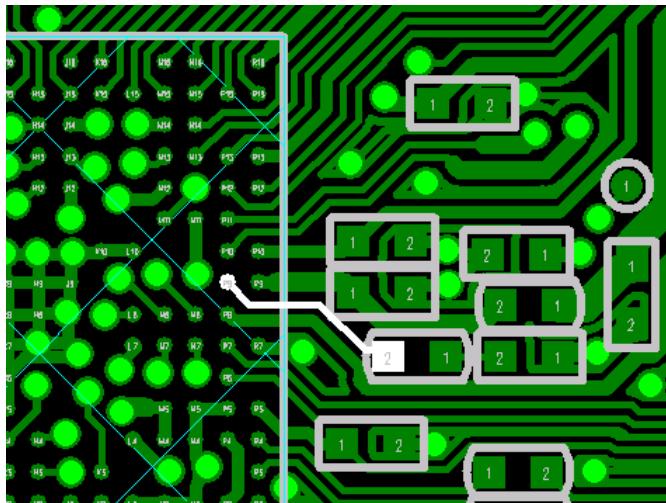
- SCH design notes



★ Recommend implementing 0~100uF or back up battery for VRTC.

Design Notice – RTC

- PCB design notes



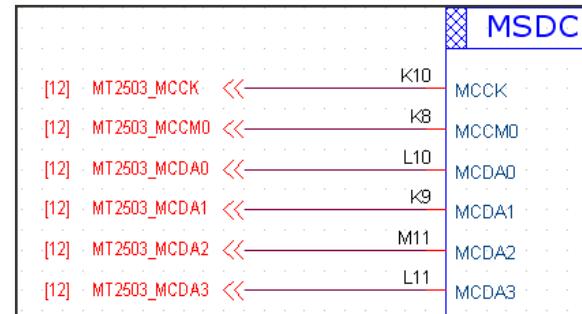
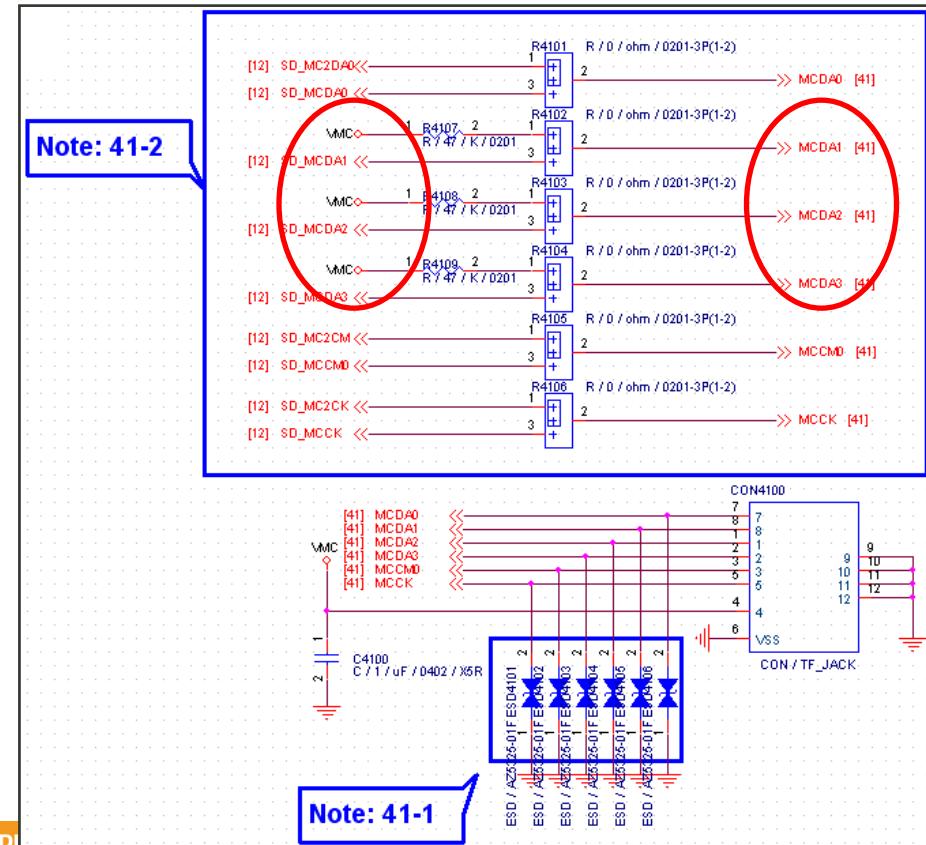
VRTC trace 4mil

MT2503_Baseband SD Card

MSDC HW Configuration

1. Provide 3.3V to SD card
2. CMD and Data chip internally provide pull-up resistor, 47K(default) and 23.5K.
3. When use 1 bit mode, please pull up the DA1~DA3 to VMC with 47K.

Pull up DA1~DA3 to VMC with 47K when use 1 bit mode



MSDC Layout Guidelines

1. DAT, CMD, CLK in a group
2. If this criteria can not be followed , the priority is ((DAT + CLK) + CMD)
3. If the ESD protection is needed, reserve ESD protection device on CMD/CLK/DAT/MCINS with Cap < 15pF
4. CLK must be grounded in both sides to reduce interference
5. Keep total trace length < 100mm
6. Keep trace difference of DAT, CMD, CLK to be < 500mil

MT2503_Baseband Camera

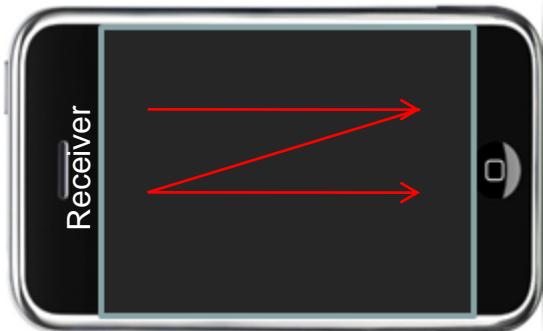
Serial Sensor Interface

- Support to 0.3M
- Support 1Lane / 2Lane / 3Lane mode and DDR Mode

BB Chip (Pin definition)	Camera side
CMMCLK	Master Clock
CMCSD0 (CMDATA0)	SPI Output - Data 0 (SPI 1-wire mode)
CMCSD1 (CMDATA1)	SPI Output - Data 1 (SPI 2-wire mode)
CMCSK (CMPCLK)	SPI Clock Output
SDA	I2C Data line
SCL	I2C Clock line
CMRST	Reset
CMPDN	Power down

Camera Module Capture Direction(1/2)

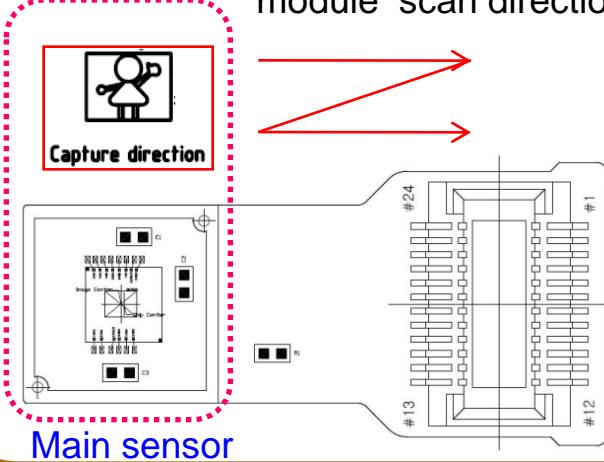
Screen's scan direction



Receiver



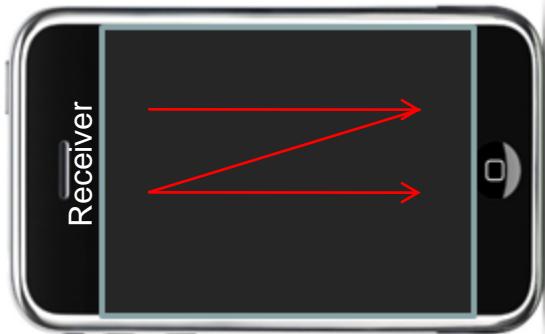
Rear facing camera module scan direction



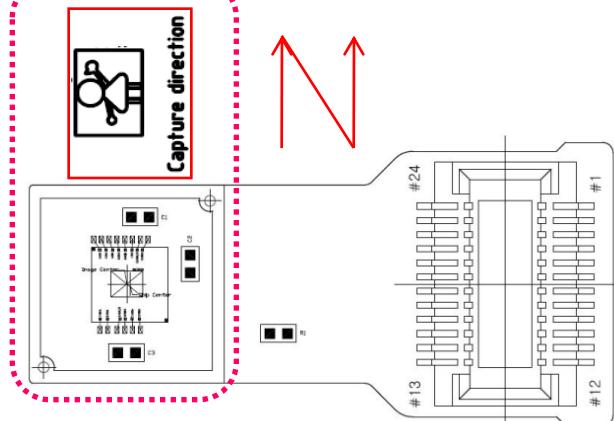
Both front- and rear-facing cameras, if present, MUST be oriented so that the long dimension of the camera aligns with the screen's long dimension.

Camera Module Capture Direction(2/2)

Screen's scan direction



Rear facing camera module scan direction



Camera Reference Circuit

- Camera GPIO PIN Mux: Two sets camera interface.
 - Default GPIO25~GPIO30
 - GPIO0~3, GPIO10,11 reserved for DAI usage.

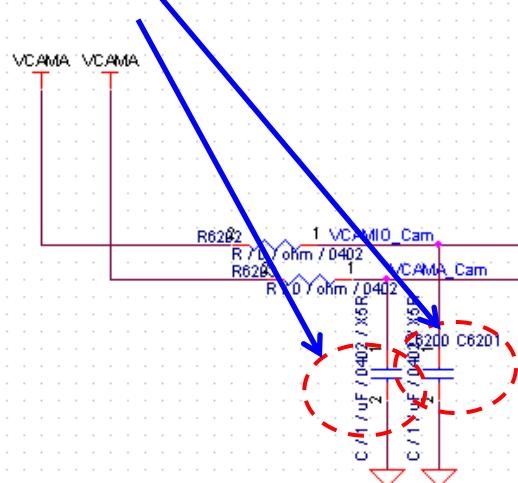
Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
GPIO25	CMRST	LSRSTB	CLKO1	EINT15	FMJTDI
GPIO26	CMPDN	LSCK1	DAICLK (2.8v)	SPI_CK	FMJTMS
GPIO27	CMCSD0	LSCE_B1	DAIPCMIN(2.8v)	SPI_SCK	FMJTCK
GPIO28	CMCSD1	LSDA1	DAIPCMOUT (2.8v)	SPI_MOSI	FMJTRSTB
GPIO29	CMMCLK	LSA0DA1	DAISYNC (2.8v)	SPI_MISO	FMJTDO
GPIO30	CMCSK	LPTE	CMCSD2	EINT16	

Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
GPIO0	EINT0	XP	URXD3	CMCSD2	CMCSK
GPIO1	EINT1	XM	UTXD3	UART1_CTS	CMMCLK
GPIO2	EINT2	YP	GPSFSYNC	PWM0(2.8v)	CMCSD0
GPIO3	MCINS	YM		PWM1(2.8v)	CMCSD1
GPIO10	URXD1	CMRST	EINT9	MCINS	
GPIO11	UTXD1	CMPDN	EINT10		

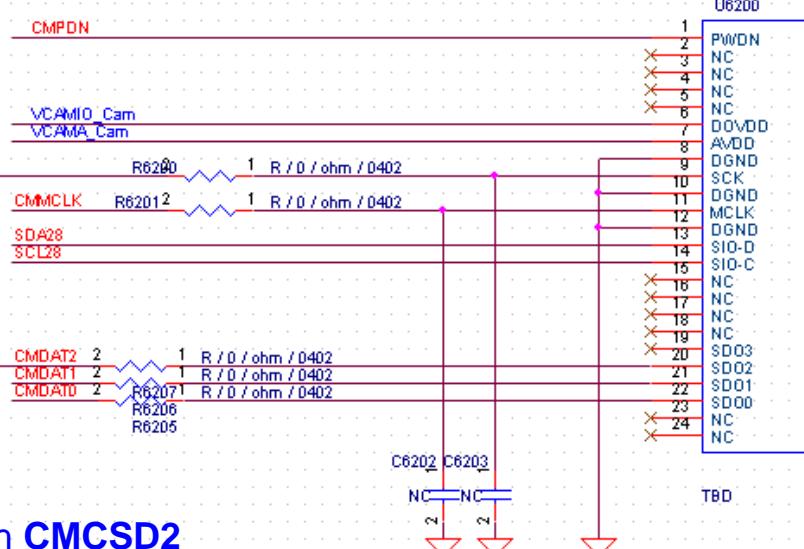
Camera Reference Circuit

Must be reserved de-couple caps and placed near by connector

Camera Interface fix 2.8V



CMCSK (CMPCLK) Pin-MUX with CMCSD2 (CMDATA0) in 3-Lane Mode



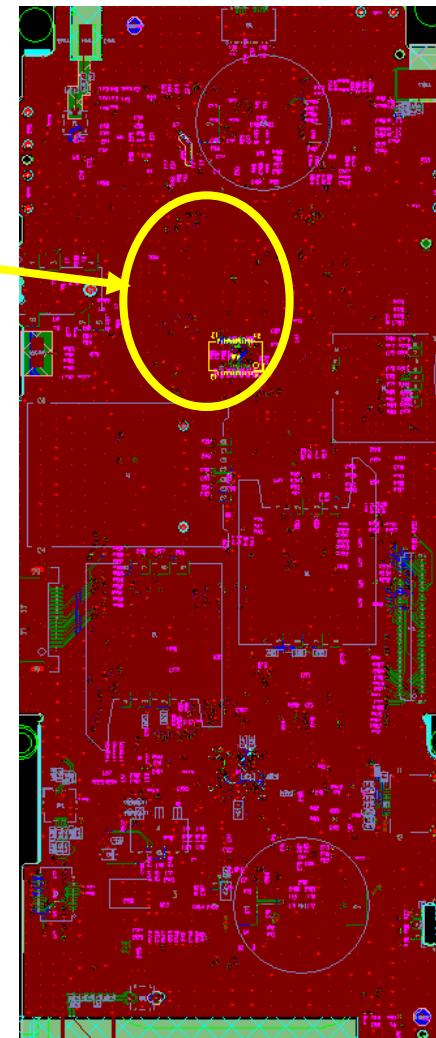
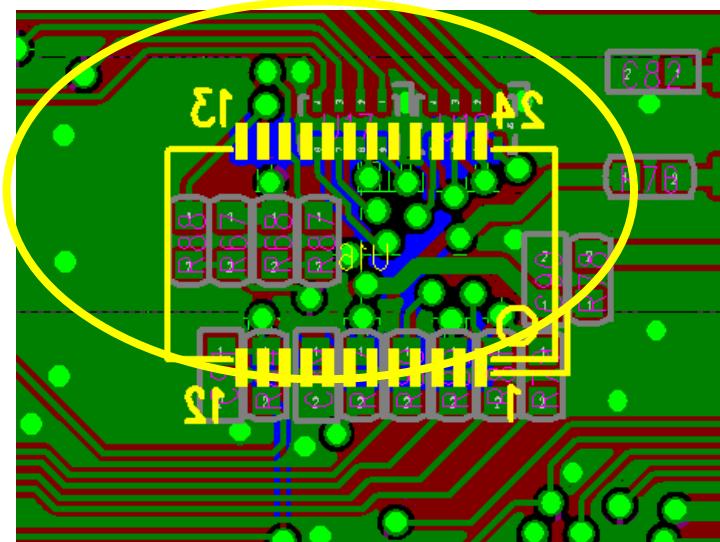
Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
GPIO0	EINT0	XP	URXD3	CMCSD2	CMCSK
GPIO30	CMCSK	LPTE	CMCSD2	EINT16	

Camera Reference Circuit

- PCB Component Placement recommend :

➤ To minimize RF radiation interference, **do not place the sensor module near or beneath the antenna.**

➤ The sensor module's power supplies(inductors , beads , resistors , capacitors) should be placed as close as possible to the connect



Serial Camera sensor

- **Serial Image Sensor Interface :**

The Image Sensor interface is divided up into three groups summarized in below that each group has special routing guidelines. The interconnecting lengths in the controller package should be calculated for the length matching.

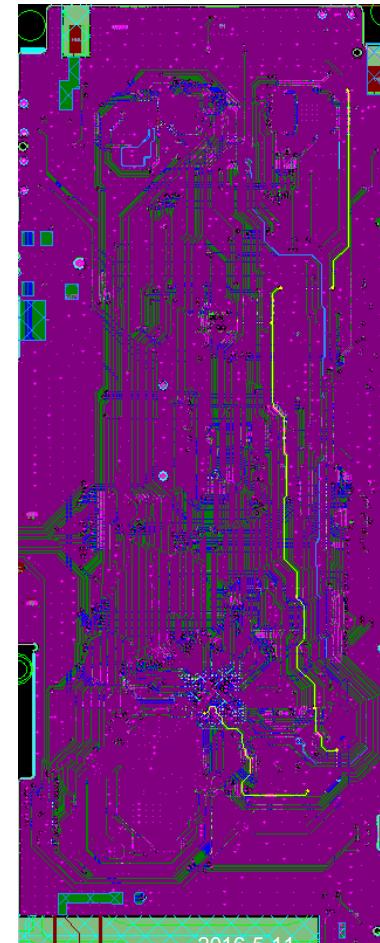
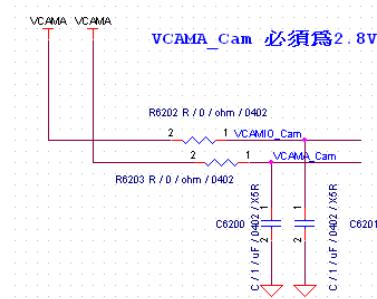
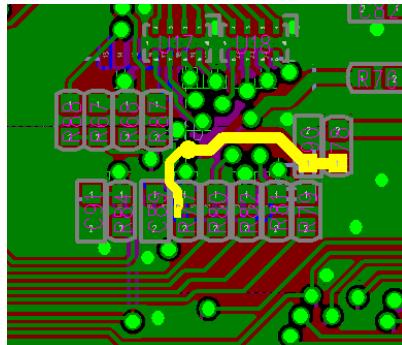
Group	Signal Name	Description
SPI	SDO (CMCSD0) SCK (CMCSK)	Image sensor SPI data output Image sensor SPI CLK output clock shall be routed surround with ground plane (high priority)
Clock	MCLK	Image sensor master clock output clock shall be routed surround with ground plane (high priority)
Control	SCL SDA CMPDN	I2C clock output I2C data input/output Image sensor PDN signal output

Camera power (1/2)

- **Analog Power Routing (Must be!!)**

This section states the layout recommendations for the image sensor Analog power routing. Refer to below table for the routing guidelines. **Analog Power shall be routed surround with ground plane.**

Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Analog Power)	$W \geq 12\text{-mil}$, $S = 4\text{-mil}$ with GND trace.
Remark	<p>Analog power must be routed surround with ground plan.</p> <p>De-couple cap shall connect to main ground directly.</p>

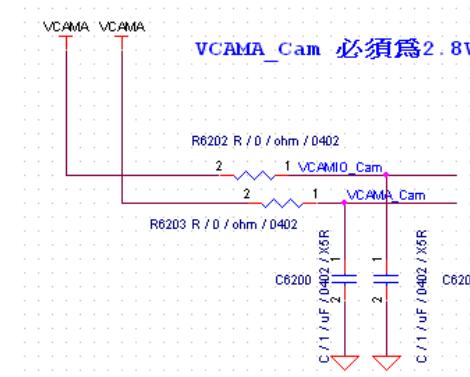
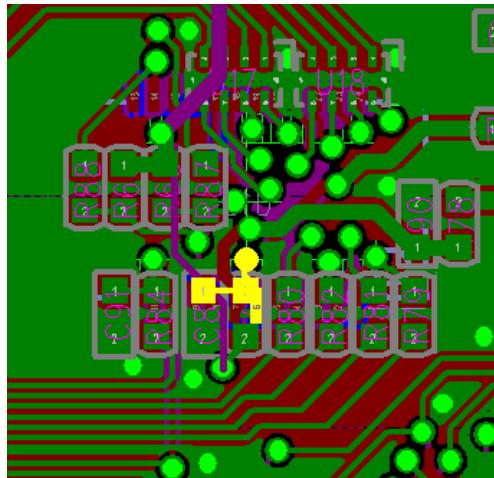


Camera power (2/2)

● Digital Power Routing (Nice to have)

This section states the layout recommendations for the image sensor digital power routing. Refer to below table for the routing guidelines. Digital Power shall be routed surround with ground plane.

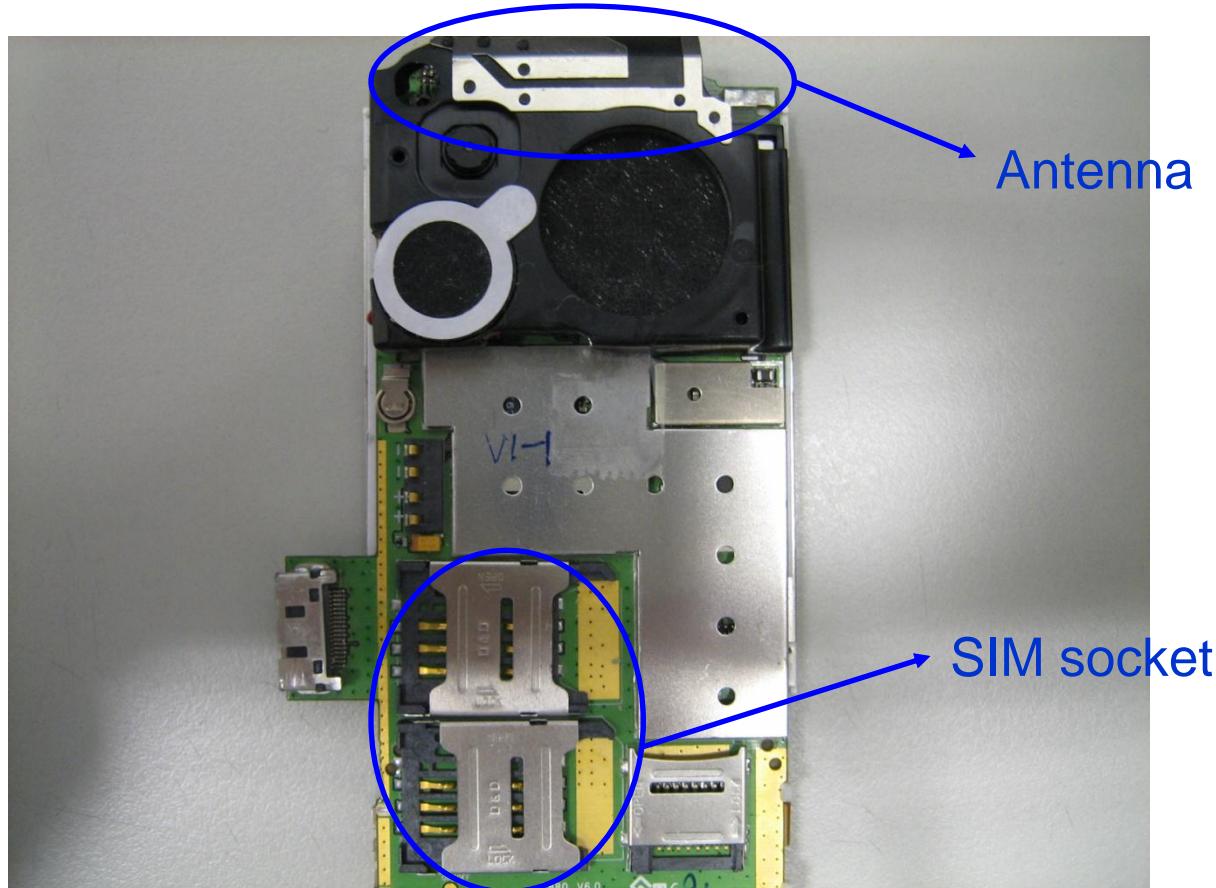
Parameter	Routing Guideline
Reference plane	Route microstrip over unbroken ground or power plane.
Main trace patterns (Digital Power)	$W \geq 12\text{-mil}$, $S = 4\text{-mil}$ with GND trace.
Remark	Digital power shall be routed surround with ground plan. De-couple cap shall connect to main ground directly.



MT2503_Baseband SIM Card

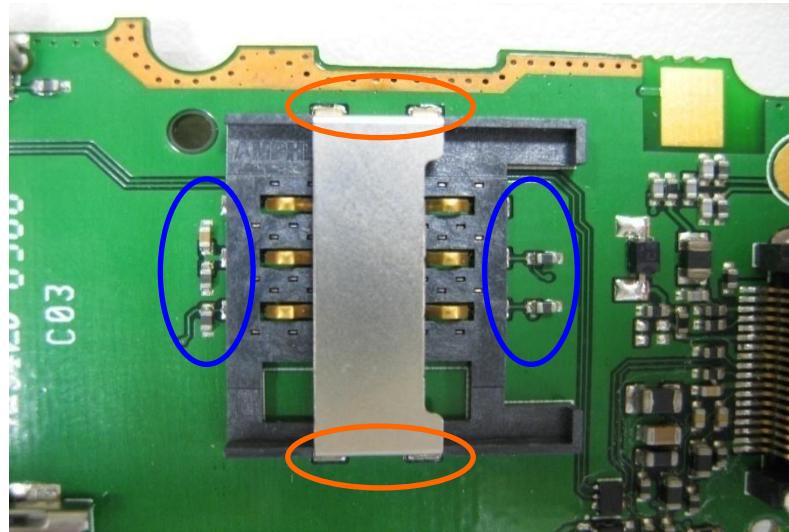
Case study 1

- Mechanical component
 - Place the SIM socket as **far away** from the antenna as possible.



Case study 2

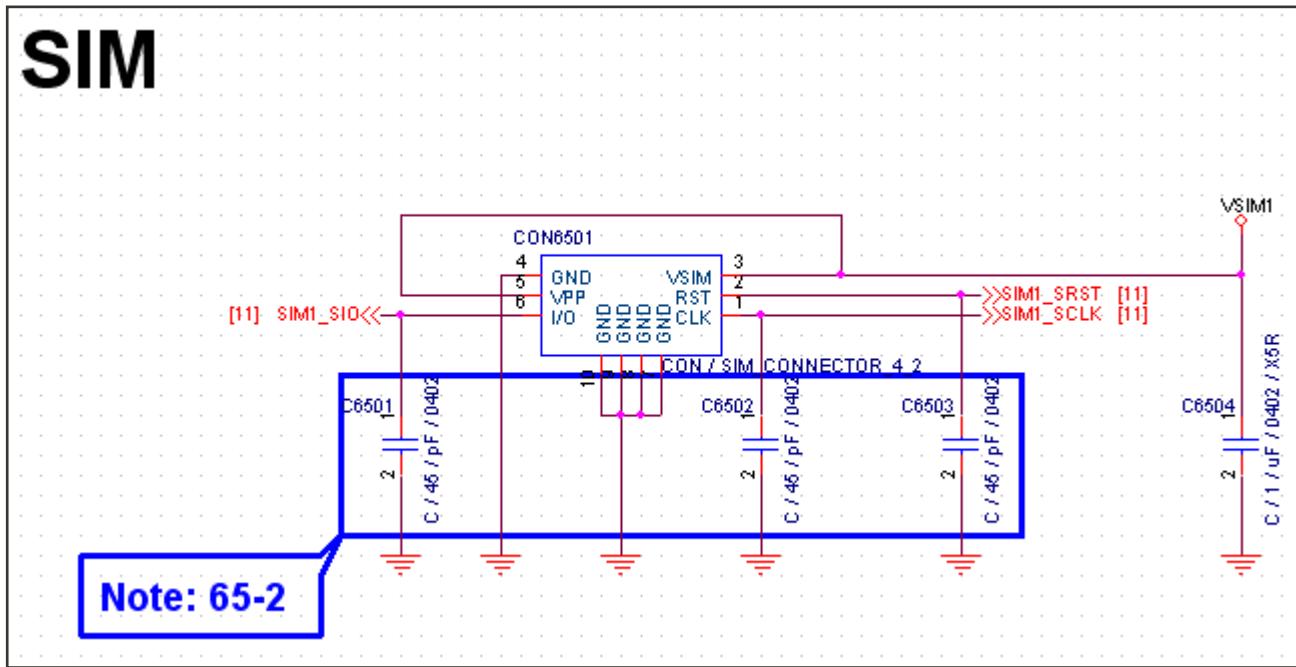
- Mechanical component
 - SIM socket must be grounded well.



- The metal plates of the SIM socket have better grounding using the **attaching points** on the top/bottom.
- The **capacitors** should be placed close to the pins.

SIM layout(1/2)

- VSIM bypass cap is 1uF.
- Caps in Note 65-2 are optional for better RF de-sense performance (C load on trace <45pF).



SIM layout(2/2)

- The capacitor should be placed as close as possible to the VSIM pins.
- VSIM width is 8mil at least.
- SIM_CLK trace is far from other traces 8mil. It is better to shield it from GND if possible.
- For SIM IF, the equivalent capacitor must be under 60pF.
- SIM_CLK is not close to SIM_IO to avoid cross talk.

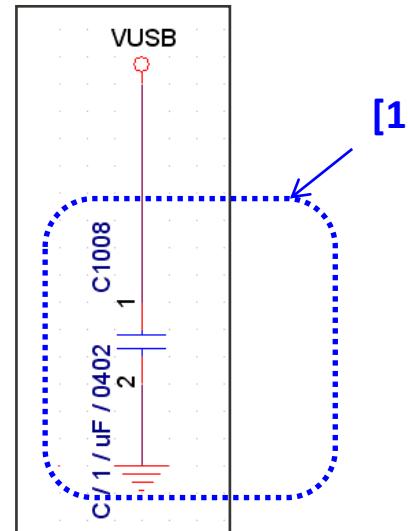
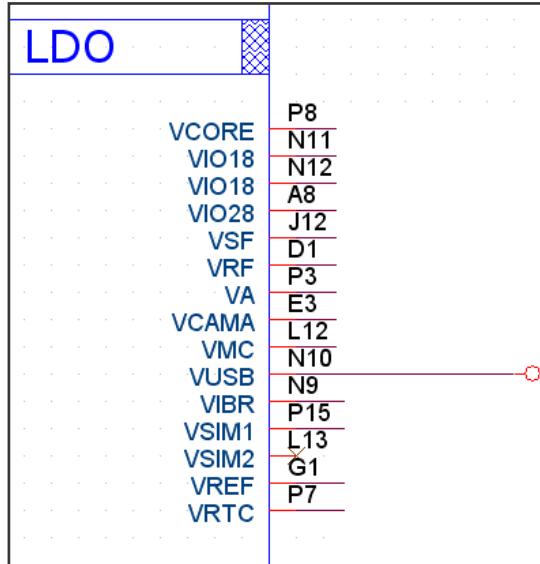
MT2503_Baseband USB

Schematic Notice – USB

■ MT2503 USB schematic (1/3)

– USB Power: VUSB. [1]

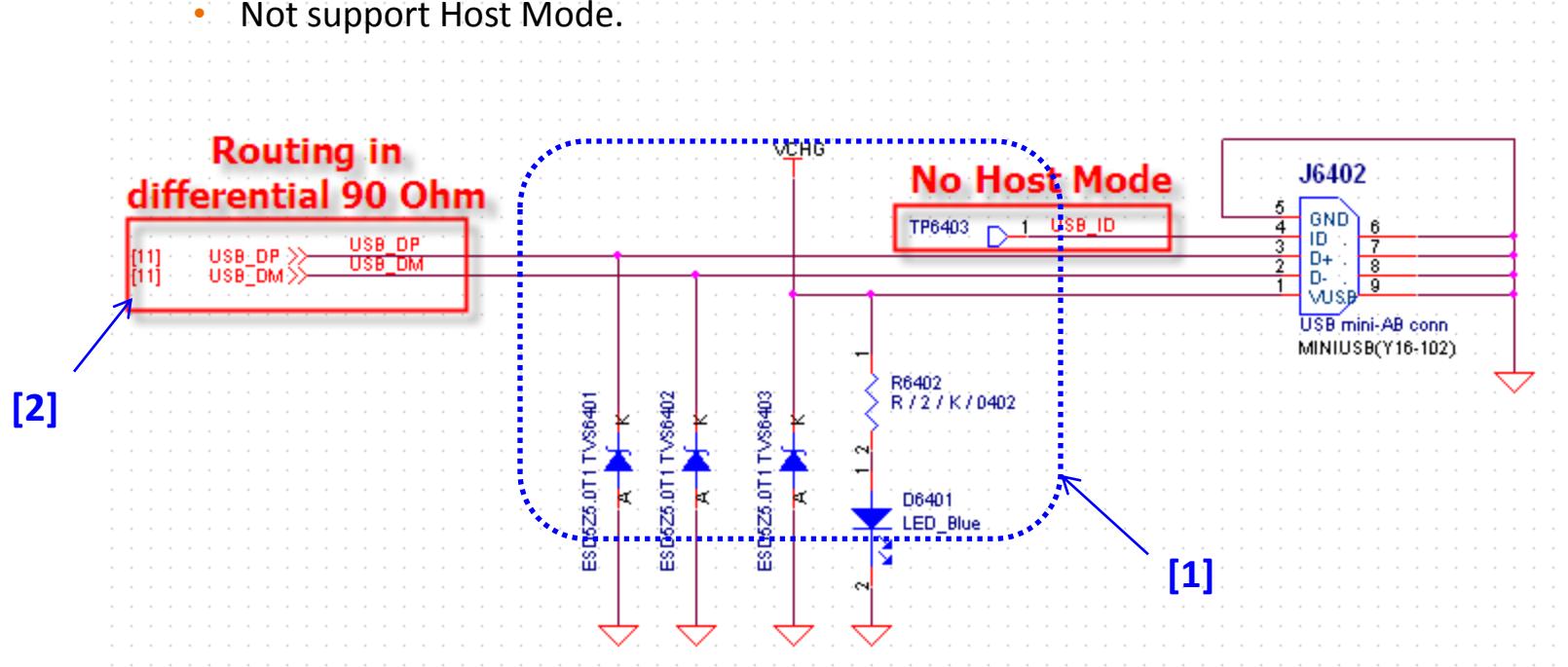
- Add a capacitance 1uF for LDO stable.
- Place the 1uF capacitance close to PMU LDO output.



Schematic Notice – USB

■ MT2503 USB schematic (2/3)

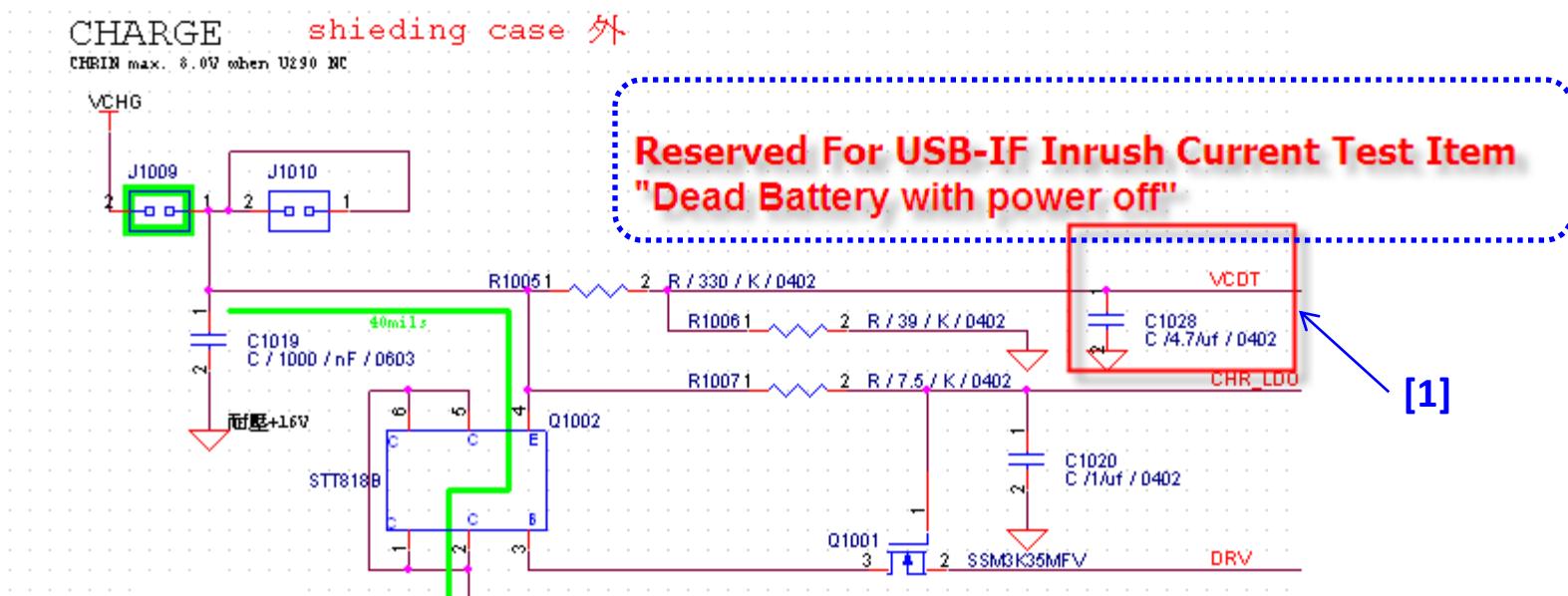
- USB application circuit on receptacle side
 - Reserve ESD protection device for USB differential pair . [1]
- USB Differential pair: USB_DM/ USB_DP. [2]
 - The USB 90-Ohm characteristic impedance “Recommend” implemented in PCB layout.
- USB Device Mode Only
 - Not support Host Mode.



Schematic Notice – USB

■ MT2503 USB schematic (3/3)

- USB application circuit on VBUS side
 - Reserve 4.7uF in VCDT for USB-IF test item. [1]



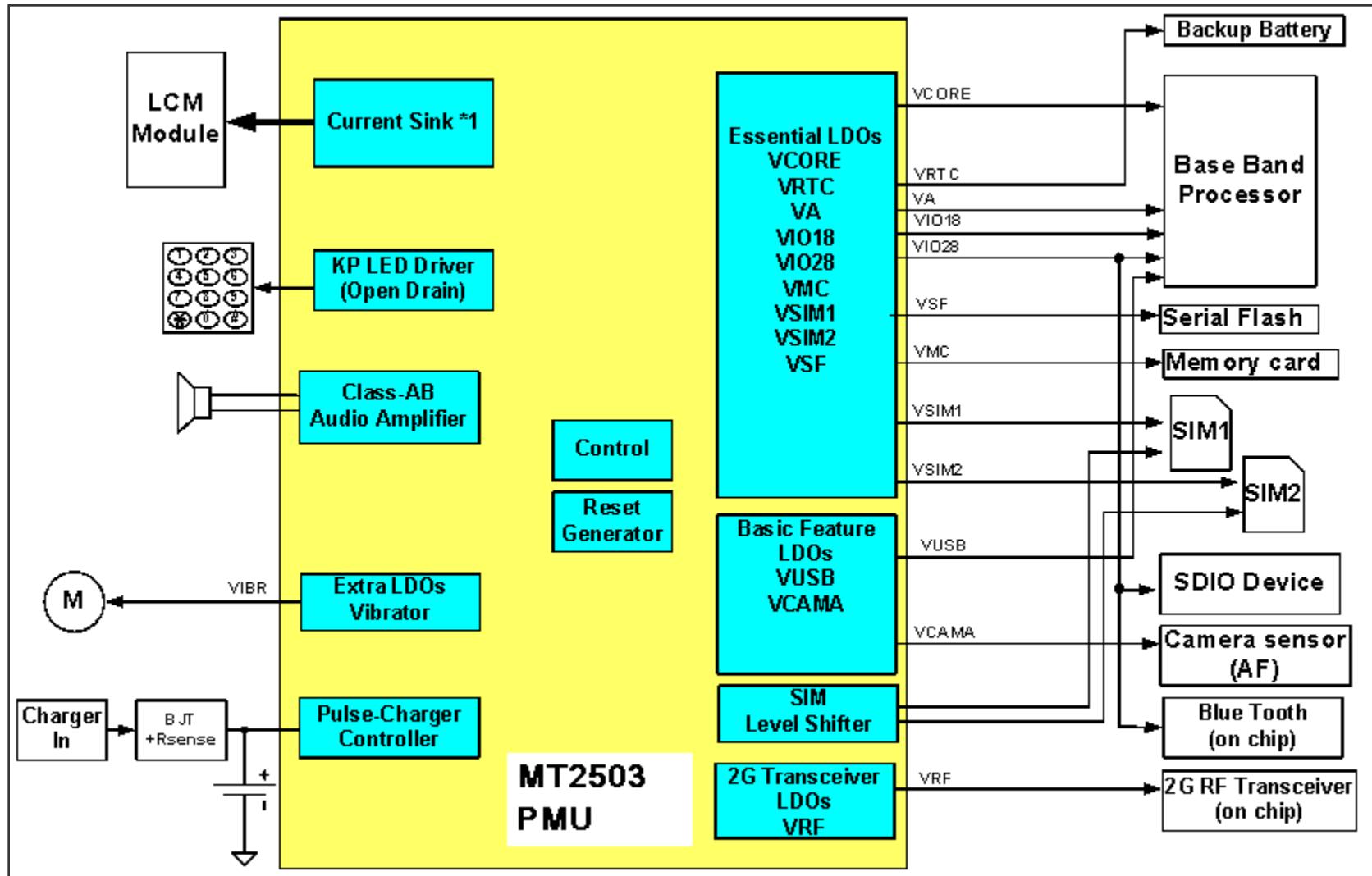
**For more information about USB generic
design notice, please refer to DMS**
(..\HW (For Customer Release) \ Common Design Notes \ USB)

MT2503_Baseband PMU - Introduction

MT2503 – General Description

- The MT2503 built-in high performance power manager unit.
- Highly integrated functions fulfill all power requirement in feature phone system
 - LDOs
 - Analog LDO * 3
 - Digital LDO * 9
 - VRTC * 1
 - Charger controller
 - AC/USB
 - Pulse-Charger
 - Driver
 - Parallel LCM backlight LED * 1
 - Keypad back-light * 1

PMU Block Diagram



PMU Feature list(1/3)

Function	MT2503 PMU		
General	Bandgap	YES	
	DDLO	2.5V	
	UVLO	Power On Threshold: 3.2V Power Off Threshold: 2.9V (Programmable)	
	Reset	YES	
	Soft-Start	YES (Default On LDOs)	
Protection	Thermal Shutdown	YES	
		Vout (V)	I_max (mA)
High Current Regulator	VCORE	0.75~1.35	150
Analog LDO	VRF28	2.8	150
	VA	2.8	150
	VCAMA	2.8	70

PMU Feature list(2/3)

Function		MT2503 PMU	
		Vout (V)	I_max (mA)
Digital LDO	VIO18	1.8	100
	VSF	1.86/ 3.0 /3.3	50
	VIO28	2.8	100
	VSIM	1.8/3.0	30
	VSIM2	1.8/3.0	30
	VUSB	3.3	45
	VCAMD		
	VMC	1.8 /2.8/3/3.3	100 (3V3@200mA>2.9V)
	VIBR	1.8/2.8/3.0	100
RTC	VRTC	2.8 / 3.3	2

PMU Feature list(3/3)

Function		MT2503 PMU	Note
Driver	LED_KP	60mA	
	Current Sink	1 x (96mA;48mA/ 0.25V), Current/Enable control)	
Charger	Charger type	Pulse charger(CC-CV)	
	Maximum Input Voltage	30	
	Maximum Charging Voltage	Programmable	
	OV	4.4	
	CC Mode	160mV/Rsense 8 Step Current Setting	
	Pre-Charge Mode	70mA/200mA	
	Battery Detection	V(NTC Pin)	
	Watchdog Timer	Yes	

MT2503_Baseband PMU - Function Description

PMU Function Description

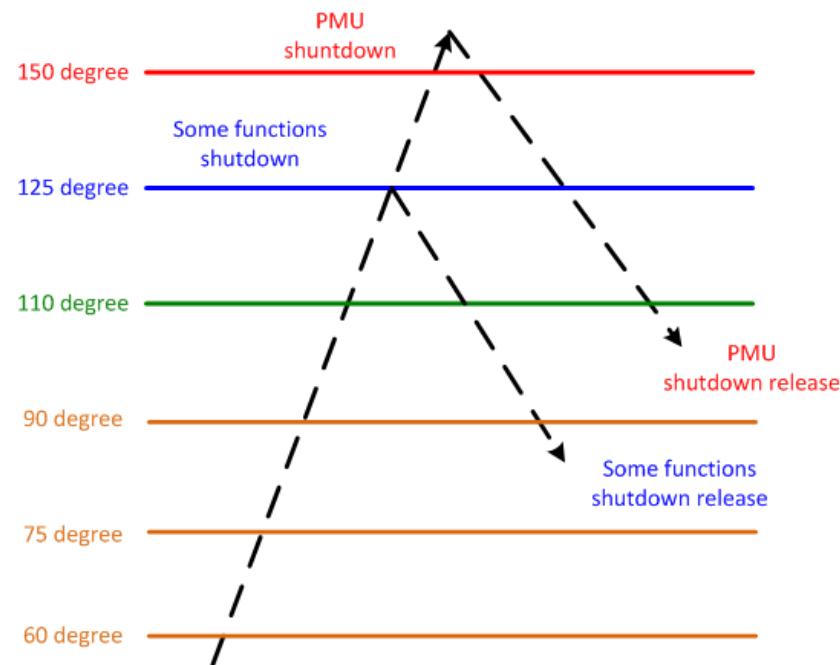
- **32K Removal Power on/off sequence**

Power on sequence	Power off sequence
MT2503	MT2503
VRF28	PWRKEY
VRTC	
PWRKEY	50msec
50msec	
Vcore	VUSB
2msec	VA
VIO18 (LDO)	VSF
2msec	VIO28
VIO28 (LDO)	
2msec	2msec
VSF	VIO18
2msec	2msec
VA (LDO)	Vcore
2msec	
VUSB (LDO)	
190msec	
RESETB Release	

PS: Above delay time is typical , the delay time variation spec is -50%~+100%
Example: Typical 2ms: variation is 1ms~4ms

PMU Function Description

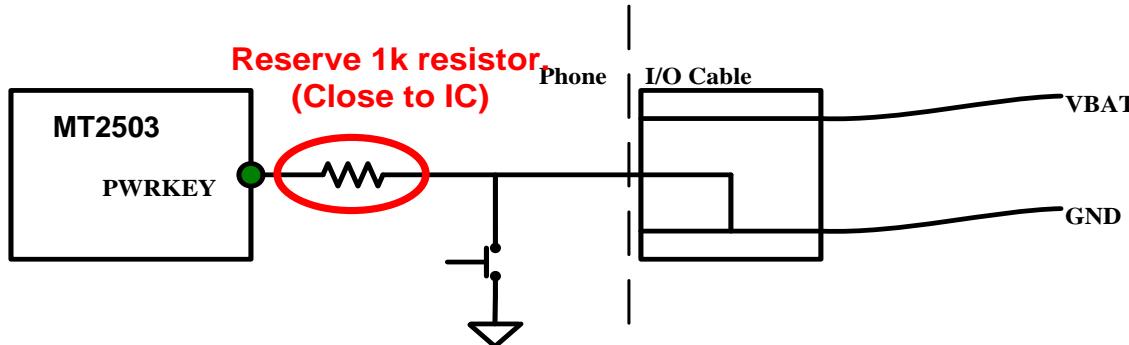
- Thermal part
- SW control
 - $T_j > 125\text{degC}$, disable big power function, others keep the same
 - **SW function latch**
 - **HW disable big power function ~ Ex: VIBR, SPK**
 - Function recover when $T_j < 90/75/60 \text{ degC}$.
 - **SW function release**
- HW control
 - **HW shutdown release when $T_j < 110 \text{ degC}$.**
 - **$T_j > 150\text{oC}$ PMU HW shutdown**



MT2503_Baseband PMU - Reference Design

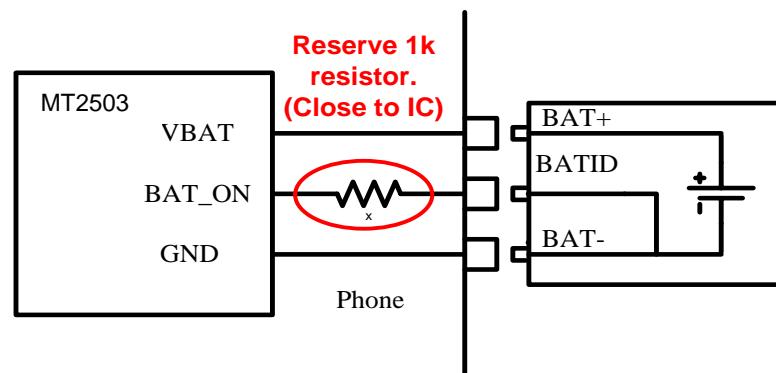
Reference Design

IC Protection: PWRKEY and BAT_ON

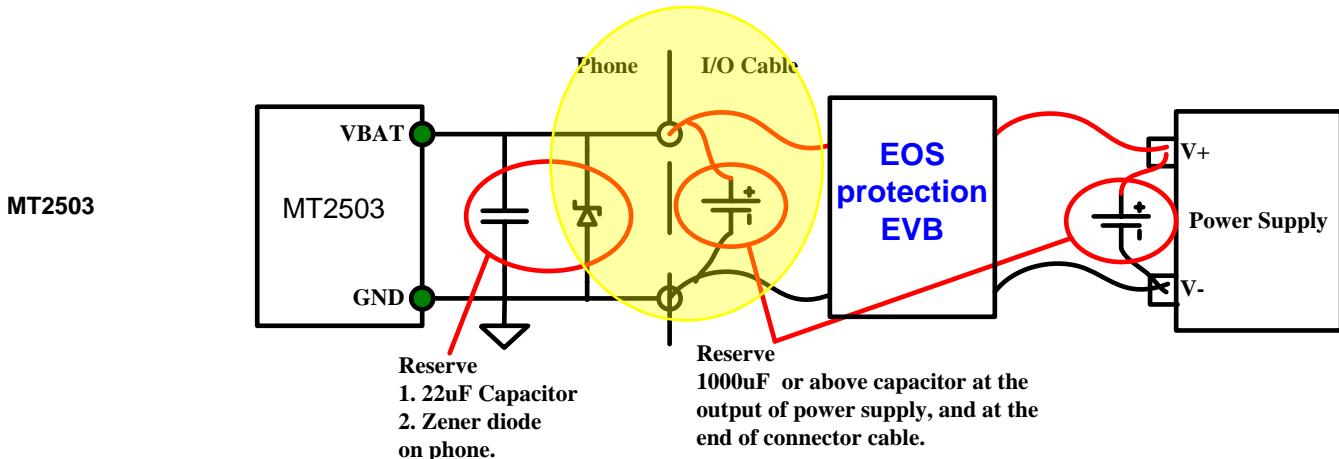


Please reserve 1k resistor on phone PCB to protect **PWRKEY** no matter if PWRKEY connect to any I/O connector or not.

Please reserve 1k resistor on phone PCB to protect **BAT_ON** pin if BAT_ON is used to detect battery.



Reference Design IC Protection: VBAT



MT2503 has lower VBAT voltage rating. (**Max. 4.4V.**) Some protection should reserve to prevent the damage by voltage surge.

- Design notice in Phone side:

- 1) At least 22uF capacitor.
- 2) Add Zener diode (5.1V/500mW) to protect the IC against low frequency voltage surge. Put it between battery connector and MT2503.

Notice: If using IO connector or test point to supply VBAT for download, manufacture, or repair, should let VBAT trace passing zener diode and 22uF capacitor before entering IC.

- Design notice in Power Supply side:

Add 1000uF (or above) capacitor at the output of the power supply to reduce the voltage bounce caused by long power cable. And the power cable should be as short as possible.

Also add 1000uF (or above) capacitor at the end of power cable (near phone side).

- Production line power supply:

Suggest add EOS protection EVB (contact MSZ ACS)

PMU Function Description

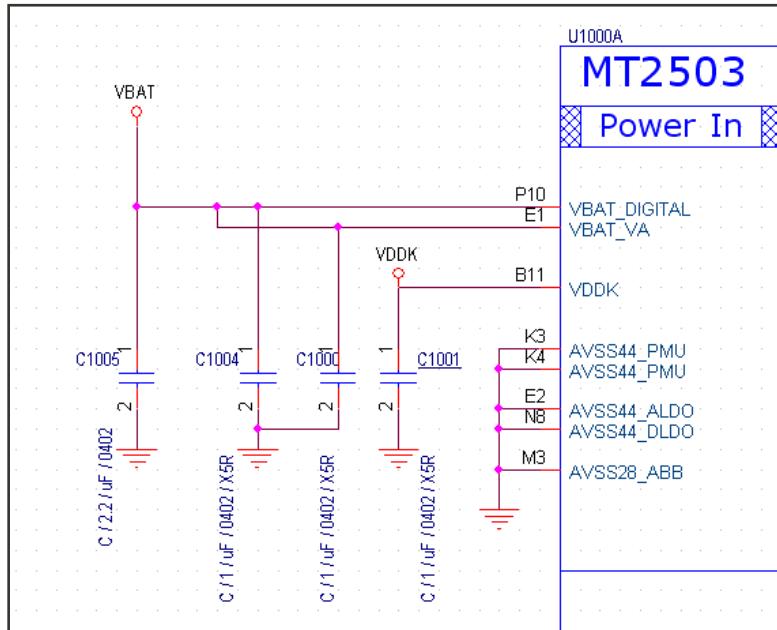
- IC Protection: Zener Diode Selection Guide (for VBAT)

Selection Guideline

- 500mW zener diode has lower Z_{ZT} than 200mW and can sink more exceptional surge voltage/current.
- [MT2503 must select 5.1V/500mW](#) zener to enhance VBAT pin protection.
- $I_r < 100\mu A$ @ $V_r = 4.2V$, $T_a = 25^\circ C$, Using 5.1V zener will introduce some leakage when $VBAT = 4.2V$. Large I_r current will introduce more leakage current.
- For more information about Zener Diode ,you can get it from MOL QAL/DRL(BB_Discrete_Validation List)

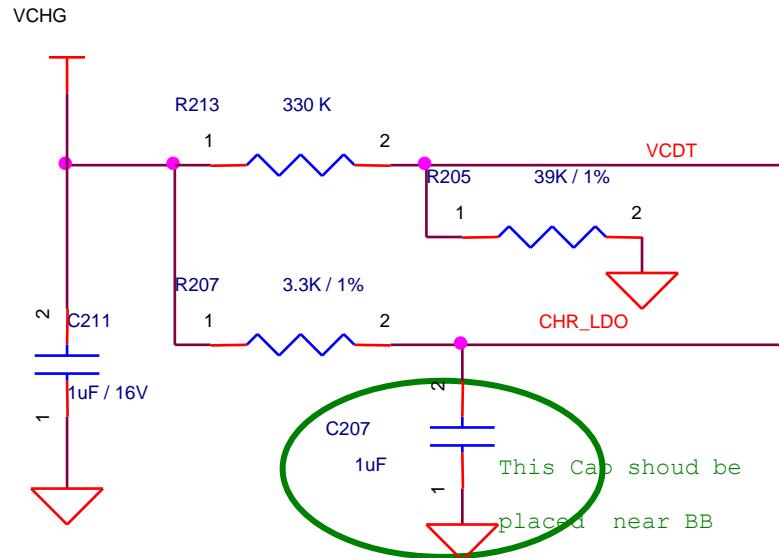
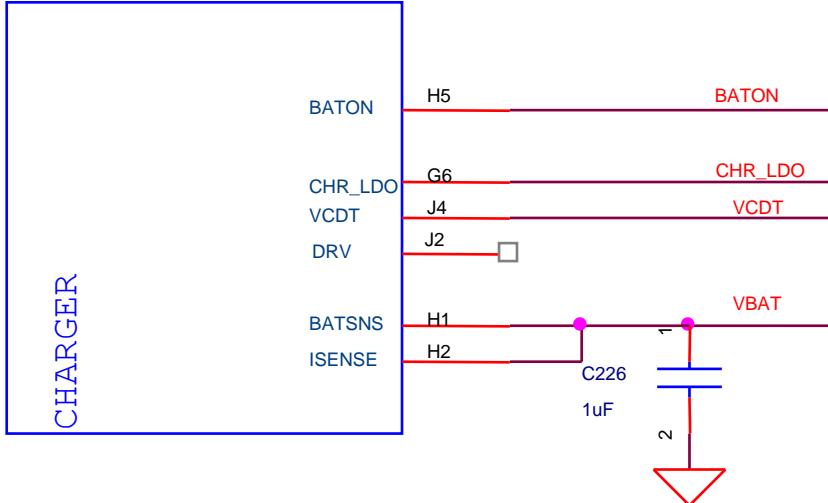
Design Notice – PMU SCH

- All input power pins of BB must be connected.
- Bypass cap must be added for input power end, close to M10, E1 PIN.
- Please keep CIN closer to MT2503 and put in shield case



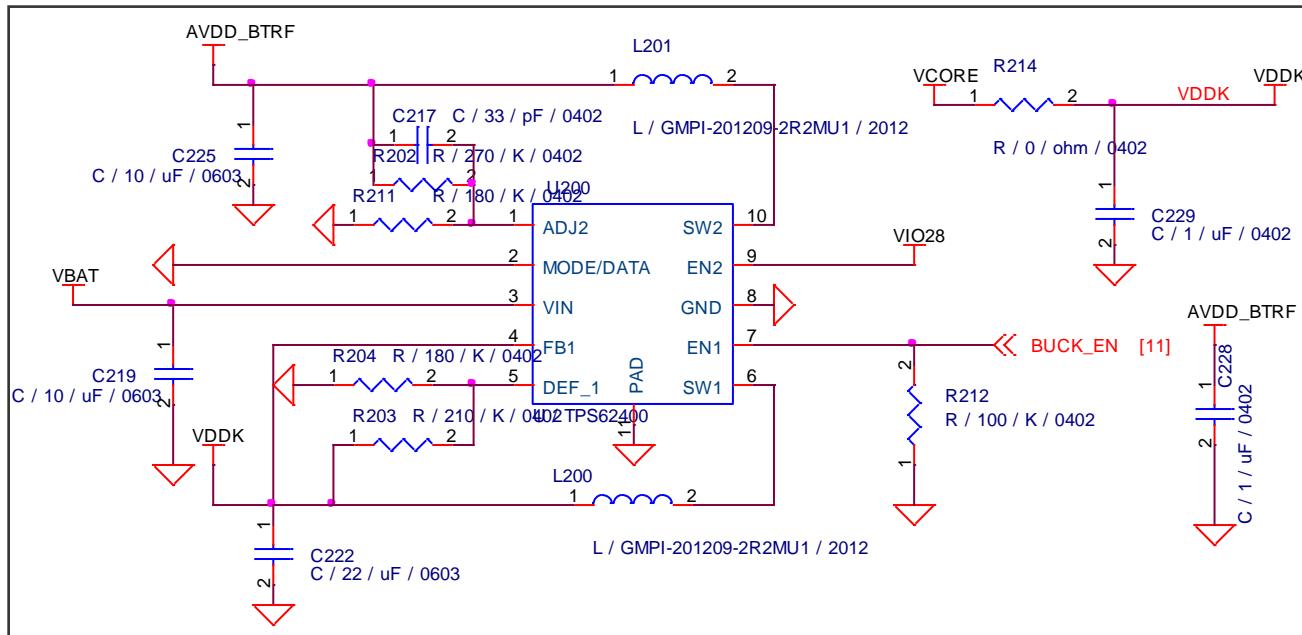
Design Notice – PMU SCH

- If required, follow reference design to design Charge Block.
- If charge block is not needed, design following the diagram below, DRV NC,BATON are connected in default way.



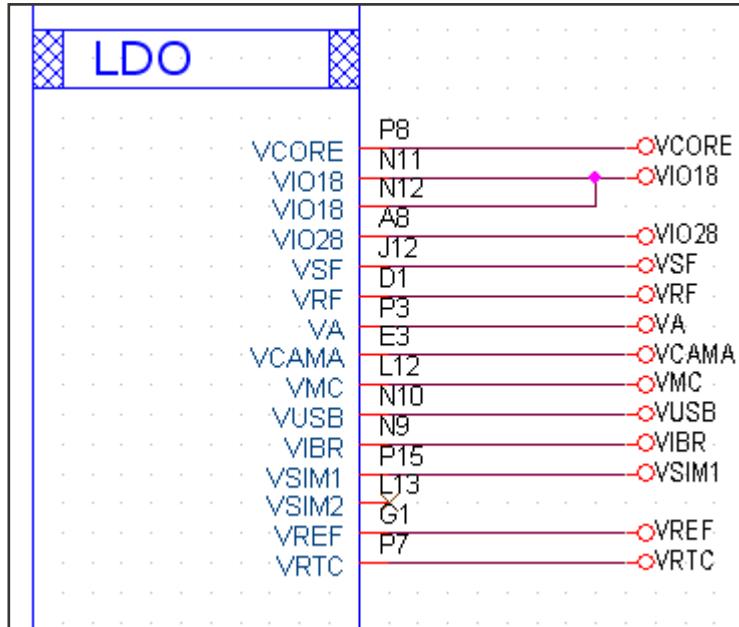
Design Notice – PMU SCH

- For ultra-low power design, add external two-way Buck and choose Buck IC based on QVL.
- When external Buck is used, the circuit connecting Vcore and VDDK via OR must exist.



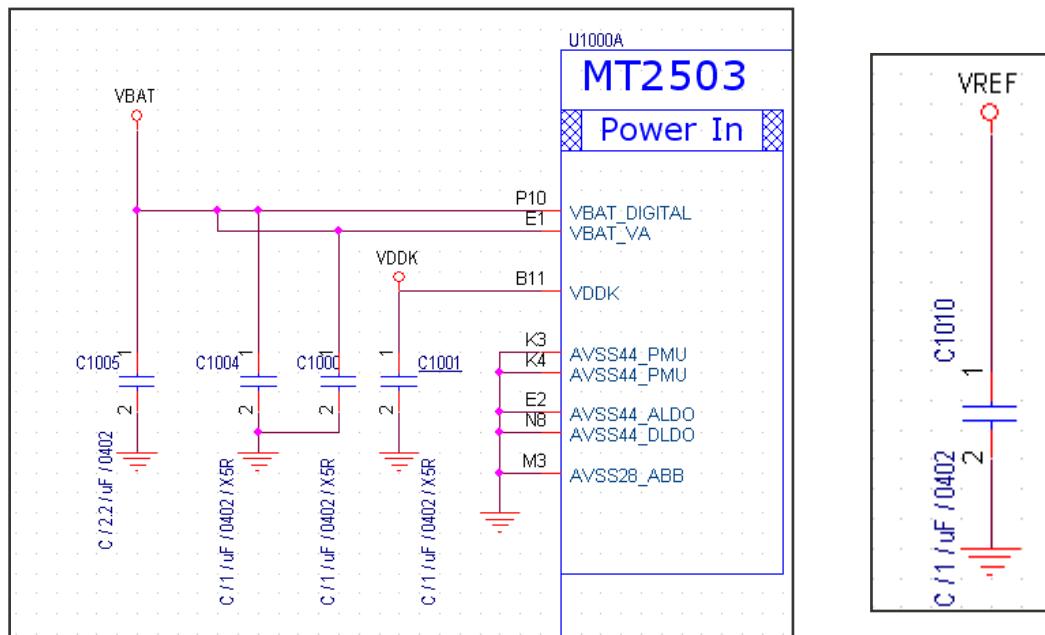
Design Notice – PMU SCH

- For LDOs which are used, put bypass cap near to BB.
- If VCORE\VIO18\VIO28\VSF\VRF\VA\VREF\VUSB \VRTC power are not used, it must add 0.1uF bypass cap. For other LDOs, like VCAMA, VMC, VIBR, VSIM1,VSIM2 , if they are unused, NC them directly, no need to add bypass cap



Reference Design Schematic

- Reserve enough bypass capacitors at Vcore to obtain good system stability.
(Place 1.0uF cap. as close to VDDK as possible, and reserve one cap. pads as close to VCORE LDO output that is recommended.)
- Place VREF bypass cap. as close MT2503 IC as possible.
 - VREF(G1) cap should connect to AVSS44_PMU(K3) and then connect to system GND.



MT2503_Baseband PMU - Function Block Notice

LDO Regulators List

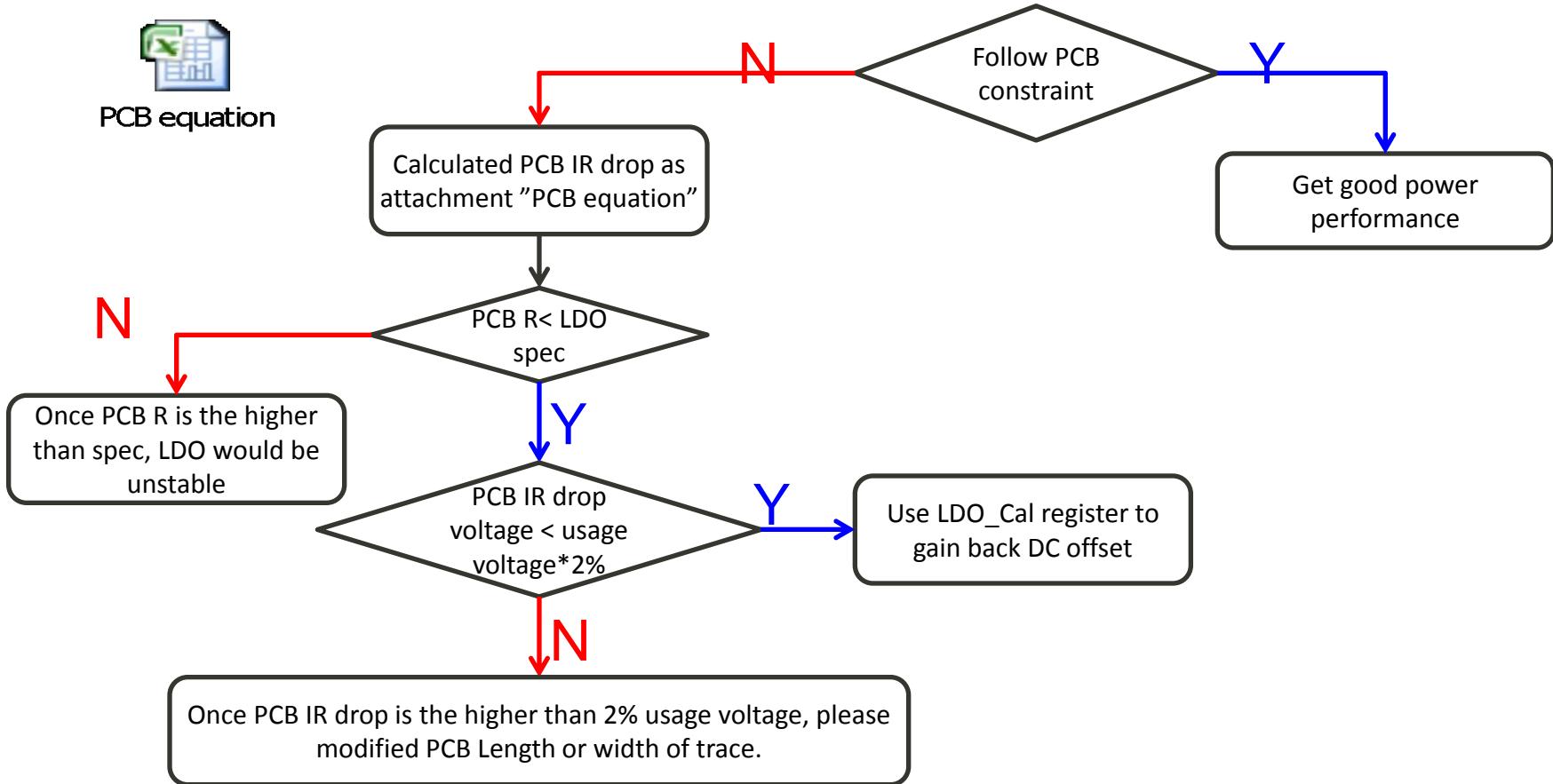
Block	Name	Voltage	I _{max}	Cap range (application side)	Cap Location	PCB ESR
High Current Regulator	VCORE	1.35/ 1.3 /1.2/1/0.9/0.85/0.75	150mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
ALDO	VRF28	2.8	150mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VA	2.8	150mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VCAMA	2.8	70mA	1uF~3uF +/-20%	Far-End	<200mΩ
Digital LDO	VIO18	1.8	100mA	1~3uF +/-20%	Far-End	<200mΩ
	VSF	1.86 /3.0/3.3	50mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VIO28	2.8	100mA	1~3uF +/-20%	Near-End: 1uF Far-End: other cap	<200mΩ
	VSIM1	1.8 /3.0	30mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VSIM2	1.8 /3.0	30mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VUSB	3.3	45mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VMC	1.8/2.8/3/ 3.3	100mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VIBR	1.8/ 2.8 /3.0	100mA	1uF~1.5uF +/-20%	Far-End	<200mΩ
	VRTC	2.8 /3.3	2mA	0uF~0.1uF	Far-End	<200mΩ

LDO Layout rule

I _{max} (mA)	PCB Trace width(W)	PCB length (L _{max})
0~40	6mil	2800mil(7.1cm)
50~190	8mil	
200~290	10mil	

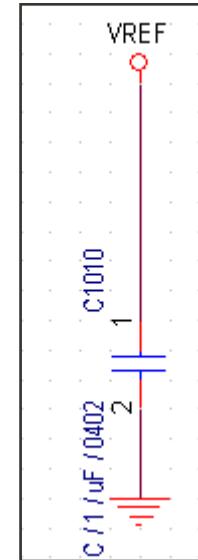
LDO Schematic/Layout Notice

- PCB IR drop calculation flow chart



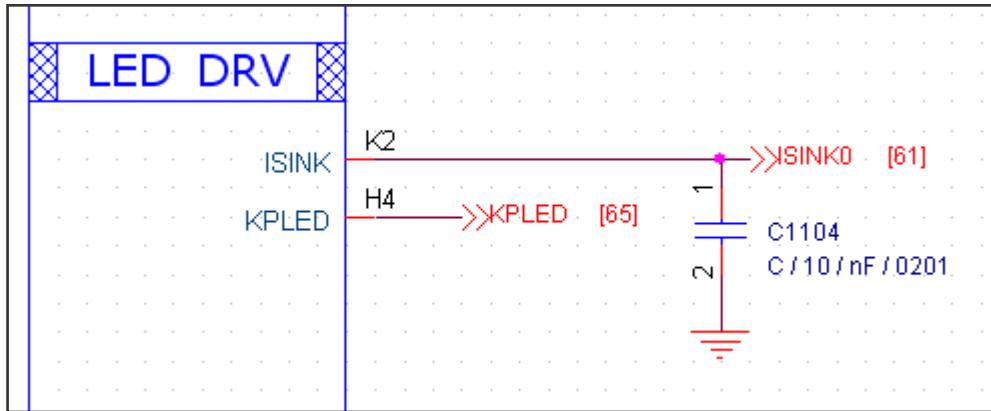
VREF Notice

- VREF bypass cap as close as possible to MT2503
- VREF cap is 0.1uF ~1uF.



MT2503_Baseband PMU - Driver

Driver : Schematic/Layout Notice



- The cap(10nF) is must in 2 layer pcb for FM de-sense and optional in layer(>2L) pcb
- More information pls see FM part

Driver : Component Selection Guide-LED

Absolute Maximum Ratings at Ta=25°C

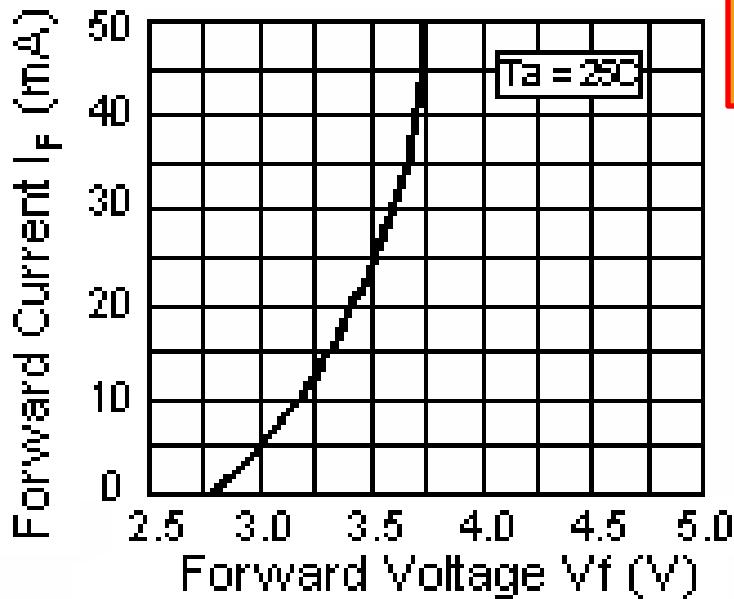
Parameter	LTW-206DCG-E3H	Unit
Power Dissipation	120	mW
Peak Forward Current (1/10 Duty Cycle, 0.1ms Pulse Width)	100	mA
DC Forward Current	30	mA

- The DC forward current absolute maximum rating should be higher than operation current, otherwise that would have reliability concern.

Driver : Component Selection Guide-R

Condition 1: **if** Forward Voltage Tolerance of all backlight LEDs \leq $\pm 0.1V$

You can connect cathode of LED to ISINK directly without current matching resistors..



VF Bin → VF(forward voltage) of backlight LED may has distribution and vendor may classified them into some groups.

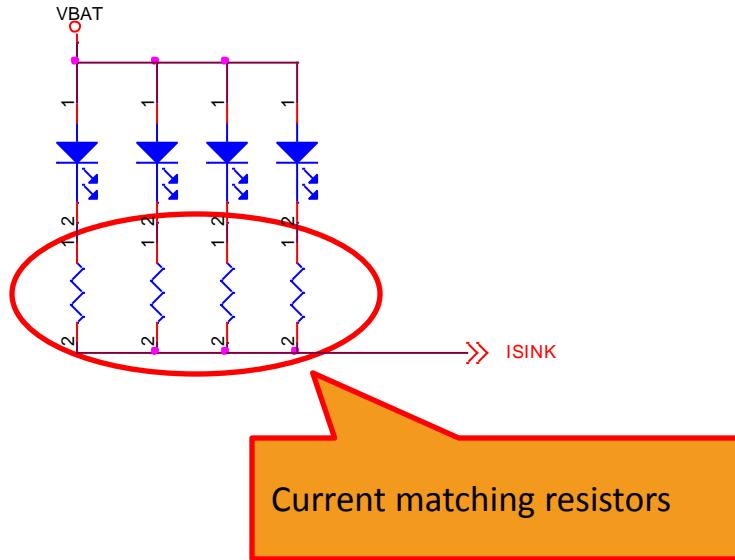
VF Bin	Forward Voltage (V) at $I_F = 20mA$	
	Min.	Max.
VZ	2.8	2.9
V0	2.9	3.0
V1	3.0	3.1
V2	3.1	3.2
V3	3.2	3.3
V4	3.3	3.4

If you choose a classification and the absolute difference of Min and Max is smaller or equal to $0.1V$. You can connect cathode of LED to ISINK directly without matching resistors.

- Please confirm with LED backlight module vendor to make sure the LEDs' forward voltage tolerance smaller than $\pm 0.1V$ to prevent current mismatch issue.
 - VF tolerance $\pm 0.1V \Rightarrow$ Current mismatch $< 5mA$

Driver : Component Selection Guide-R

Condition 2: **if** Forward Voltage Tolerance of all backlight LEDs $> \pm 0.1V$
Please reserve current resistors on dual LEDs ISINK path.



- VF mismatch $< 0.1V$ \Rightarrow No resistor
- $0.1V < VF$ mismatch $< 0.45V$ \Rightarrow 10ohm resistor
- $0.45V < VF$ mismatch \Rightarrow 15ohm resistor

Component Selection Guide-Vibrator

MTK VIBR LDO gear:

Regulator	Output Voltage (V)
VIBR	1.8/2.8/3.0

Vibrator specification:

Applicable condition:

1-1: Rated voltage: 3.0V DC

1-2: Voltage range: 2.6V-3.6V DC

1-3: Standard load: Oscillator R1.85x4.8L

1-4: Rotation direction: Clockwise from oscillator end

1-5: Temperature range: -10 degree~+60 degree

1-6: Storage temperature: -40 degree~+85 degree (20 degree, 65% RH, 1013Pa)

1-7: Motor position: all-direction

- Make sure output voltage setting of VIBR LDO is within the vibrator specification, otherwise vibrator will burn out and vibrating strength is not strong enough.

Vibrator



MT2503 External Buck for Vcore/BT Selection Guide

MT2503 External Buck for Vcore/BT Selection Guide

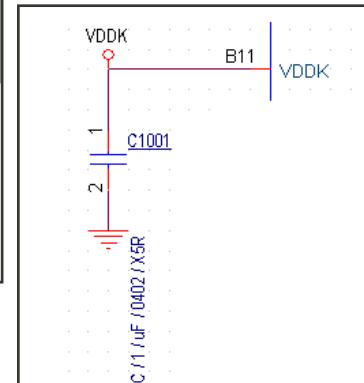
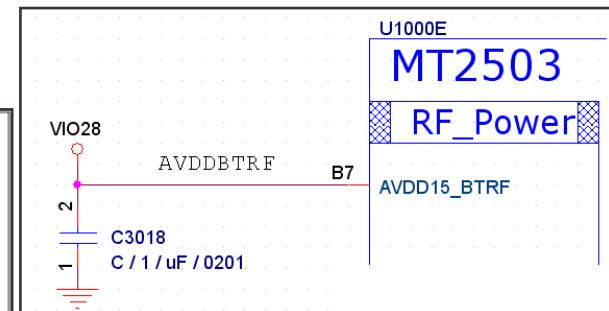
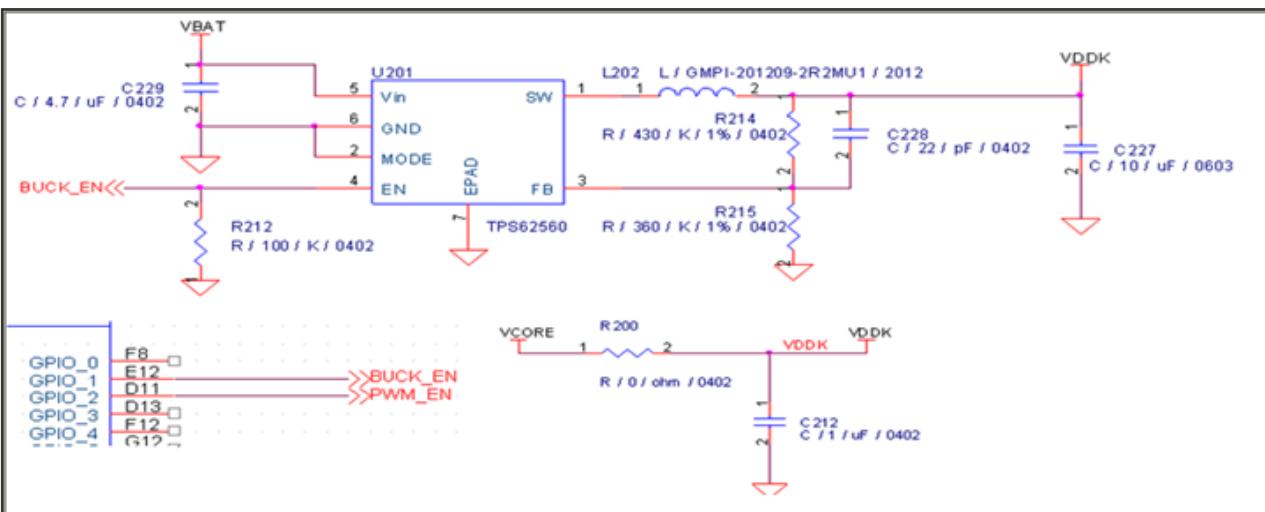
Item	Condition	Request SPEC	Note
CH1 (Vcore) Output accuracy	VBAT =3.0~4.4V,lout 0mA~150mA	MT2503 1.3V +/- 80mV	Must take care
CH2 (AVDD_BTRF) Output accuracy	VBAT =3.0~4.4V,lout 0mA~150mA	MT2503 1.5V +/- 80mV	If care BT voice/mp3 low power, please use dual buck
Output current	CH1 Vout in 1.3V +/- 80mV CH2 Vout in 1.5V +/- 80mV	150mA.<Imax<1A	
Quiescent Current (Input current)	VBAT =3.0~4.4V, Vout 1=1.2/1.3V and Vout 2=1.5V @lout1=0mA and lout2=0mA	<100uA	Small value is batter
Enable pin	Need EN1 pin, Make sure GPIO can control well,EN2 control by VIO28		
Turn-ON Rise Time	Time from active EN to reach 95% of Vout nominal	<500uS	
Efficiency	VBAT =3.6V,lout 5mA	>70%	Must take care
	VBAT =3.6V,lout 30mA~200mA	>78%	
Package	Parts package	<3x3mm	Small is batter
Other	If Vout> Buck regulation voltage ;Buck can't sink current.		Must take care

Reference Schematic by Single Buck TPS62560

If care BT voice /mp3 low power ,please use dual buck

- The independent enable pin for each channel

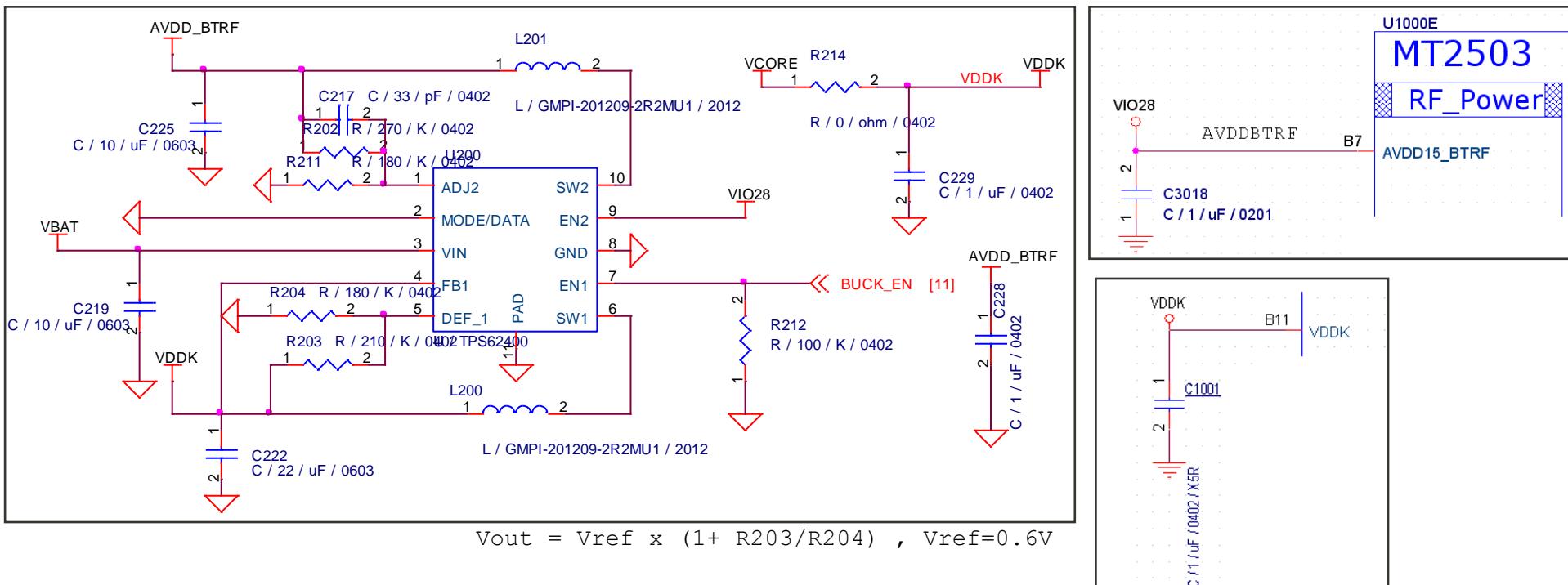
- EN connect to GPIO(PD), AVDD15_BTRF use power VIO28
- Buck output must connect with PMU's Vcore LDO together.
- Output voltage setting(referring to datasheet):
 - $V_{out} = V_{ref} * (1 + R_{214} / R_{215})$, $V_{ref} = 0.6$
 - For MT2503 output 1.3V , $R_{214}/R_{215}= 430k/360k$
- Place 1uF for VDDK and closes near IC



Reference Schematic by Dual Buck TPS62400

If use dual buck ,BT voice /mp3 can save 4~5mA

- The independent enable pin for each channel
 - EN1 connect to GPIO(PD)
 - EN2 connect to VIO28
 - Buck output1 must connect with PMU's Vcore LDO together.



Buck Enable pin DWS configuration

- If external buck is used:

SW: At the end of project makefile, add: CUSTOM_OPTION += __EXT_BUCK__

Tool: Set DWS file and GPIO which controls buck enable pin as below:

- GPIO1 DWS setting demo:

The image shows two windows of the ASTER02D DWS configuration tool. Both windows have a title bar: "C:\Documents and Settings\mtk08844\Desktop\External buck DWS配置\ASTER02D..." and an "X" button.

The top window displays a "GPIO Setting" table with 16 columns labeled: Def.Mode, M0, M1, M2, M3, M4, M5, M6, M7, M8, M9, In..., In..., R0, R1, D..., In, Out, In. Rows represent GPIO pins: GPIO0, GPIO1, GPIO2, and GPIO3. The "Def.Mode" column for GPIO1 is set to "0:GPIO1". The "R0" and "Out" columns for GPIO1 are checked, indicating it is configured as an output pin.

	Def.Mode	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	In...	In...	R0	R1	D...	In	Out	In
GPIO0	2:XP	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	P	<input type="checkbox"/>	IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO1	0:GPIO1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	P	<input type="checkbox"/>	OUT	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
GPIO2	4:PWM0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	P	<input type="checkbox"/>	IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>					
GPIO3	2:YM	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	P	<input type="checkbox"/>	IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

The bottom window displays a "GPIO Setting" table with 16 columns labeled: R0, R1, D..., In, Out, INV, O..., VarName1, VarName2, VarName3, U..., In. Rows represent GPIO pins: GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, and GPIO5. The "Out" column for GPIO1 is checked, indicating it is configured as an output pin. The "VarName" column for GPIO1 contains the value "gpio_external_buck_pin".

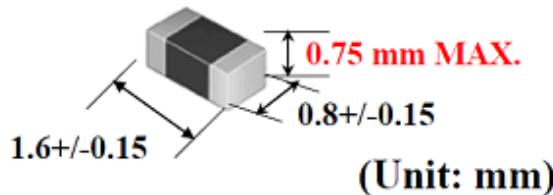
R0	R1	D...	In	Out	INV	O...	VarName1	VarName2	VarName3	U...	In
IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				<input type="checkbox"/>	GPIO0
OUT	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	gpio_external_buck_pin			<input type="checkbox"/>	GPIO1
IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				<input type="checkbox"/>	GPIO2
IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>				<input type="checkbox"/>	GPIO3
											GPIO4
											GPIO5

Note: If buck setting is enabled in software, but it does not match with GPIO hardware design or HW has no buck design, system cannot boot up.

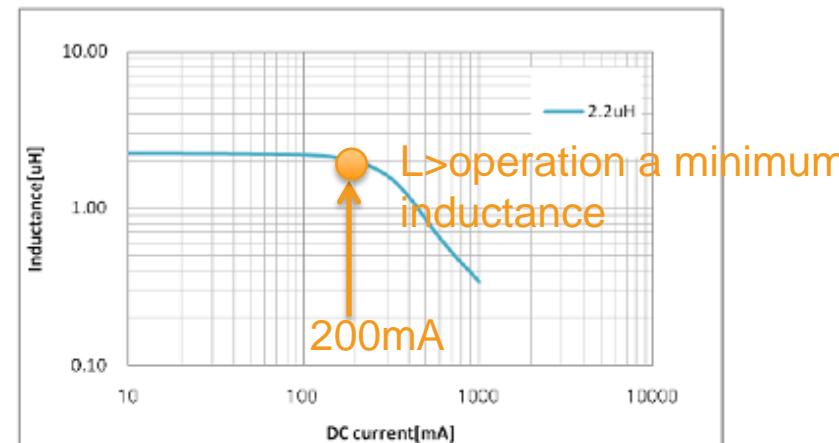
Inductor Selection Guide

- Depended on QVL's buck
 - Get the converters operation a minimum inductance and minimum capacitance.
 - Normal, choose L tolerance < +/- 20%
 - (Included I_{max} , -20 degree, 65 degree conditions)

■Dimensions



■Inductance-Current Characteristics



Inductor Selection Guide

- Current rating > Buck Imax
 - A conservative approach is to select the inductor current rating just for maximum switch current(cycle by cycle current limit)
 - Select Buck maximum output current is in 200mA~1A. It will get easily optimum efficiency point and select inductor current rating to prevent the damage once output short.

■ Specification

PN	Inductance [uH]	DCR [mohm Typ.]	Rated current[mA]		
			Isat Typ. (ΔL: 30%)	Irms Typ (ΔT: 40degC)	Irms Max (ΔT: 40degC)
LQM18PN2R2MDH	2.2	380	300	800	650

The inductor current rating “must be” higher than PMIC Imax and inductance variation should be lower than +/-20% for all operation condition.

Inductor Selection Guide

For more information about Inductor Material Determination, please refer to MTK online

http://online.mediatek.inc/Lists/QVL_Component/Attachments/28/Power%20Inductor%20Validation%20List_20140627_V1.3.xlsx

MT2503_Baseband PMU - Pulse Charger

Pulse Charger

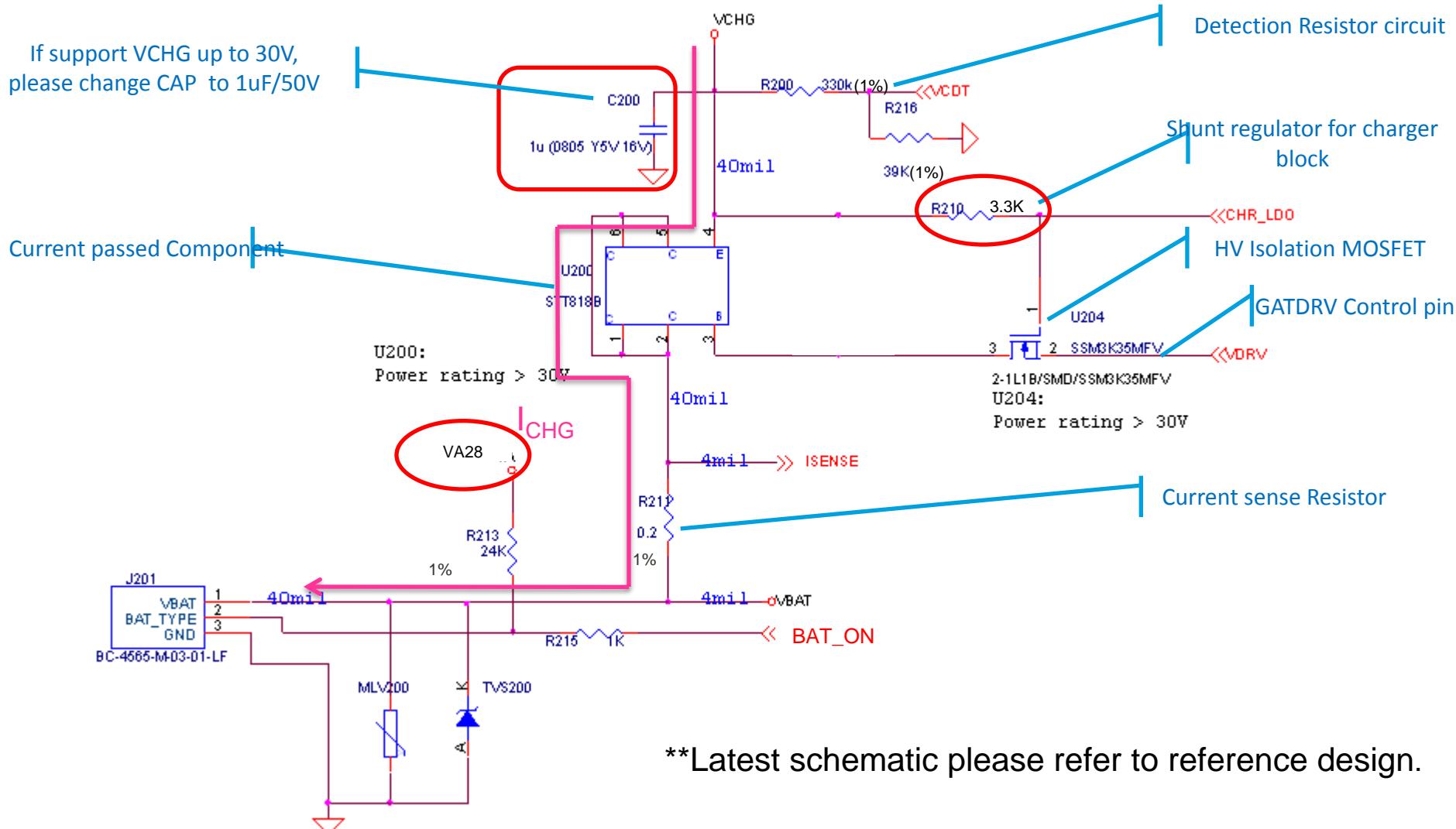
■ Feature

- Maximum input voltage up to 30V
 - (30V is system endurable voltage , not charge-able voltage)
- Constant current pre-charging
- Constant current mode current control
- Constant voltage mode for linearly current reducing
- Charger OVP and battery OVP
- Pre-charge/CC safety timer
- Watchdog timer

Pulse Charger Feature List

Feature	Chip
Charging type	Pulse Charging
Maximum charger input voltage	30V
Support battery type	Li-ion
VCHG OVP	Pre-CC : 10.5V CC : 10.5V (Maximum) ; 7V (Default)
CV	4.2V (Default)
CC Maximum Current	160mV/R _{SENSE}
Pre_charge	70mA(USB) / 200mA(AC<7V), 70mA(AC>7V)
Battery OVP	4.30V (Default)
Watchdog timer	Yes
Pre-charge safety timer	35 Minutes
Passed element	BJT+ N-MOSFET
Pre-charge/CC overlap	Yes

Design Notice – Pulse Charge SCH



Design Notice –Charge Component

- U200 (BJT):Current passed Component
 - h_{FE} (DC Current Gain) is 60~100 (Typical 90 @-20~80 °C) at $I_C=0.5A$
 - For thermal dissipation concern, the U200 power dissipation must be large than 1W.
 - V_{CE} (Collector-Emitter Voltage) $\geq 30V$
 - $I_C > 0.8A$ (Depend on application)
- U204 N-MOS
 - V_{GS} threshold $< 1.5V$ @ $I_D=0.1mA$
 - $V_{DS}>30V$ (Depend on application)
 - $R_{DS(ON)} < 10 \Omega$ @ $I_D = 10 mA$, $V_{GS} = 2.5 V$
- C200 (VCHG input cap)
 - If want to support VCHG up to 30V, please change CAP to 1uF/50V.

Charge Current Setting

	MT2503	MT2503
Sense Resistor	0.2 Ohm	0.3 Ohm
Pre-Charge	70mA (USB or AC >7V) 200mA (AC < 7V)	46mA (USB or AC >7V) 133mA (AC < 7V)
CC	15	70mA
	14	200mA
	13	300mA
	12	450mA
	11	550mA
	10	650mA
	9	700mA
	8	800mA
	7	900mA
	6	1000mA
	5	1100mA
	4	1200mA
	3	1300mA
	2	1400mA
	1	1500mA
	0	1600mA

**For large charge current must care BJT power dissipation.

Charger OVP

- Charger over voltage protection **HW default is enable.**
After power on, SW will configure “VCDT_HV_VTH”

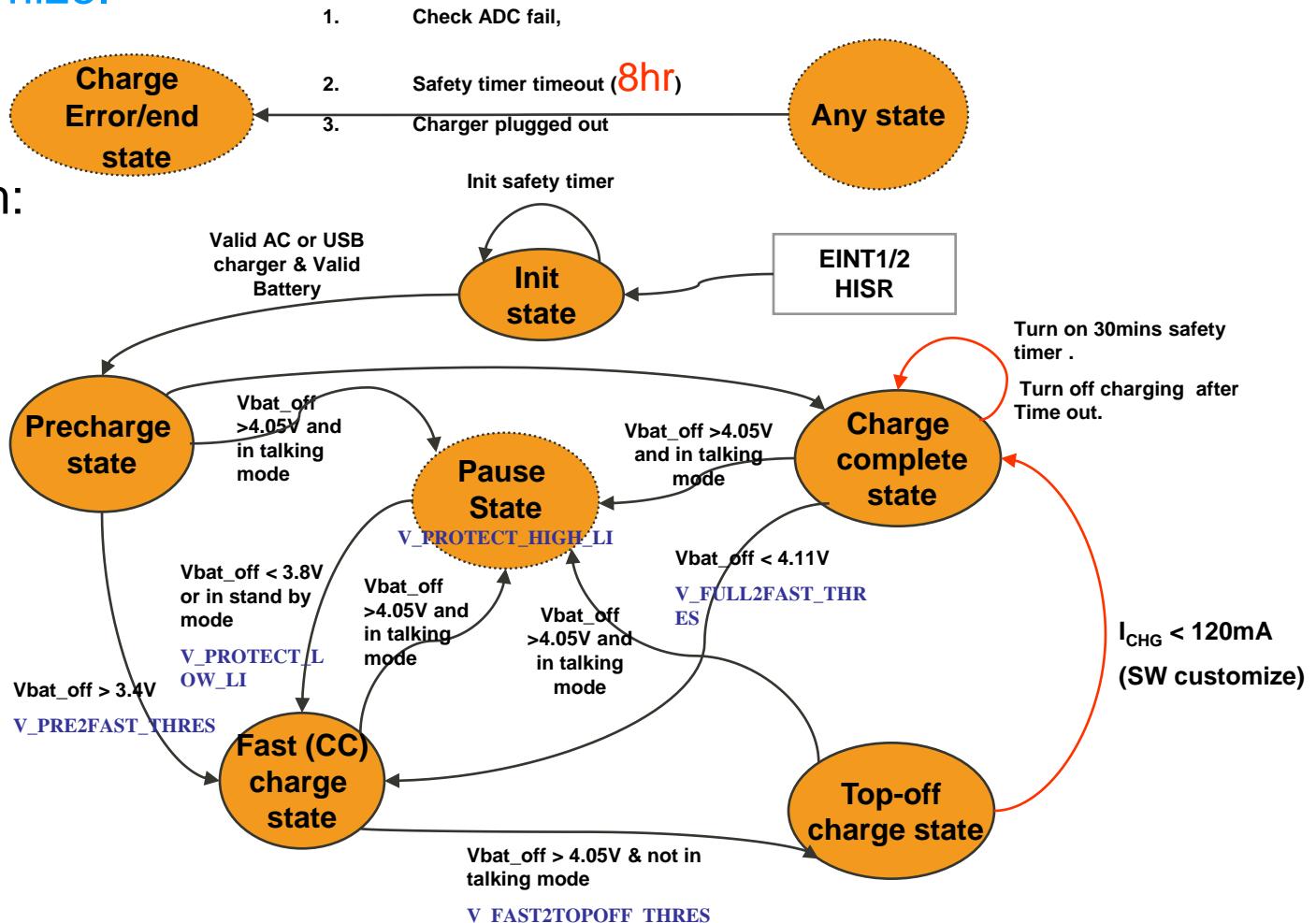
	Min	Typical	Max
09	5.7	6	6.3
10	6.175	6.5	6.825
11	6.65	7	7.35
12	7.125	7.5	7.785
13	8.075	8.5	8.93
14	9.025	9.5	9.97
15	9.975	10.5	11.02

— HW default voltage

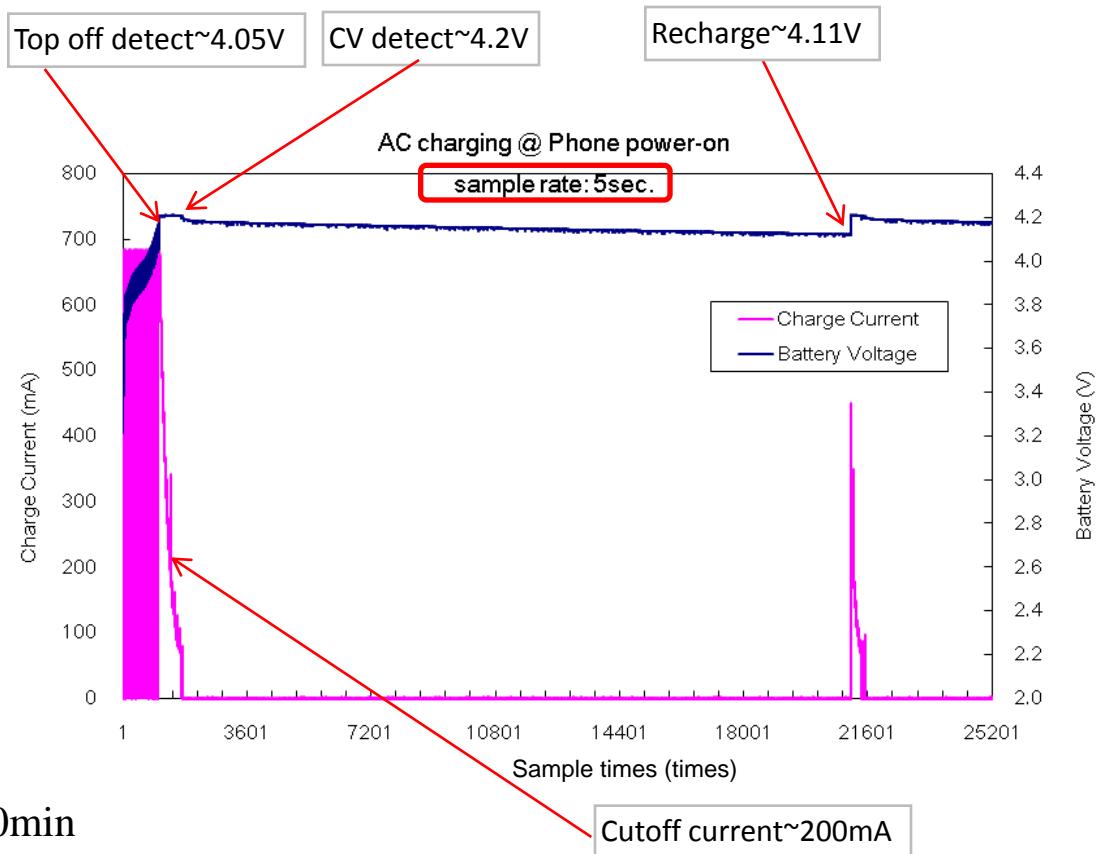
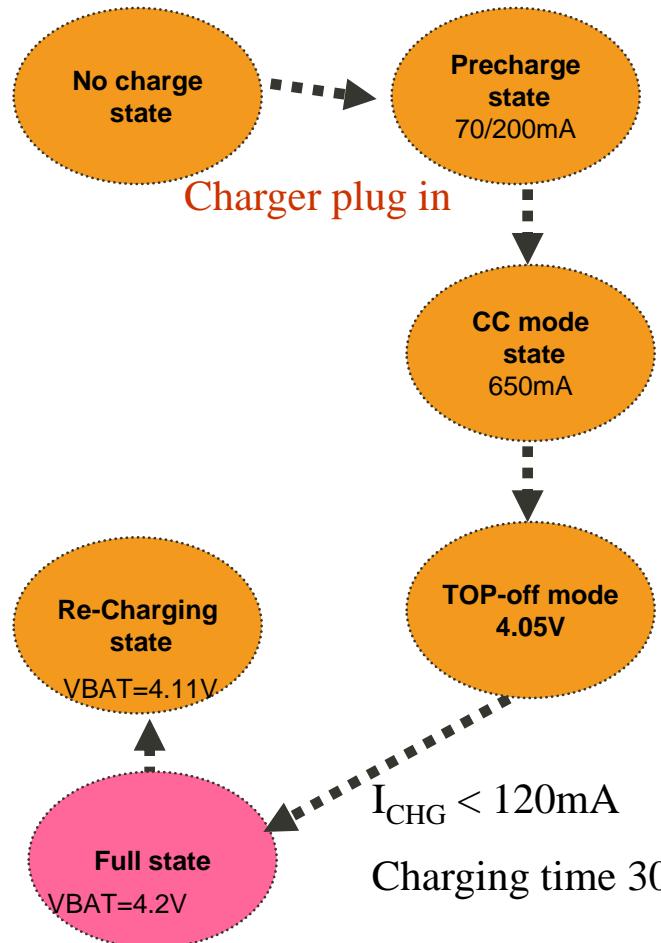
Charging State

- Please refer to pulse charging SW customize programming guide to customize.

State diagram:



Charging Curve

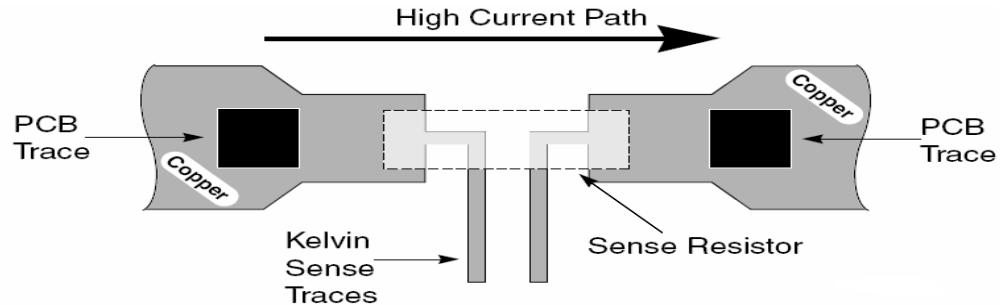


BAT_ON Use Notice

BAT_ON Connection State	Affection
Floating	It will trigger battery plug-out detection and can't charge.
With NTC resistor	Normal (want to sense thermal, use this option is must be!)
Connect 10kohm to GND	1) Temperature can't be sensed.
Short to GND	<p>1) Temperature can't be sensed. 2) Will trigger high-temperature protection.</p> <p>How to disable high-temperature protection: 1) Need to set BATON_HT_EN=0 (software)</p>

Charger Layout Notice

- **CHR_LDO decouple cap close to IC.**
- Rsense (Current sense resistor)close battery connector and trace is 40mil(star connect to connector)
- The exposed pad of the BJT (Current passed component) should connect to a large copper ground plane to get good thermal performance.
- ISENSE and BATSNS should be connected as the below figure.
- The trace from R_{SENSE} to battery connector should not share with other VBAT traces.
- ISENSE/BATSNS should be routed “Kelvin Sense Traces” which are away from noisy signals.



Charger Layout Notice

BJT Layout for Thermal Concern

- In right-hand of Figure, BJT (U201) connect to battery pack, this trace (mark with Blue line) will pass through much larger charging current.
- To consider the BJT thermal, this power trace is recommended to use 40mil trace's width or a copper plane.
- More VIAs on BJT's "C" terminal is recommended.

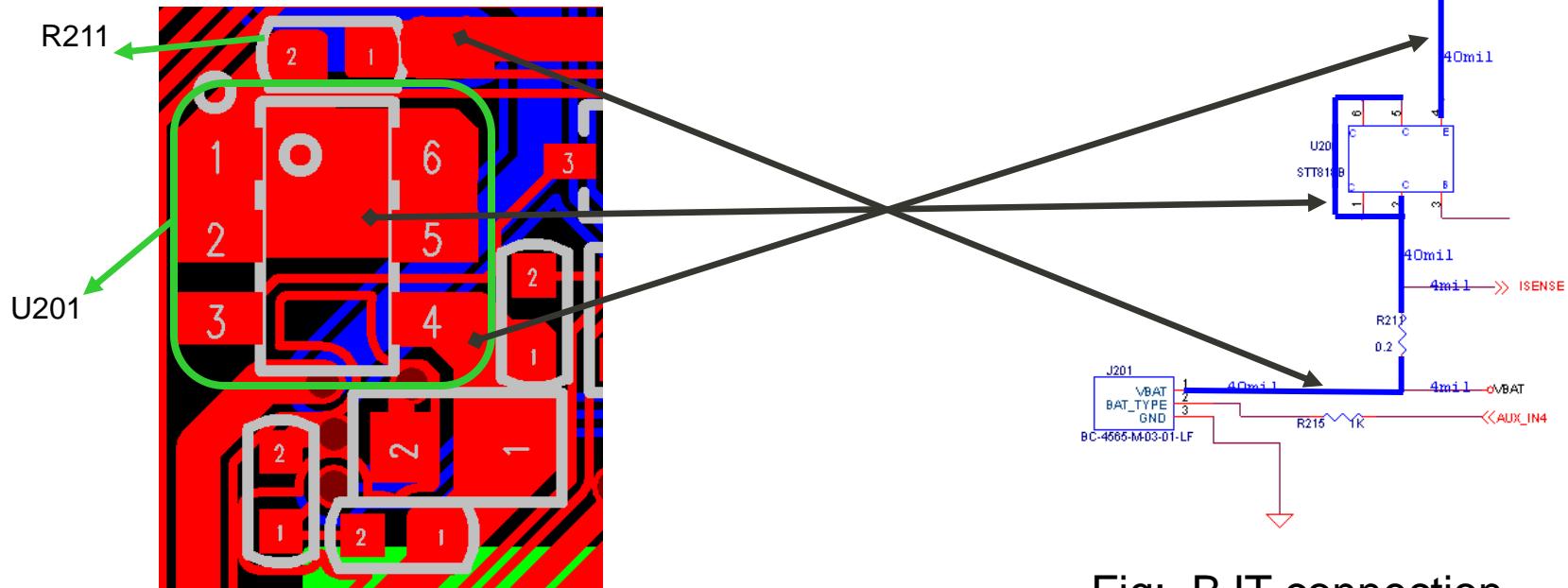


Fig: BJT connection

Rsense selection guide for wearable

- Battery capacity should be larger than 80mAh.
 - Due to MTK pulse charger current setting level is large.
 - Decrease BJT Beta can suited for small capacity battery.
- Rsense must smaller than 1.2 ohm.
 - Because of current ripple is high.
 - Current waveform will be square.
- Step1. Depend on battery capacity, normally pre-charge current = 0.1~0.3 C.
 - Ex. Battery capacity = 300 mAh.
 - Check datasheet pre-charge current 0.1~0.3C = 30~90mA.
- Step2. Check pulse charger current setting, select Rsense to match pre-charge current spec.
 - Ex. $I = 14mV / Rsense$
 - Pre-charge current = $14mV / Rsense$ to match 30~90mA
 - Select Rsense = 0.4 ohm.
 - Download current = $V_{sense} / Rsense = 90mV / 0.4 \text{ ohm} = 225 \text{ mA}$.
 - Default CC current = Download current, and can be configured by SW ; more detail, in next page

***Remind!! If Rsns > 0.68 Ohm,
Do not support DL wo battery!!***

Charge Current Setting

		MT2503
Sense Resistor	Rsense (Ohm)	
Pre-Charge	14mV (USB or AC >7V) 40mV (AC < 7V)	
CC	15	14mV
	14	40mV
	13	80mV
	12	90mV
	11	110mV
	10	130mV
	9	140mV
	8	160mV
	7	180mV
	6	200mV
	5	220mV
	4	240mV
	3	260mV
	2	280mV
	1	300mV
	0	320mV

If use these two current setting, may not see decrease current at CV mode.

$$\text{Current formula} \Rightarrow I = \frac{V_{sense}}{R_{sense}}$$

**For large charge current must care BJT power dissipation.

The CC current can be configured by SW , If your project need modify this parameter ,please contact MTK

MT2503_Baseband PMU - USB-IF BC 1.1 Feature

USB-IF B.C. v1.1 Feature Introduction

BC1.1 vs. YDT1591-2006

	USB-IF BC1.1			YDT1591-2006
Define Items	Dedicate Charger	Charging Host	Standard Host	Dedicate Charger
Output Voltage	DC: 4.75~5.25V			DC: 4.75~5.25V
Output Current	≤1800mA	500~1500mA	<500mA	300~1800mA
DP/DM	DP & DM short together	DP & DM 15KΩ to GND	DP & DM 15KΩ to GND	DP & DM short together
Interface	USB A/Micro USB AB			USB A
Others	Refer to BC1.1 standard for detail definition of detection mechanism.			N/A

USB-IF B.C. v1.1 Feature Introduction

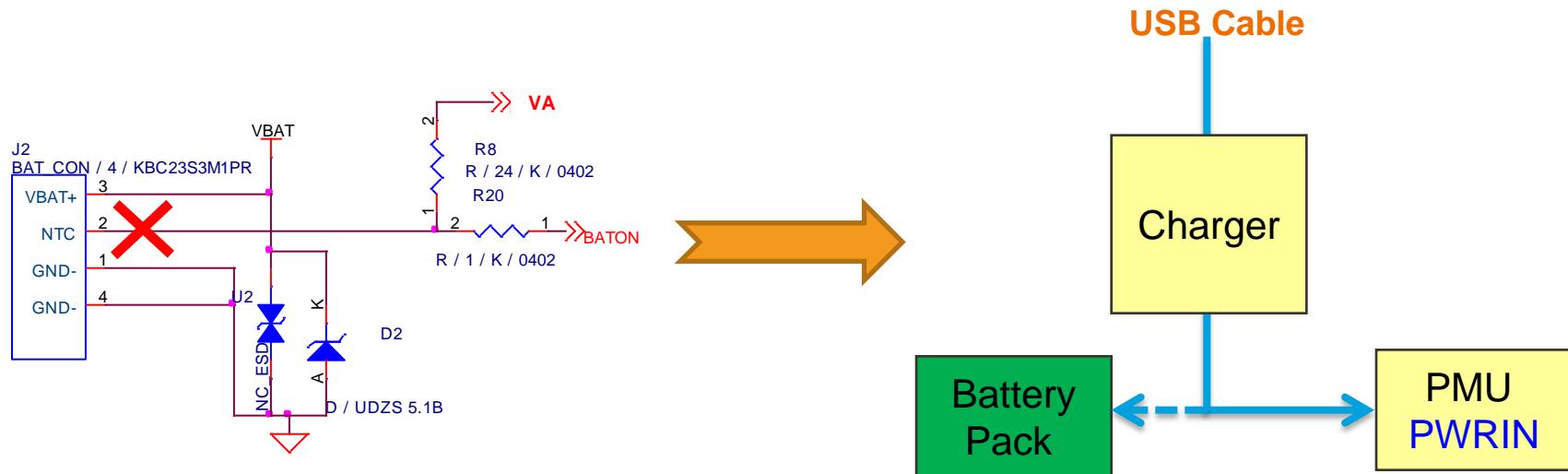
Apply BC1.1 to Fast Charging Time

- Define three types of charging ports in BC1.1
 - Standard Downstream Port
 $I_{CHG_MAX}=500mA$ and support USB2.0 communication.
 - Charging Downstream Port
 - $I_{CHG_MAX}=1.5A$ and support USB2.0 *Low/Full-speed* communication.
 - $I_{CHG_MAX}=900mA$ and support USB2.0 *High-speed* communication.
 - $I_{CHG_MAX}=560mA$ and support USB2.0 communication during *chirp*.
 - Dedicated Charging Port
 $I_{CHG_MAX}=1.8A$ but **can't** support USB2.0 communication.
- On reference design
 - Standard Downstream Port:450mA charging current
 - Charging Downstream Port:450mA charging current
 - Dedicated Charging Port:650mA charging current (**SW customize**)

MT2503_Baseband PMU - Down Load without Battery

Application note

- Down Load without Battery feature default is enable that uses USB power port as source in factory D/L stage.
(No need to press DL key, internal shorted, different from previous)
- If false triggered, software can disable this function when detect in normal power on.
- 8 seconds timeout for security concern.



MT2503_Baseband AUX ADC

CH Description, Typical input range, Scaling, and Typical output range

- MT2503

CH#	Description	Typical input range (V)	Scaling	Typical output range (V)
0	BATSNS	2.5~4.5	0.5	1.25~2.25
1	ISENSE	2.5~4.5	0.5	1.25~2.25
2	CHRIN	0~1.5	1	0~1.5
3	BATON	0.1~2.7	1	0.1~2.7
4	AUX_IN4	0 to 2.8	1	0 to 2.8
others	Internal use	N/A		

- AUX_IN4 can customers use in other function
- Other CH internal sense and used in some MTK features
- BATSNS has trim ADC Gain and offset in factory stage

AUX ADC SPEC

parameter	Comments	Min	Typ	Max	Units
Supply voltage		2.66	2.8	2.94	V
Resolution		-	-	10	bits
Analog-input bandwidth	w/o TSC w/i TSC			31.9k ^[2] 22.6k	Hz
Sample rate	w/o TSC w/i TSC			63.7k ^[1] 45.1k	Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	10-bit output	-1.5	-	+1.5	LSB
DNL	10-bit output	-1	-	+1	LSB

^[1] $F_{s,max} = 1.0833\text{MHz}/(10+1+4+2)=63.7\text{kHz}$ (w/o TSC),
 $F_{s,max} = 1.0833\text{MHz}/(10+3+9+2)=31.9\text{kHz}$ (w/i TSC).

^[2] $F_{Nyquist} = F_s/2$



CONFIDENTIAL B

Design Notice - MT2503_RF



Outline

- RF Brief introduction
- Reference design
- De-sense Design Note

MT2503 RF Features

- Receiver
 - Dual single-ended LNAs support
 - Quad band quadrature RF mixers
 - Fully integrated channel filter
 - High dynamic range ADC
 - 12dB PGA gain with 6dB gain step
- Transmitter
 - Transmitter outputs support quad bands.
 - Highly precise and low noise RF transmitter for GSM/GPRS applications
- Frequency Synthesizer
 - Programmable fractional-N synthesizer
 - Integrated wide range RFVCO and loop filter
 - Fast settling time suitable for multi-slot GPRS applications
- Digitally-Controlled Crystal Oscillator (DCXO)
 - Differential **2 pin** 26 MHz crystal oscillator
- - Low power mode support for 32K crystal removal
 - On-chip programmable capacitor array for coarse tune and fine tune.
- - Provide one high quality 26MHz clock buffer for co-clock with WiFi and can meet 802.11n STD
 - TRX BOM : Only need 1 bypass cap. and 1 crystal BOM .
 - Front end BOM : no need Tx SAW and Rx SAW.
 - Superior RF performance, Good margins on all Rx/Tx specs.
 - Support SAIC & VAMOS modem , achieve tier-1 modem performance around the world.
 - Easy implementation and full software support (driver, DCXO, calibration) enable straightforward design-in.

MT2503 RF Pin definition

Pin Name			Description
Name	I/O	Pin number	
RXLB	I	A1	LB LNA input
RXHB	I	B1	HB LNA input
TX_HB	O	C2	High band TX output
TX_LB	O	B2	Low band TX output
XTAL1	I	B4	Crystal pin
XTAL2	I	B5	Crystal pin
* FREF	O	C5	26 MHz clock frequency external output
VRF	VDD	D1	VDD for high frequency RF blocks
* EXT_CLK_SEL	I	D5	Clock selection for external or internal 26 MHz clock. When CLK_SEL=1, the DCXO receive external clock from XTAL 1.
* BPI_BUS0	O	B10	Control pin
* BPI_BUS1	O	B8	Control pin
* BPI_BUS2	O	A10	Control pin

* Ball map change in MT2503

MT2503 RF Pin DSDA Control Pin maps

maps control.

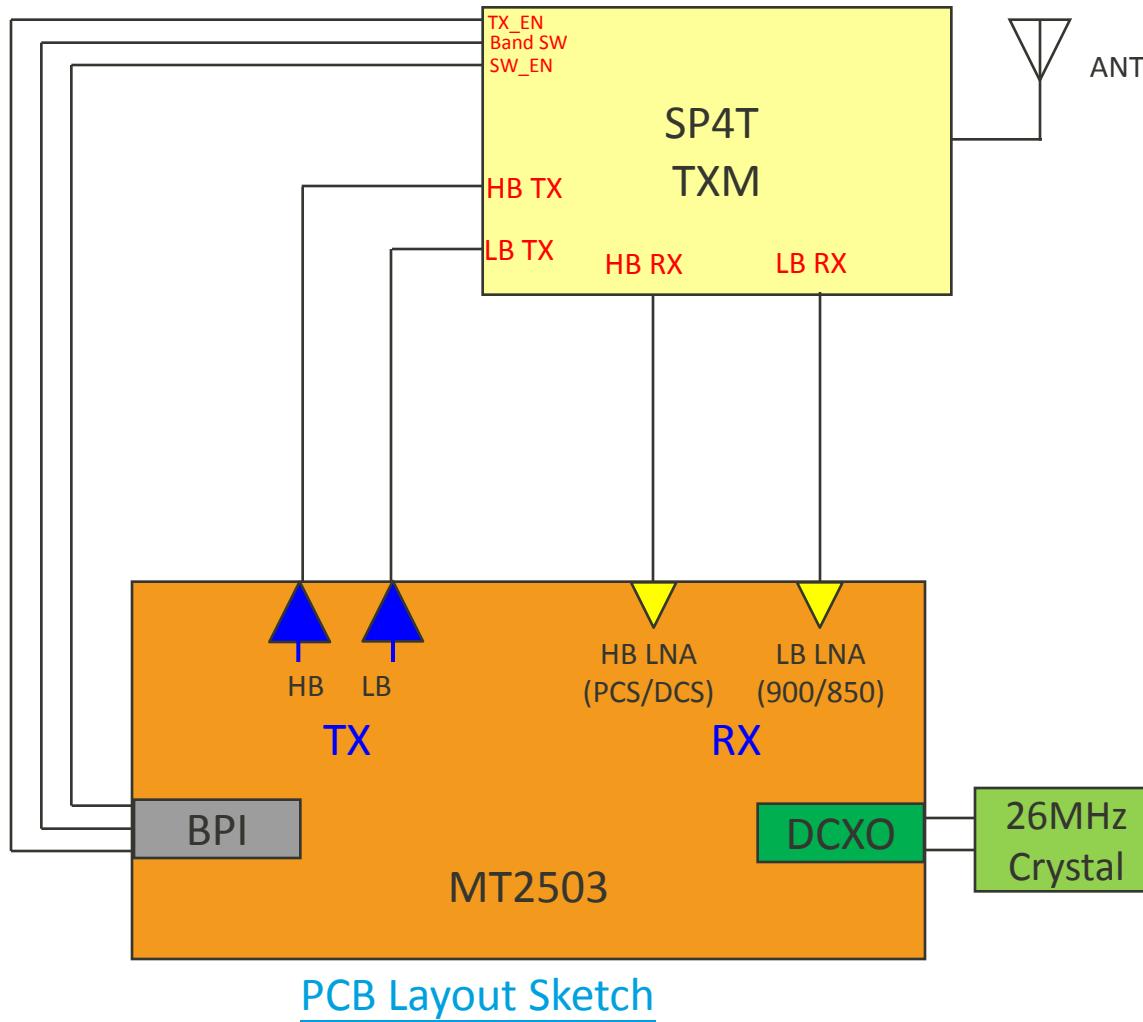
- 6 BPI for DSDA control if needed

RF  

• 6 BPI for DSD control if need

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	RXLB GHF	AVSS_2 GHF	SRCLK_E NAI	X	AVSS_2 GHF	BT_LNA	X	VIO28	BPI_BU S2	X	SCL28	CMRST	X	CMMCL K	CMCSD 0	GPS_XI N	GPS_XOU T	GPS_AVD D43_RTC	GPS_AVD D43_DCV	A		
B	RXHB	TX_LB	AVSS_2 GHF	XTAL1	XTAL2	AVSS_2 GHF	AVDD 5_BTR	BPI_BU S1	BPI_BU S0	VDDK	SDA28	GPIO_3	GPIO_2	CMCSD 1	CMCSK	X	GPS_DVS S11_COR FB	GPS_DCV S11_CLD	GPS_AV S11_CLD	B		
C	X	TX_HB	EINT	X	FREF	X	X	KCOL1	KROW1	KROW2	X	X	GPIO_0	X	CMPDN DD11_C OPF1	GPS_DV DD11_C OPF1	GPS_FO RCE_O	X	GPS_DCV	GPS_AV S43_DCV	C	
D	VRF	AVSS_2 GHF	GPIO_0	GPIO_1	EXT_CL K_SEL	X	KROW0	KROW3	KCOL3	X	KCOL4	GPIO_4	GPIO_5	GPIO_1	GPIO_6	GPS_32 K_OUT	GPS_AV DD11_R OPF1	X	GPS_AVD D11_CLD	X	D	
E	VBAT_V A	AVSS44 ALDO	VCAMA	TESTM ODE	KCOL0	KCOL2	UTXD1	URXD1	KROW4	GPIO_9	GPIO_8	GPIO_7	X	X	X	GPS_DV DD28_S OPF1	GPS_TX1	GPS_AVD D28_TLD	GPS_AVD D28_CLD	E		
F	X	FM_AN T_P	X	PWRKE Y	GND	GND	X	X	X	X	X	X	X	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_DV SS28_SF	X	GPS_JC K	X	GPS_AVD D_TCXO SHM	X	F
G	VREF	AVSS_F M	CHRLD O	BATON	GND	GND	GND	GND	GND	X	X	X	X	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_RX1	GPS_AVD D43_VBA	GPS_AV S43_MISC	G	
H	BATSNS	ISENSE	VCDT	KPLED	GND	GND	GND	GND	GND	GND	GND	X	X	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	GPS_RX1	GPS_DVD D28_IO1	GPS_VRE F	X	H
J	X	DRV	X	AUXIN4	GND	GND	GND	GND	GND	GND	GND	VSF	X	GPS_DV SS11_C OPF1	GPS_DV SS11_C OPF1	X	GPS_SC K1	GPS_AVD DD11_C OPF1	X	GPS_AVD D18_CM	GPS_OSC	J
K	X	ISINK	AVSS44 _PMU	AVSS44 _PMU	GND	X	LSCK	MCCM0	MCDA1	MCCK	X	X	X	X	X	X	GPS_RX 0	GPS_RX 2	X	GPS_T1P	GPS_T1N	K
L	AVSS44 BOOST	AVSS44 BOOST	AU_HPL	ACCDET	LSCE_B	TESTM ODE_D	RESETB	LPTE	X	MCDA0	MCDA3	VMC	VSIM2	GPS_JR ST	X	X	GPS_JDI	GPS_DVD D28_IO2	GPS_HRS T_B	X	L	
M	AVDD_S SPK	AU_HP R	AVSS28	AU_VIN	AU_VIN	X	LSAO	LSDA	X	X	MCDA2	X	SIM2_S CLK	SIM2_S RST	X	GPS_TX 0	GPS_JR CK	GPS_SCS 1	GPS_XTE ST	GPS_AV S_RF	M	
N	SPK_OU TN	AVSS_S PK	AU_HSP	AU_HS N	AU_VIN	AU_MIC 1_N	APC	AVSS44 _DLDO	VIBR	VUSB	VIO18	VIO18	SIM2_SI O	SIM1_SI O	SIM1_S RST	GPS_JD 0	GPS_EI NT0	GPS_EINT 1	GPS_AV S_RF	GPS_RFI N	N	
P	SPK_OU TP	AVSS_S PK	VA	X	AU_VIN 1_P	X	VRTC	VCORE	X	VBAT_D DIGITAL	X	USB11 DP	USB11 DM	X	VSIM1	SIM1_S CLK	GPS_JM S	X	GPS_AVD D18_RXF OPF1	GPS_AV S_RF	P	

Diagram of application circuits



MTK 2G SOC Feature list

- The RF features of MT2503 and MT6260 are the same except EDGE Rx.

2G SOC Key feature															
IC	Modem	TX	RX	SX	Crystal	SAW Less	Default TXM	RX FE	TX current (mA)	RX current (mA)	BPIs	DSP	Package Size	Ball pitch	Ball Pins
MT6260	EDRE RX	DFM	Hetrodyne	Fractional-N	DCXO-II	Yes	1P4T	Single-End sawless	*	*	4*	ARM7*	*	0.5	199
MT2503	GPRS	DFM	Hetrodyne	Fractional-N	DCXO-II	Yes	1P4T	Single-End sawless	*	*	3	ARM7	*	0.5	215

*some feature will be updated later

Reference Design

RF Alternative Components Qualification List for MT2503

TX Modules for MT2503

2.5G TX Module Qualification Plan for MT2503						
Type	Vendor	Part Number	Size (mm ²)	Band Supported	Schedule	Note
TXM	RFMD	RF7176	6.63 x 5.24	Semi-Quad	TBD	MT6260 Qualified
TXM	RFMD	RF7198	5.25X5.3	Dual-Band	TBD	MT6261 Qualified
TXM	SKYWORKS	SKY77569 WS569	7 x 6	Dual-Band	TBD	MT6260 Qualified
TXM	Airoha	AP5200	7 x 6	Dual-Band	TBD	MT6260 Qualified

- Note:
 - Note 1: These TXMs are qualified on MTK EVB, and the performance might be fine tuned based on customer's PCB layout
 - Please refer latest MTK QVL for new updates

Crystal for MT2503

Qualified Crystal Components for MT2503

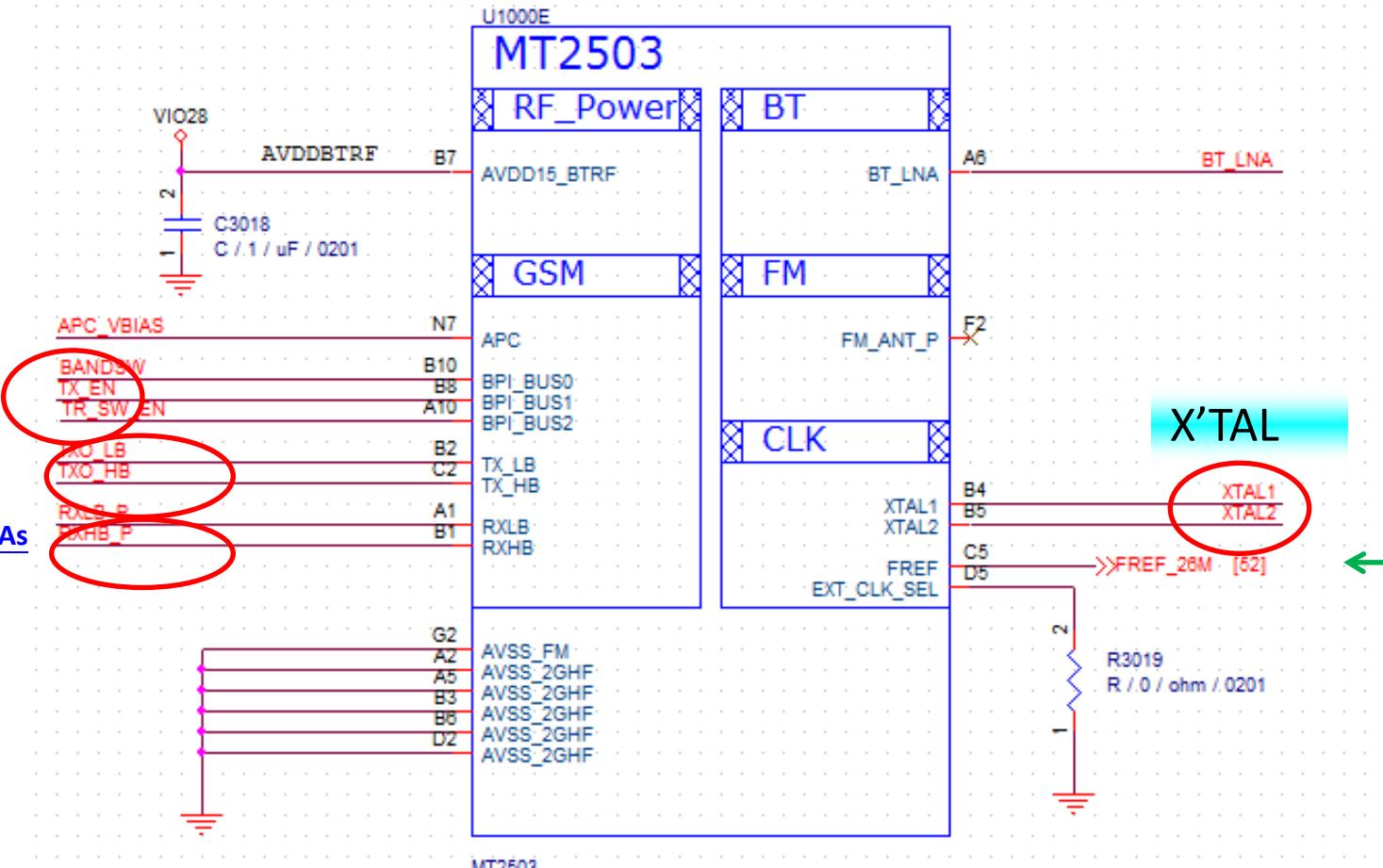
Vendor	Part Number	Freq. (MHz)	CL (pF)	AFC for CapID	Size (mm x mm)	Schedule
TST	TZ1689A	26	7.3	4500	3.2 x 2.5	
EPSON Toyocom	X1E000021043400	26	7.4	4500	3.2 x 2.5	
TXC	7M26000028	26	7.5	4500	3.2 x 2.5	
Hele (Harmony)	X3S026000B71HZ-HPR	26	7.2	4500	3.2 x 2.5	
Kyocera	CX3225SB26000B7FZFA2	26	6.7	4500	3.2 x 2.5	
Hosonic	E3SB26.0000F7GS11M	26	7.7	4500	3.2 x 2.5	
NDK	EXS00A-CS03170	26	7.5	4500	3.2 x 2.5	
CEC	K-F-26.000M-7.5-1010-2075-30	26	7.7	4500	3.2 x 2.5	
TXC	7V26000028 (Glass type)	26	7.5	4500	3.2 x 2.5	

- Note: **Don't use** MT6139/MT6140/AD6548 Crystal for MT2503
 - **MT62-50/51/52/53/55/56 /60**use the same 3225 Crystal part number
 - These crystals are qualified on MTK EVB, and the performance might be fine tuned based on customer's PCB layout and the crystal samples that vendor provided to customer !
 - Please refer latest MTK QVL for new updates

RF Schematic Review Check Items

<input type="checkbox"/>	Please use the XTAL and TXM which MTK Qualified
<input type="checkbox"/>	XTAL pin1 to chip B4, pin3 to chip B5
<input type="checkbox"/>	MT2503 TX/RX port has internal DC block, TX trace to TXM should reserve L-matching network for matching tuning
<input type="checkbox"/>	MT2503 RX trace to TXM should reserve π -matching network for matching tuning
<input checked="" type="checkbox"/>	TX L-matching should close to PA port, RX π-matching should close to MT2503 chip RX port
<input type="checkbox"/>	Check all GND_RF which should connect to ground
<input type="checkbox"/>	When MT2503 FREF connect to MT5931 , because chip has no internal cap, so that should series cap and suggest that reserve cap to GND and series 0 ohm (optional)
<input type="checkbox"/>	Vbat shunt 22uF & 39pF to GND, and close to PA_Vbat
<input type="checkbox"/>	VRF connect to MT2503, and shunt 1uF to GND
<input type="checkbox"/>	MT2503's BPI Trace connect to TXM control pin suggest that reserve series 0 ohm and shunt NC .
<input type="checkbox"/>	FEM layout should reference to design note from vendor ex: RF7198, GND pads should be the full GND plane, don't be the separated .
<input type="checkbox"/>	LCM CLK & data pins should reserve EMI filter pad for De-sense occur.
<input type="checkbox"/>	Keypad pins should reserve EMI filter pad for De-sense occur.
<input type="checkbox"/>	Camera CLK & data pins should reserve EMI filter pad for De-sense occur.

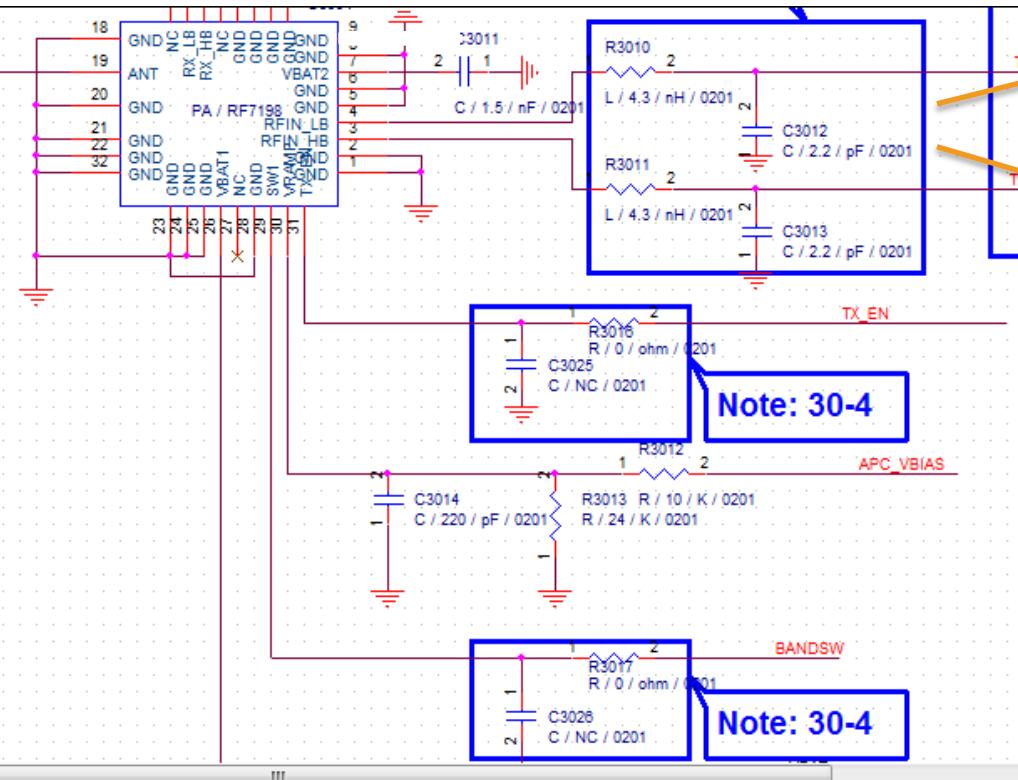
Quad-band Schematic -1/2



MT2503 RF part

Feed 26MHz CLK source to
XTAL1(B4) for debug purpose

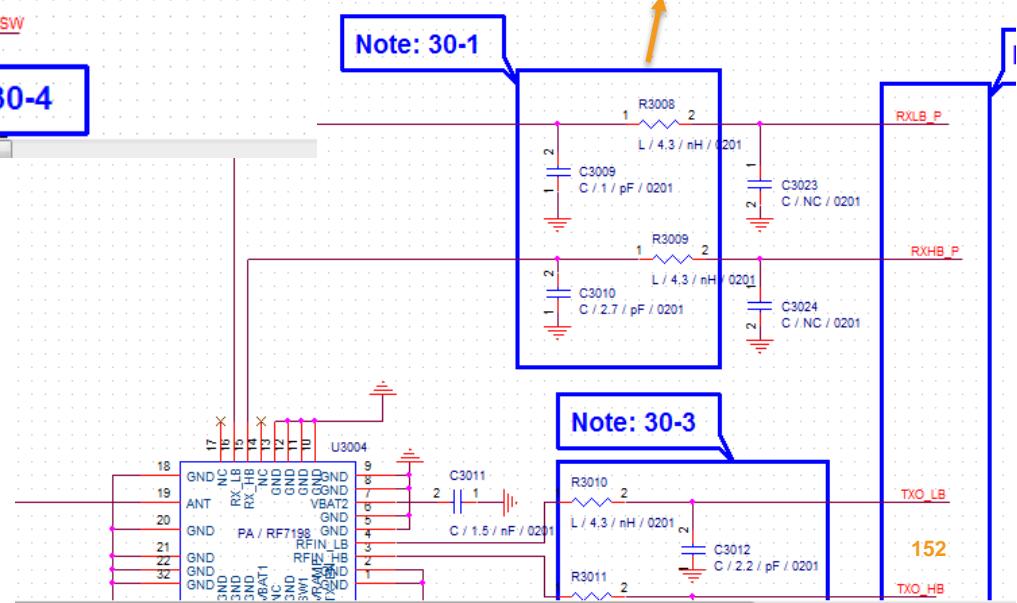
Quad-band Schematic -2/2



TX matching close to TXM

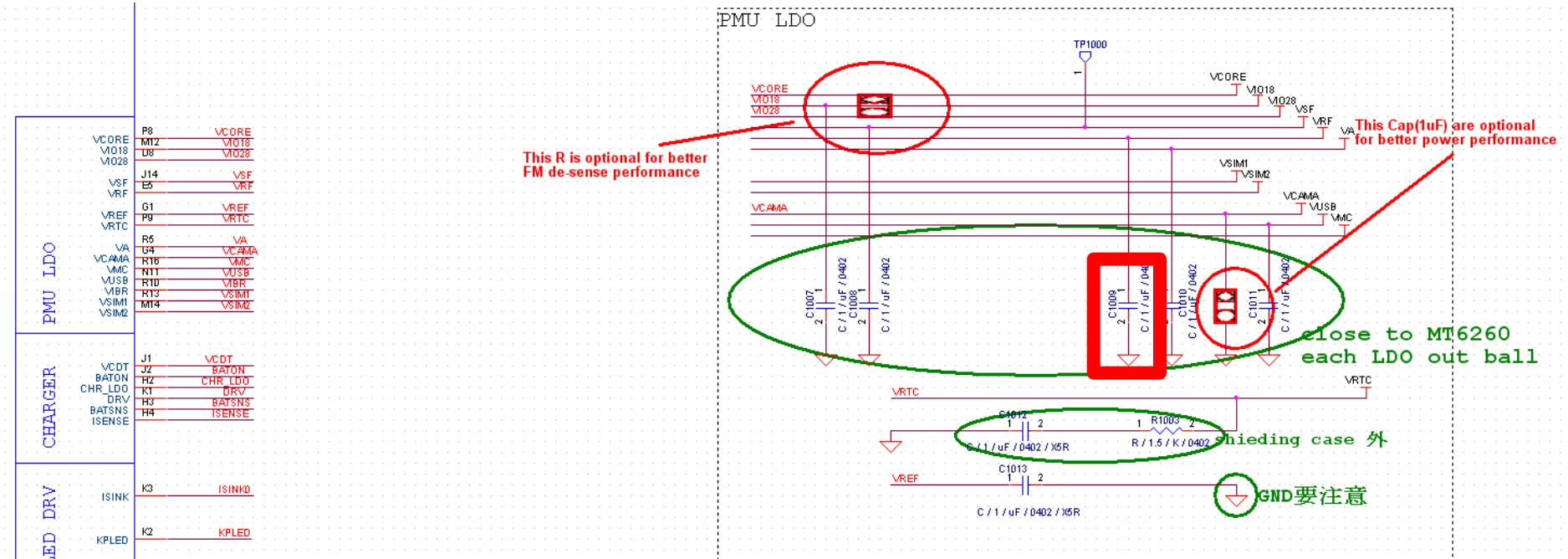
Reserve LC to close TXM for
RF performance

RX matching close to chip

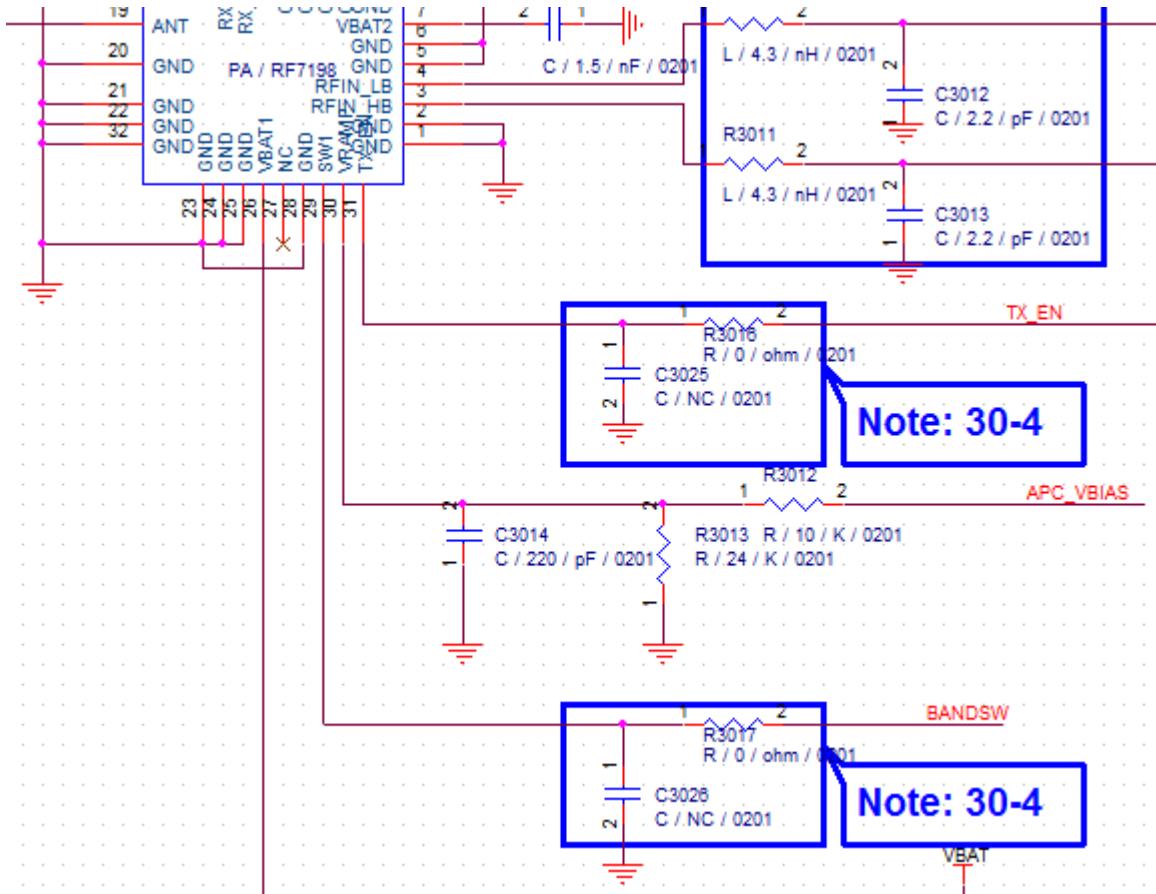


VRF

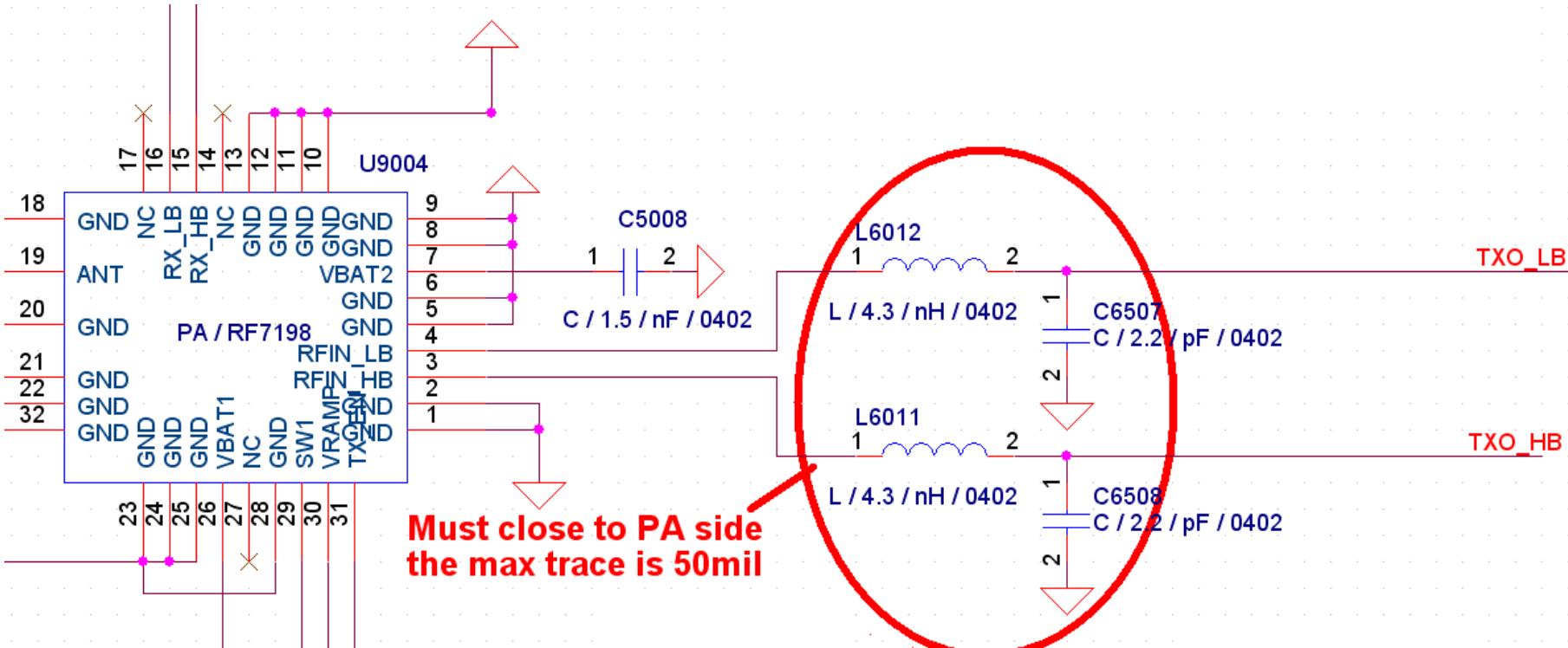
VRF Bypass Cap close to MT2503



BPI Decoupling Caps – Must Reserve



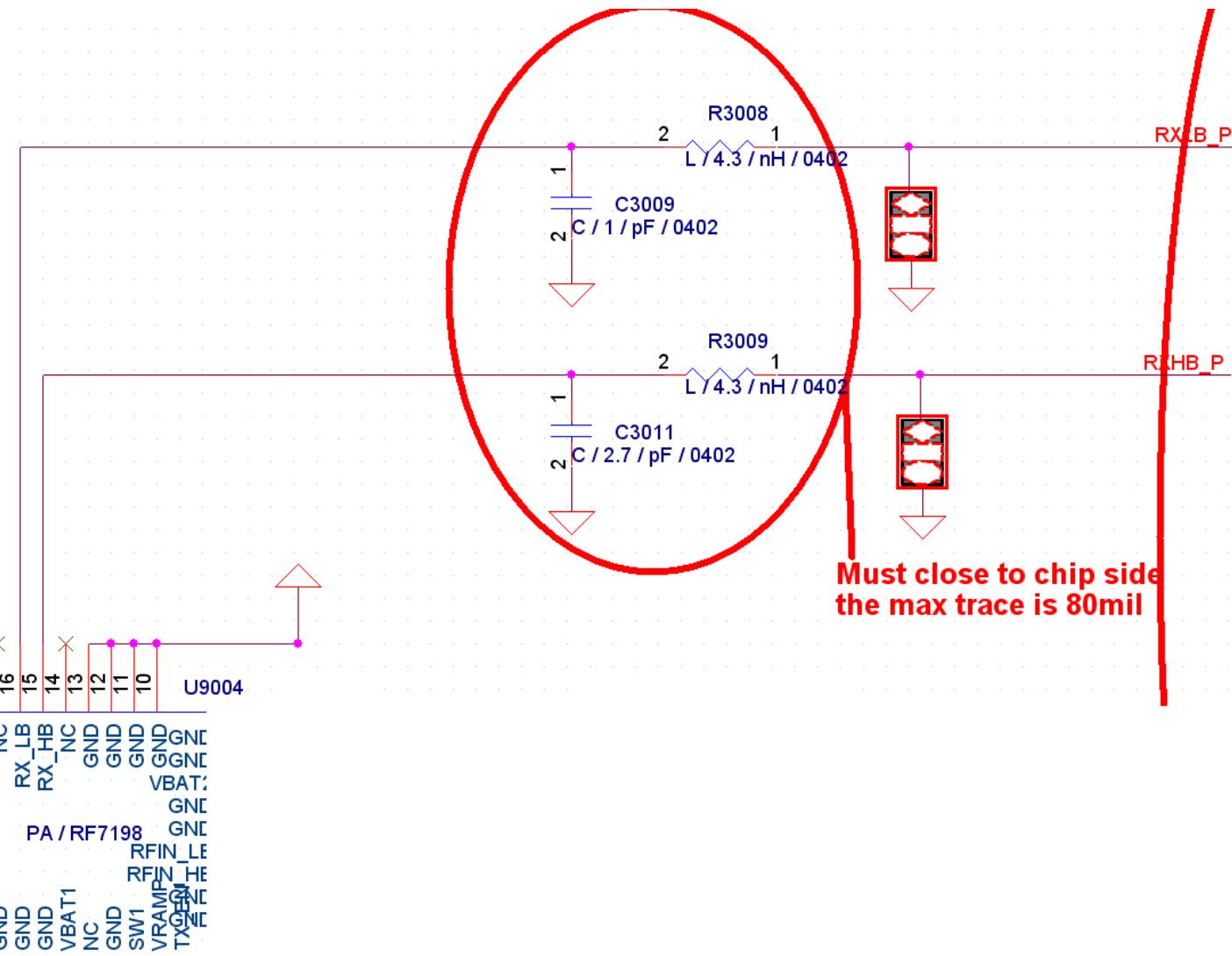
TX Matching – Must Have



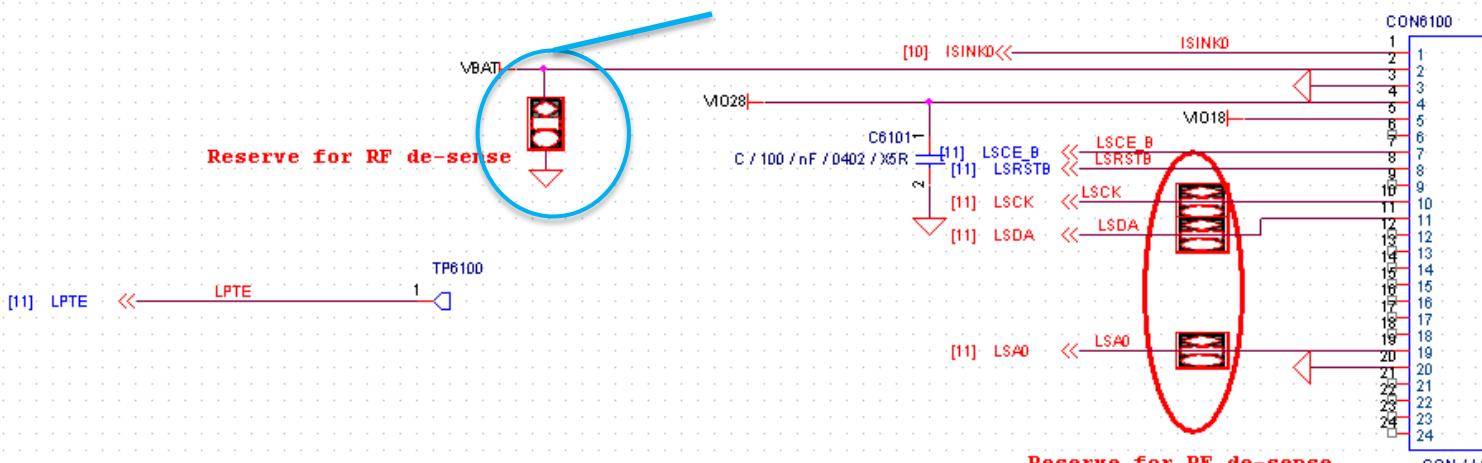
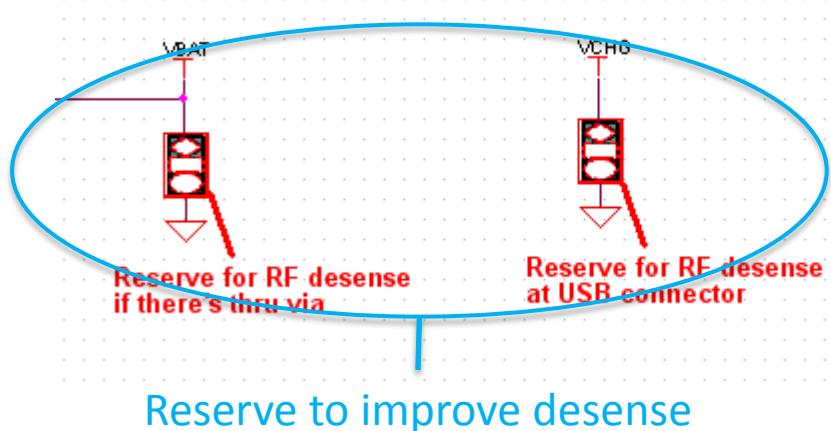
Matching components are “must have” for MP chips.

RX matching – Must Have

(Between MT2503 RX inputs and TXM RX ports)



RF Desense Improvement (Option)



RF Layout Rule(1/2)

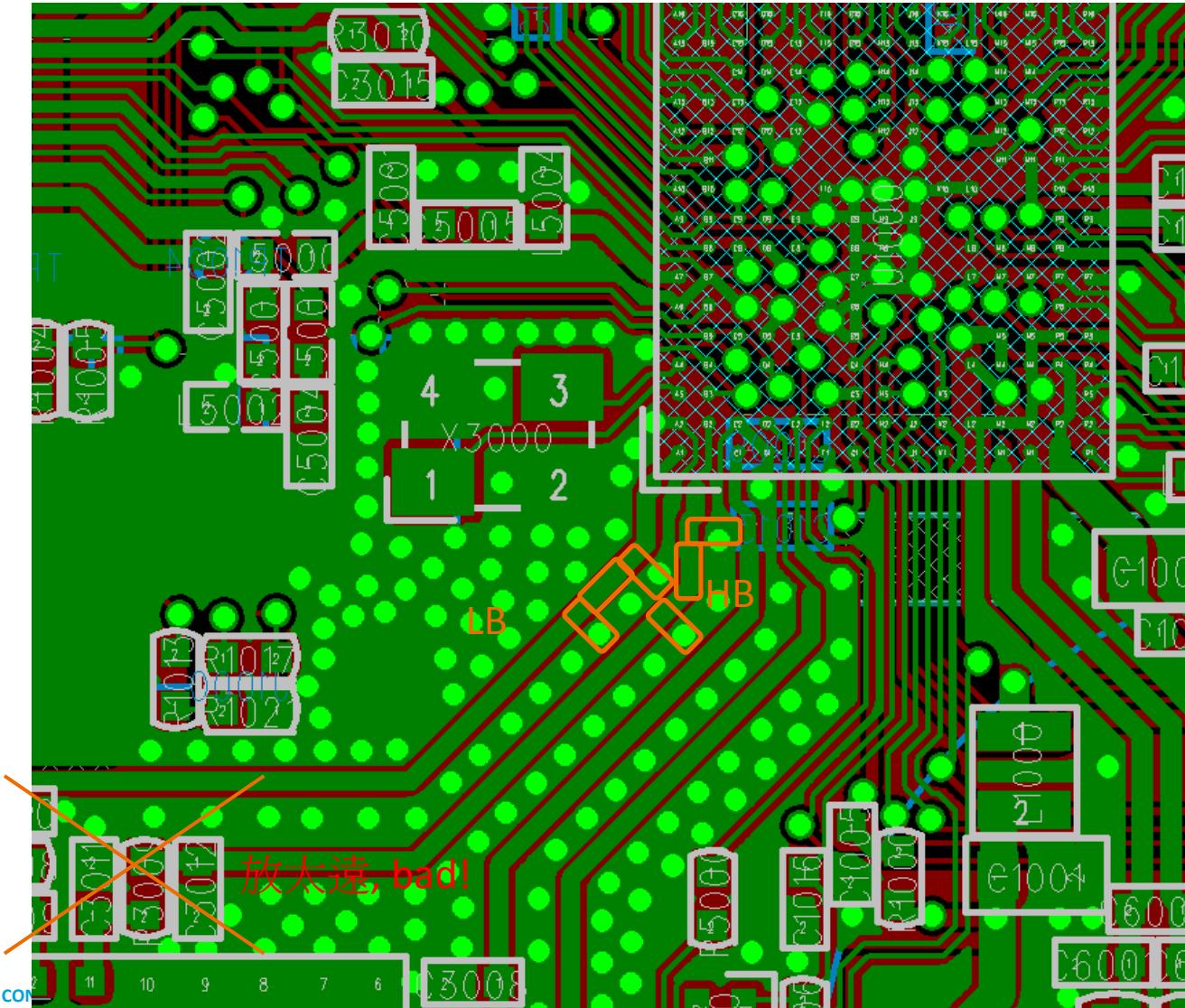
<input type="checkbox"/>	Crystal place as close as possible to MT2503PIN XTAL1/2 (B4,B5)
<input type="checkbox"/>	Because 2 pin DCXO , To avoid Xtal 1 Trace interference RF RX circuit and de-sense In PCB layout , suggest Xtal1 trace keep GND separate from RF RX .
<input type="checkbox"/>	Crystal and its trace directly refer to global ground , keep out L1&L2 ground if using 4-L PCB. No need keep out L2 if using 2-L PCB.
<input type="checkbox"/>	Crystal ground pin directly connect to global ground , do not connect to other layer GND
<input type="checkbox"/>	PIN FREF (C5) should be shielded in inner layer, and its via should keep far away from Pin XTAL1/2 (B4,B5) and their traces
<input type="checkbox"/>	When use FREF(C5) for WiFi , the trace should be shielded in inner layer individual and kept away from power trace. Besides, the length should be < 5cm
<input type="checkbox"/>	Control signals of ASM or Front-end Module do not cross the antenna port or PA outputs
<input type="checkbox"/>	Keep RF trace as 50Ω
	RX Trace must control at 50 ohm for better sensitivity.
<input type="checkbox"/>	Avoid TRX traces between MT2503 and TXM is too long. TXM and MT2503 place the same layer
<input type="checkbox"/>	RX trace between MT2503 and TXM must in surface layer, don't layout in inner layer.
<input type="checkbox"/>	Using GND wall with vias between RX trace and crystal (CPWG) to avoid 26MHz de-sense RX
<input type="checkbox"/>	Using GND wall with vias between RX trace and TX (CPWG) to avoid TX leakage coupling to RX
<input type="checkbox"/>	Using GND Wall with Gnd vias between TX and PMU part to avoid noise coupling to RX-SAW-less .

RF Layout Rule(2/2)

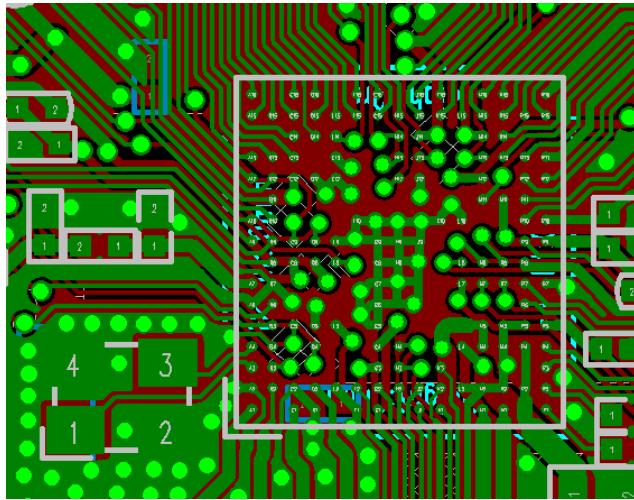
<input type="checkbox"/>	Avoid GND split under MT2503, especially for L2 (The L2 should be as completeness as reference layout !)
<input type="checkbox"/>	Place VRF (D1) bypass cap. as close as possible to MT2503
<input type="checkbox"/>	Place VA (P3) bypass cap. as close as possible to MT2503
<input type="checkbox"/>	Use inner layer and ground to protect APC(N7) trace, and do not parallel overlap with other trace.
<input type="checkbox"/>	For Camera, LCM, and MSDC, the clock and data should have better GND protection. Avoid power trace or other trace routing parallel with clock and data.
<input type="checkbox"/>	Place memory as close as possible to MT2503
<input type="checkbox"/>	BPI control line need good ground shielding. BPI pins must reserve shunt caps close to PA/FEM
<input type="checkbox"/>	PA VBAT should go star connection and individual routing. PA VBAT bypass cap 22uF & 39pF should be close to PA as possible.
<input type="checkbox"/>	Memory should be well shielded by shielding case and away with ANT, avoid desense problem

RX Matching Placement Suggestion

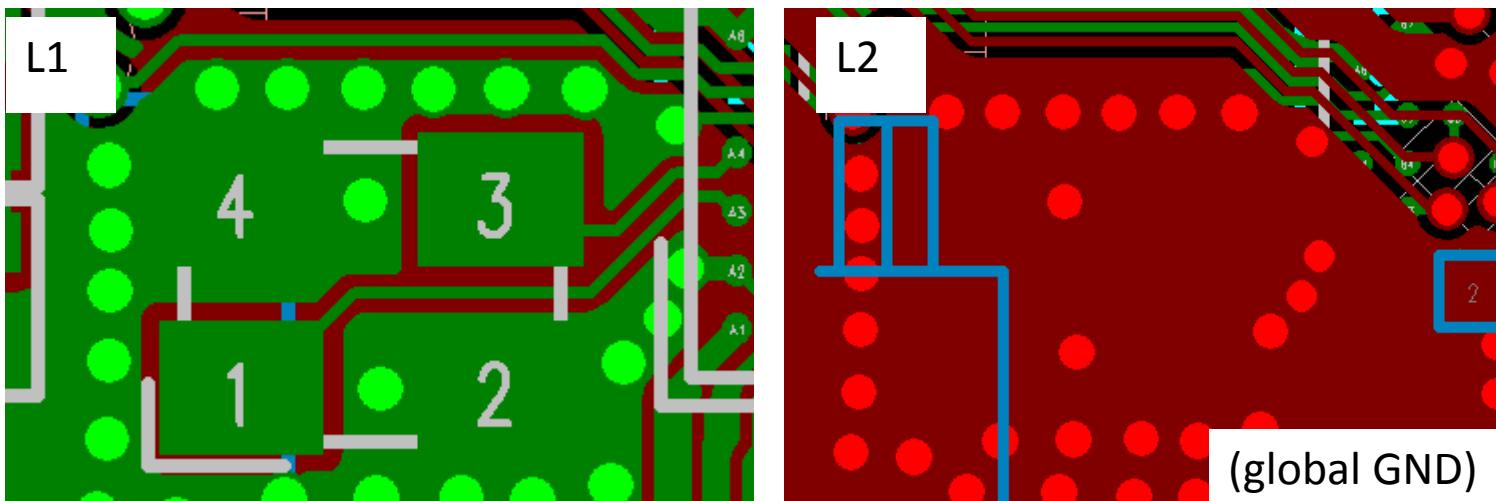
RX matching placement as blow, distance to IC < 2mm(80-mil):



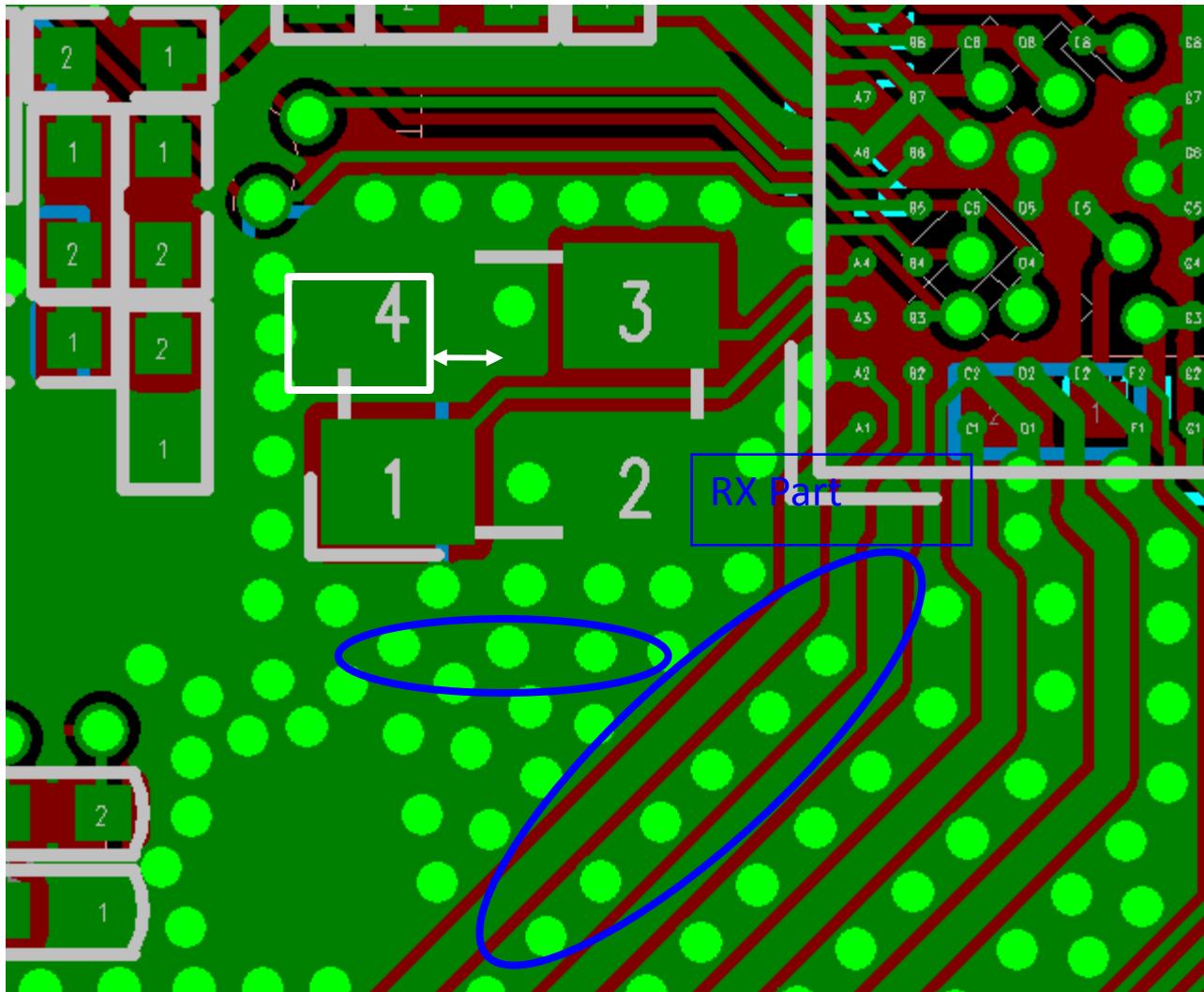
- Crystal place as close as possible to MT2503 PIN XTAL (B4/B5)



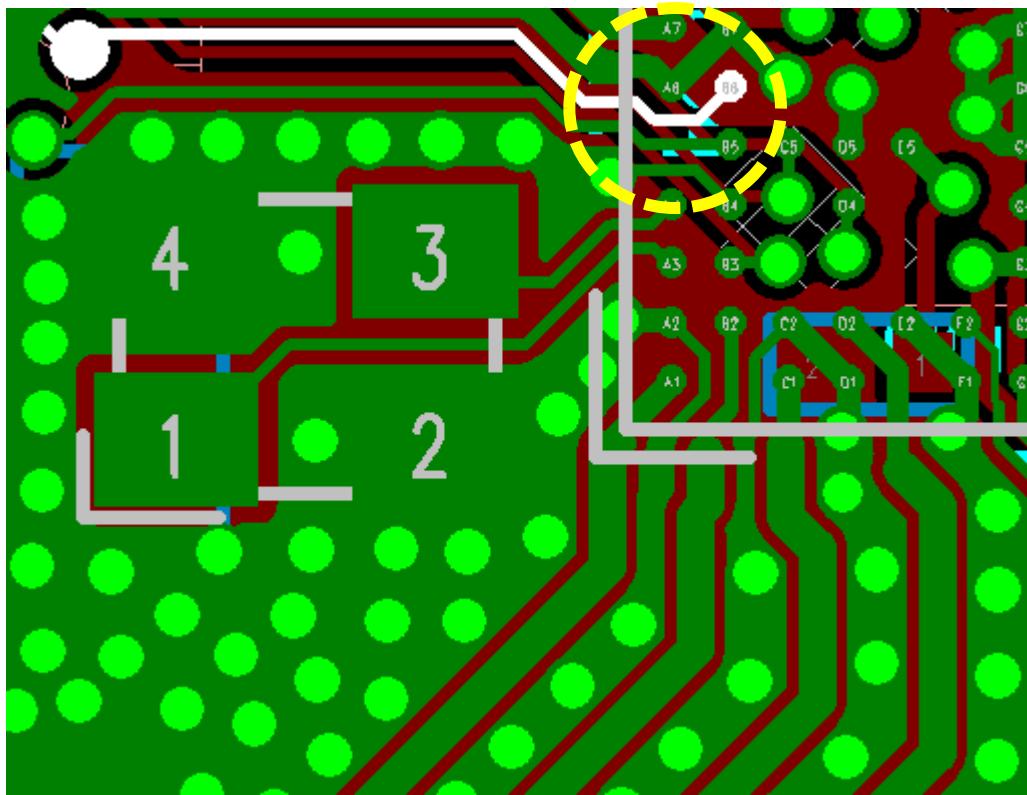
- Crystal and its trace directly refer to global ground.
- Crystal ground pin directly connect to global ground , do not connect to other layer GND



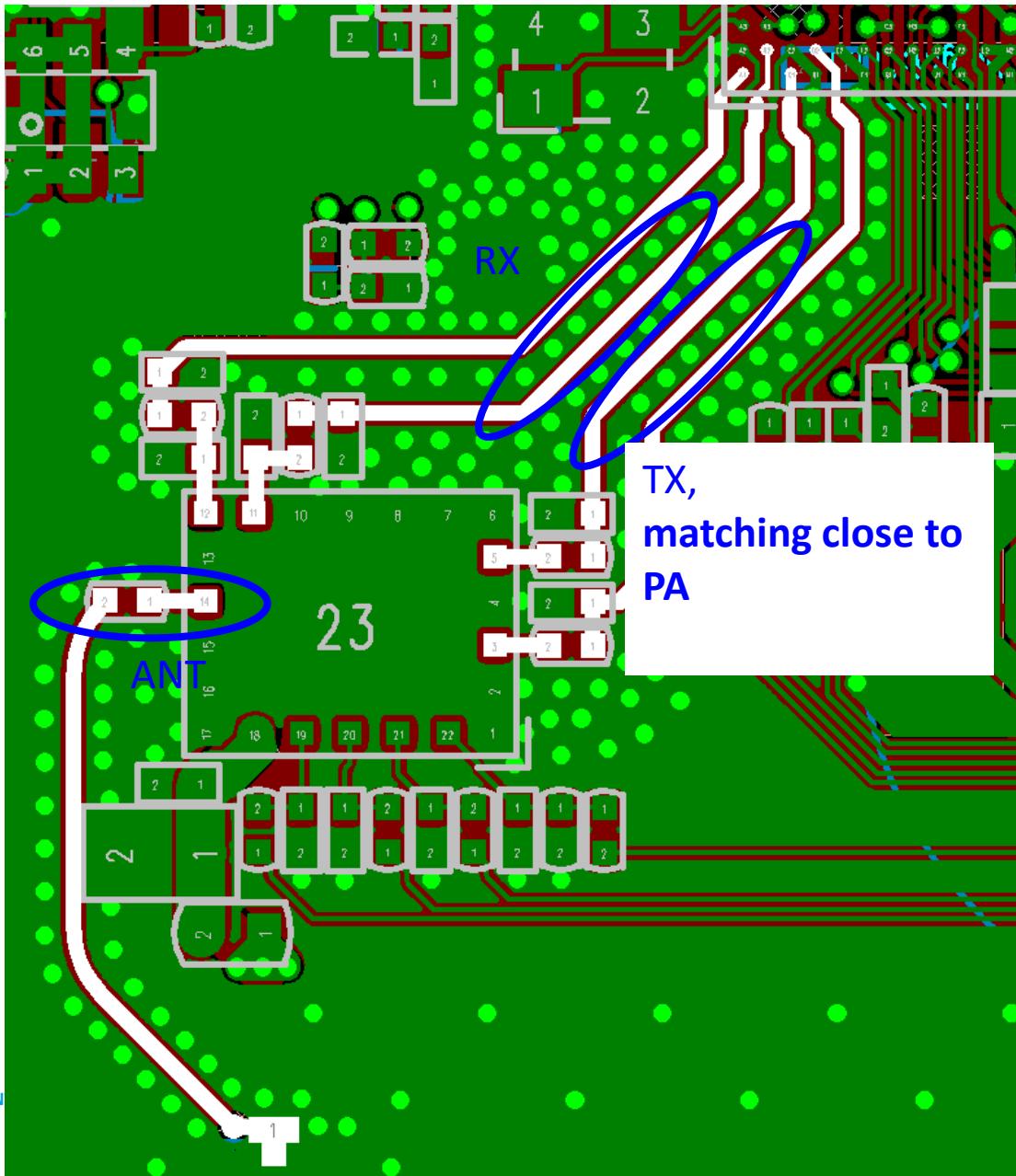
- Crystal must add GND to avoid 26MHz de-sense RX



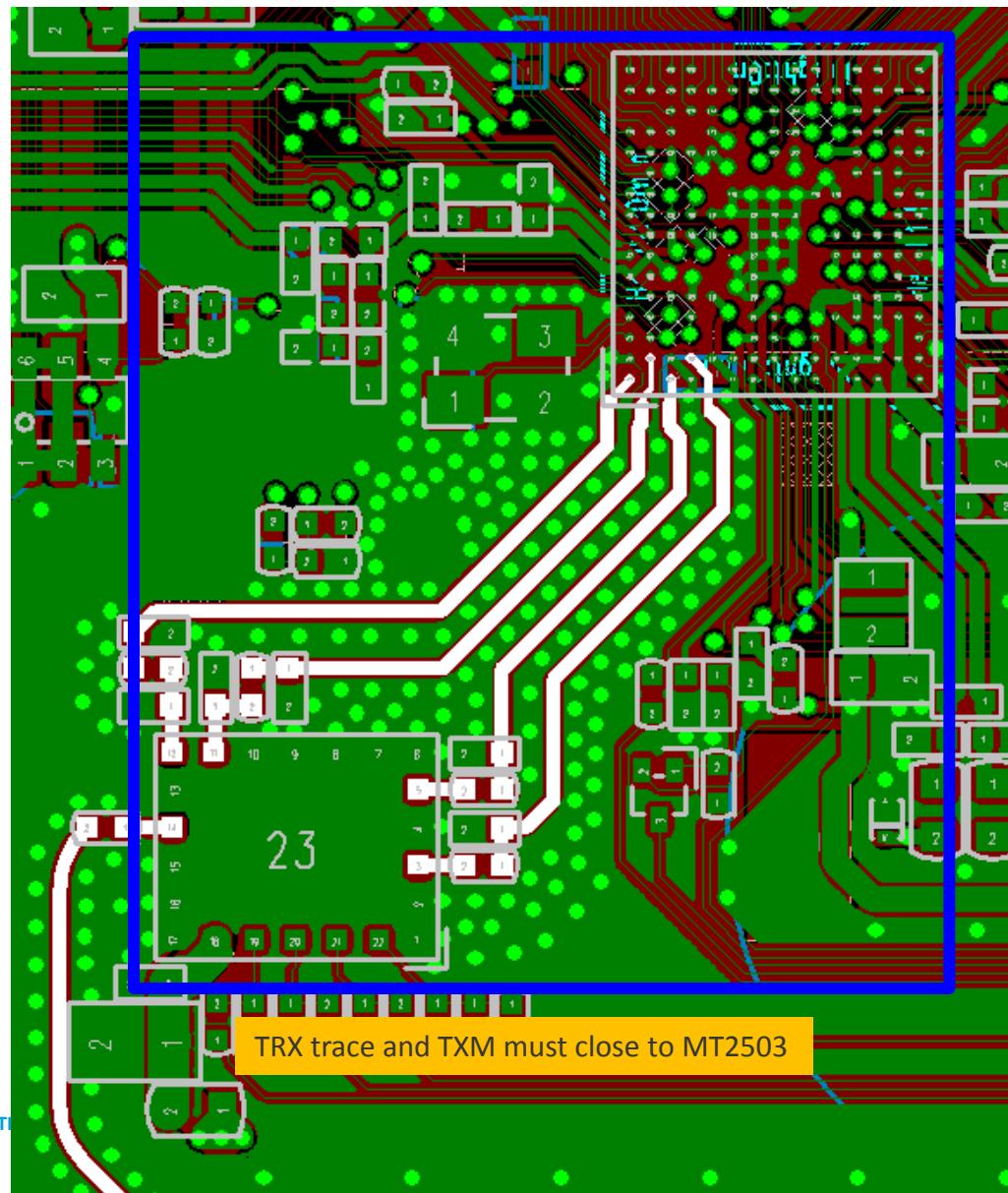
- PIN FREF1 (C5) and should be shielded in inner layer



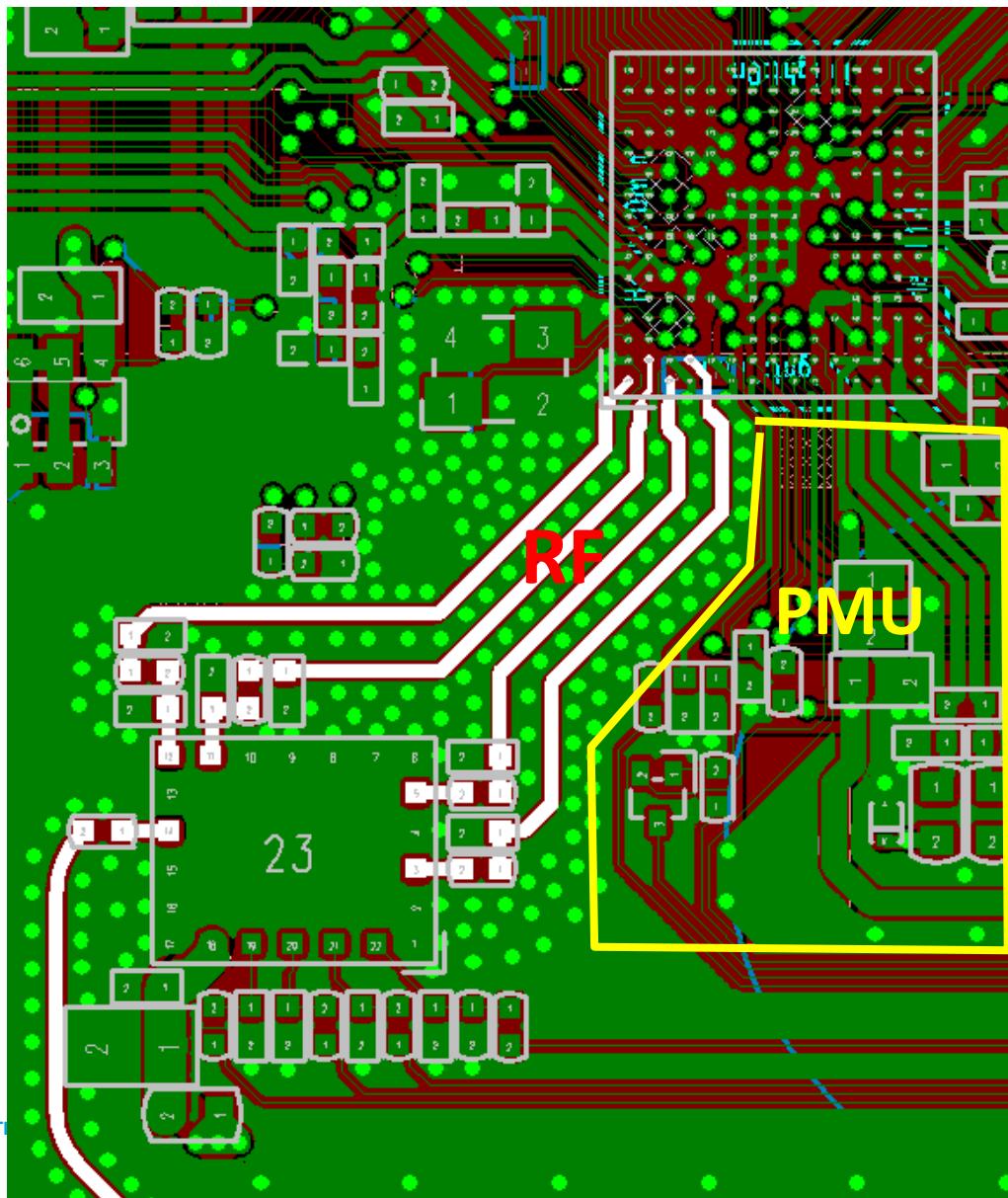
- Keep TX and RX singled ended RF trace good 50Ω

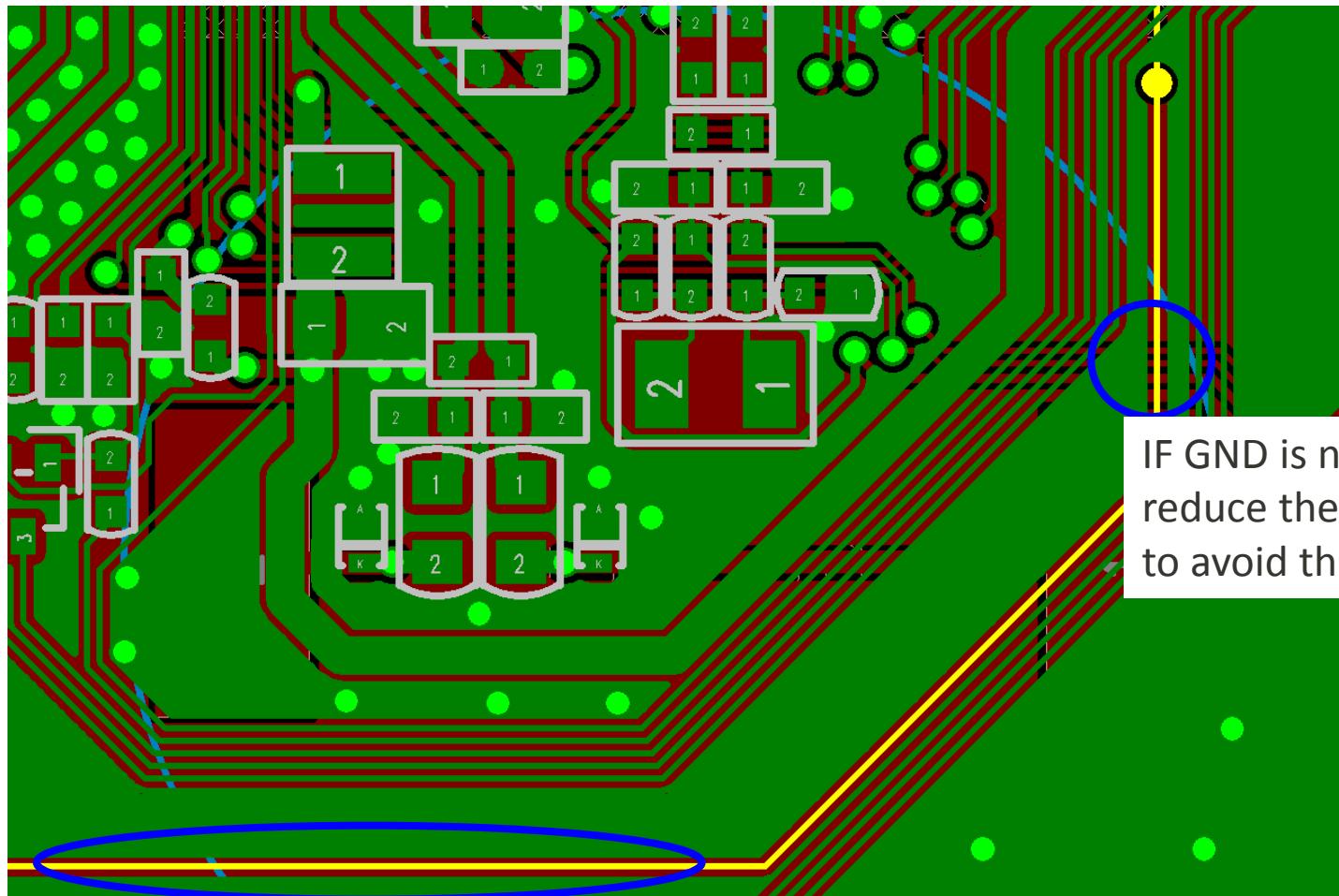


- Avoid TRX traces between MT2503 and TXM is too long.TXM and MT2503 place the same layer



- Using GND Wall with GND Vias between RF and PMU part to avoid noise coupling to RX-SAW-less .

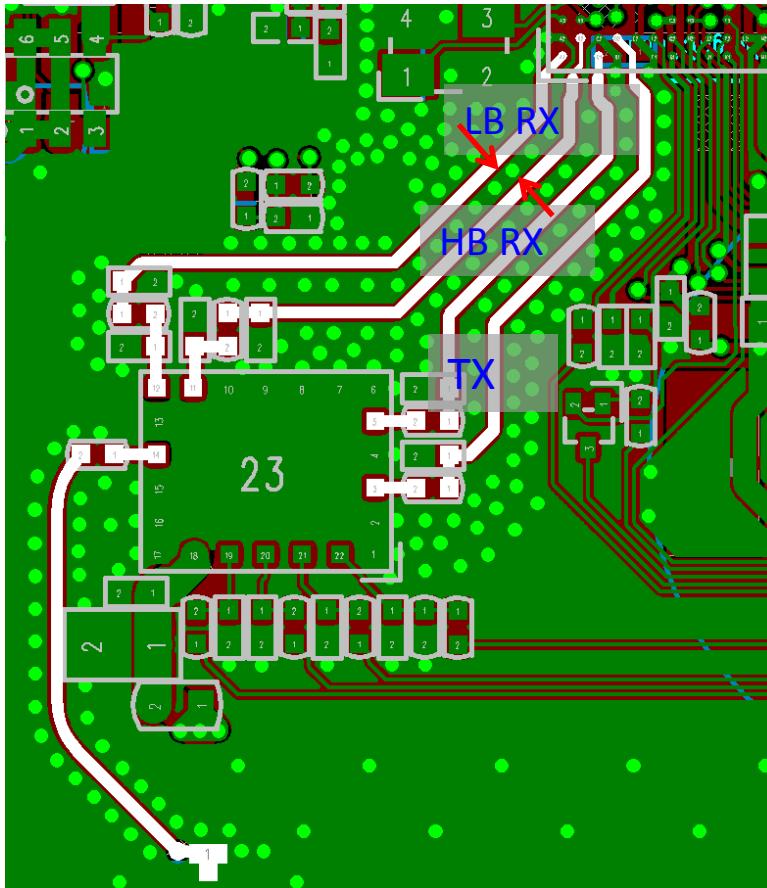


VAPC shielding by GND

IF GND is not good, it can
reduce the overlap area of VAPC
to avoid the parallel overlap

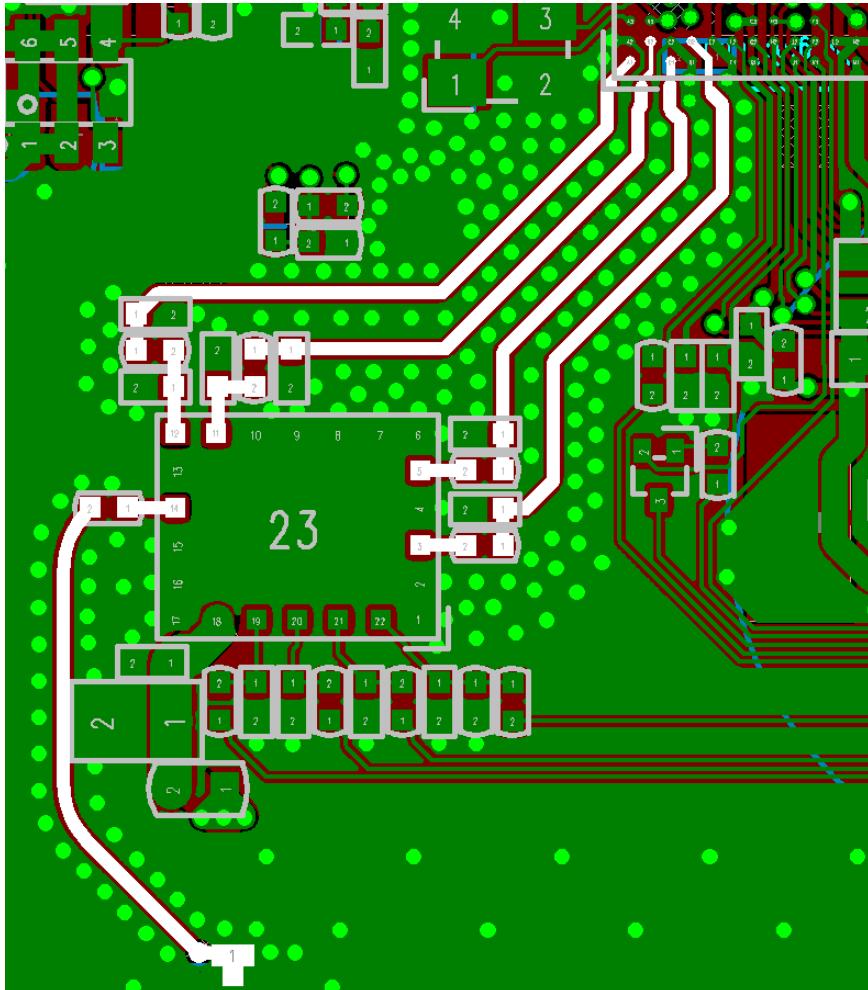
❑ Separate the LB and HB RX for 4L (for CPW / CPWG)

- ◆ For 4L, CPW or CPWG is preferred. The spacing between LB and HB RX can be reduced using the ground strip with via-holes (Spacing will be $< 3*W$).



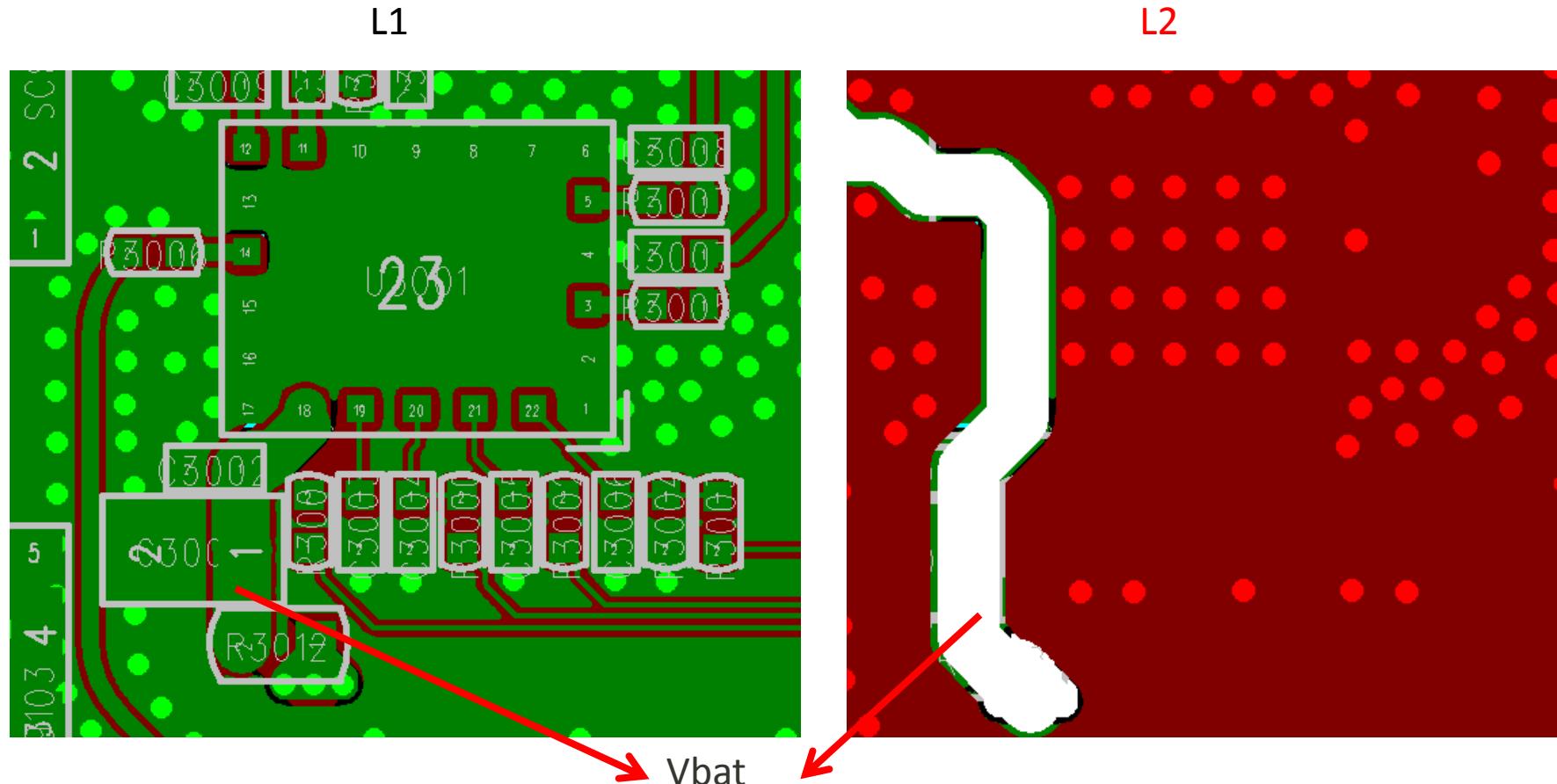
Keep good property of RX trace

- ◆ The **length of RX trace** should be smaller than 20mm (include component)
- ◆ Keep all the traces **on top layer**, do not route in inner layer



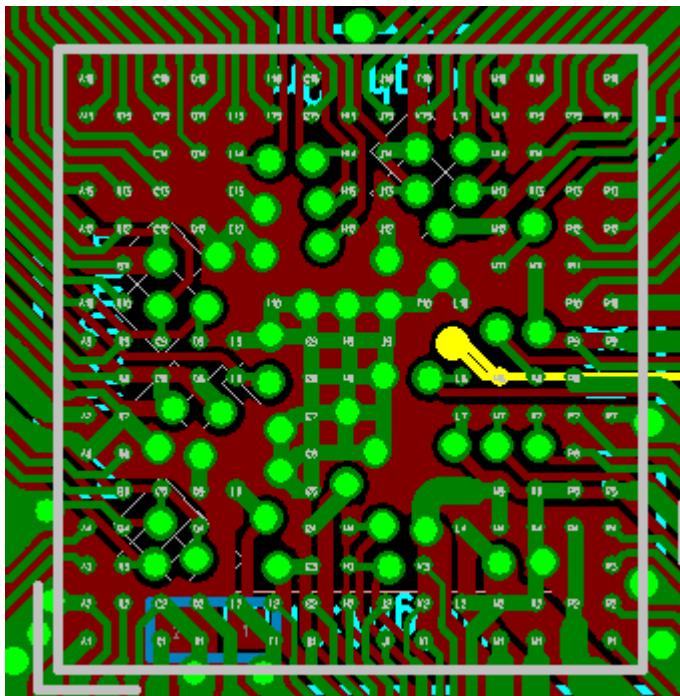
□ Vbat trace placement

- ◆ The Vbat trace may be placed under the PA for easy layout requirement.
- ◆ The ground (L2) under the RF trace must be complete.

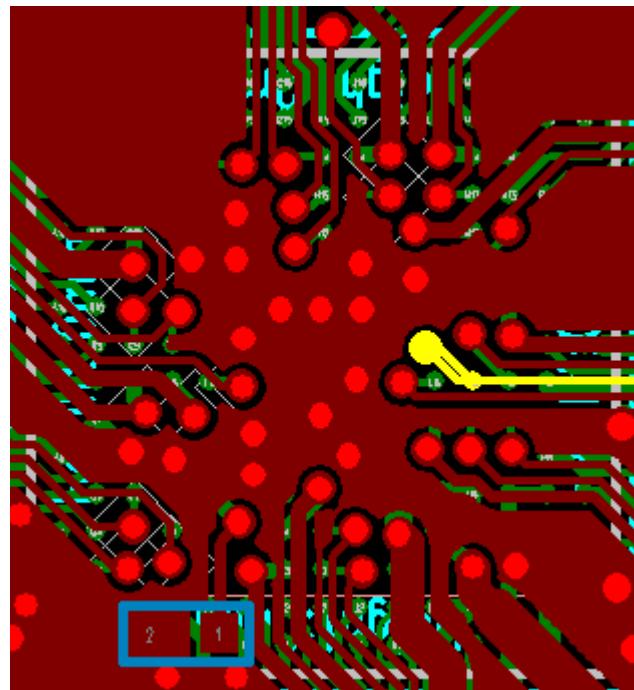


- Avoid GND split under MT2503 , especially for L2

L1

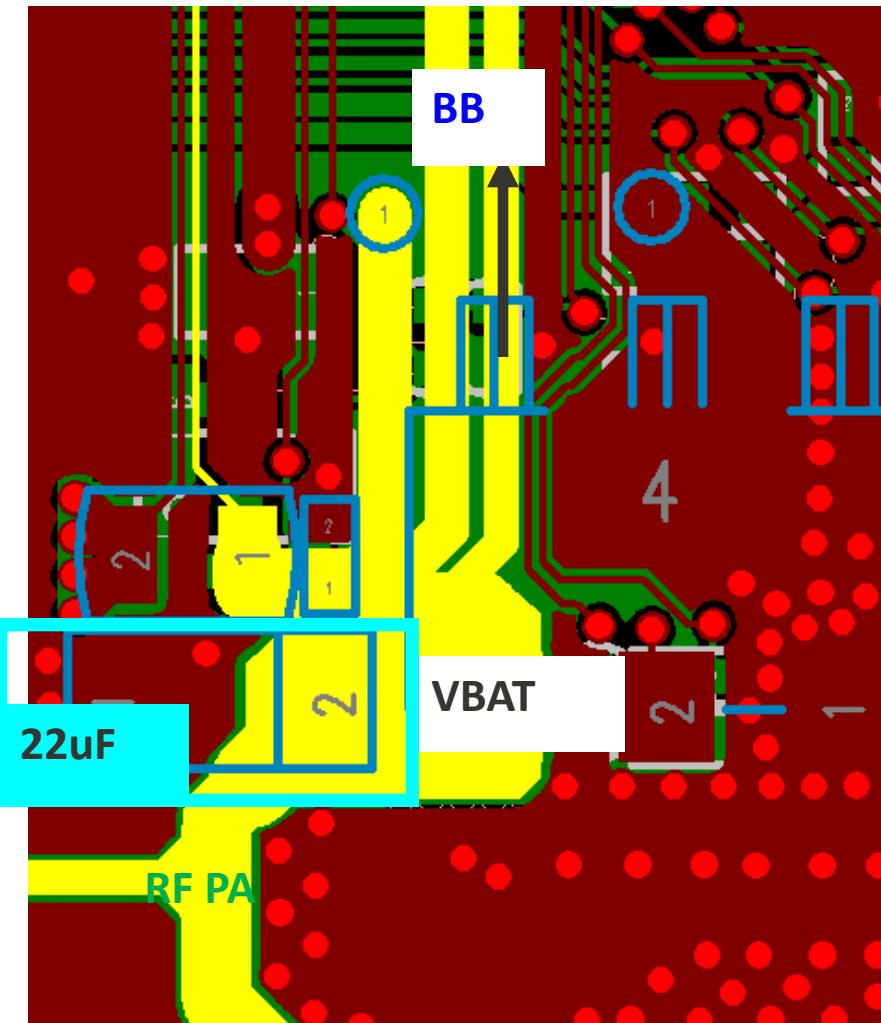


L2

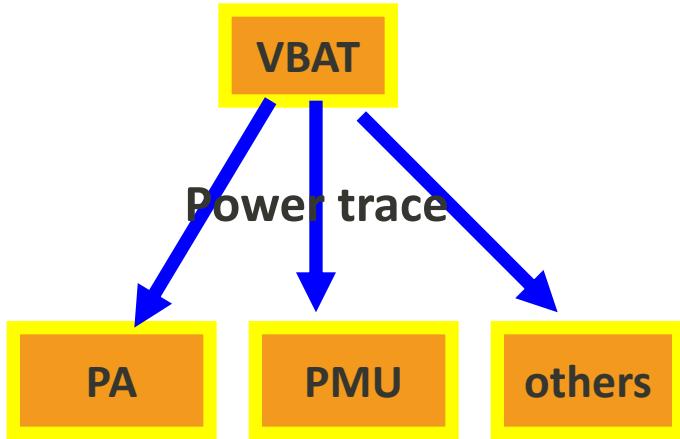


- Place VRF (D1) bypass cap. as close as possible to MT2503
- For Camera, LCM, and MSDC, the clock and data should have better GND protection. Avoid power trace or other trace routing parallel with clock and data.
- Place memory as close as possible to MT2503
- BPI control line need good ground shielding

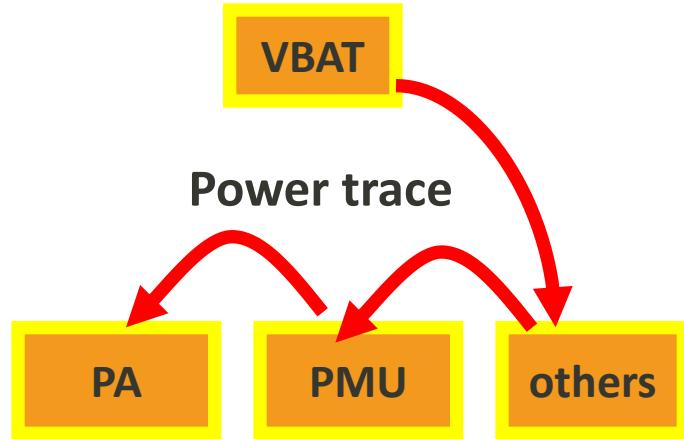
- PA VBAT should go star connection and individual routing. PA VBAT bypass cap 22uF should be close to PA as possible.



Power Trace



Star Connection (GOOD)



NOT Star Connection (BAD)

MT2503+RFMD7198

Design Note

- The GND under the module should be connected to become a GND pad.
 - GND pins shall be connected to the pad GND as well (Pin 1, 2, 5, 6, 8 to 13, 18, 20 to 25, and 28).

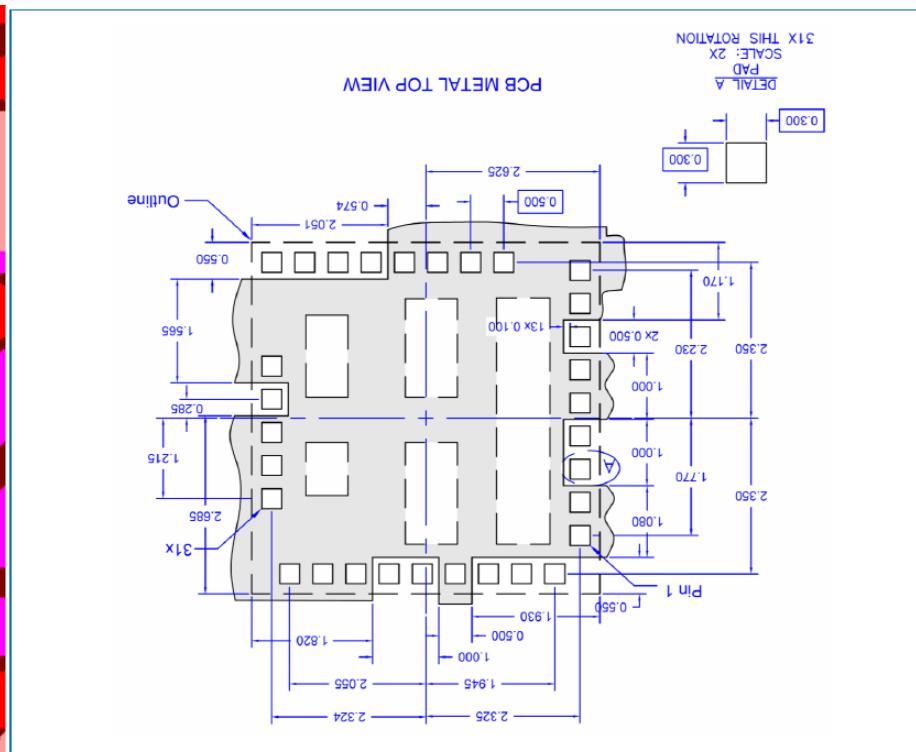
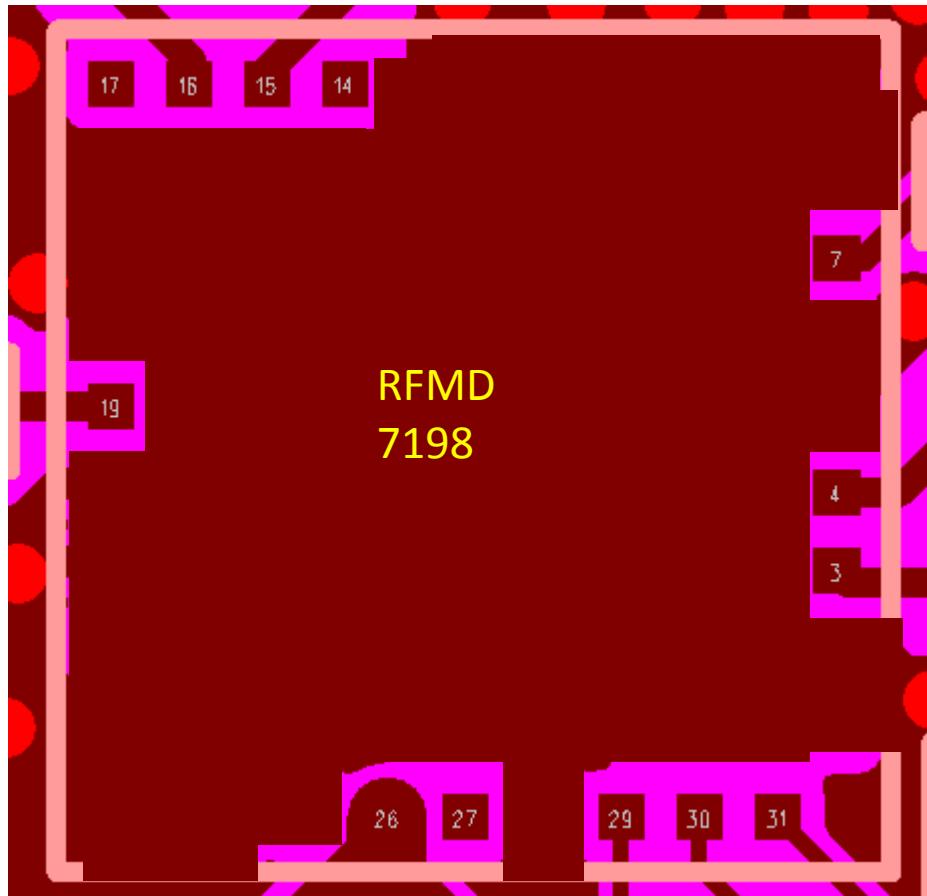
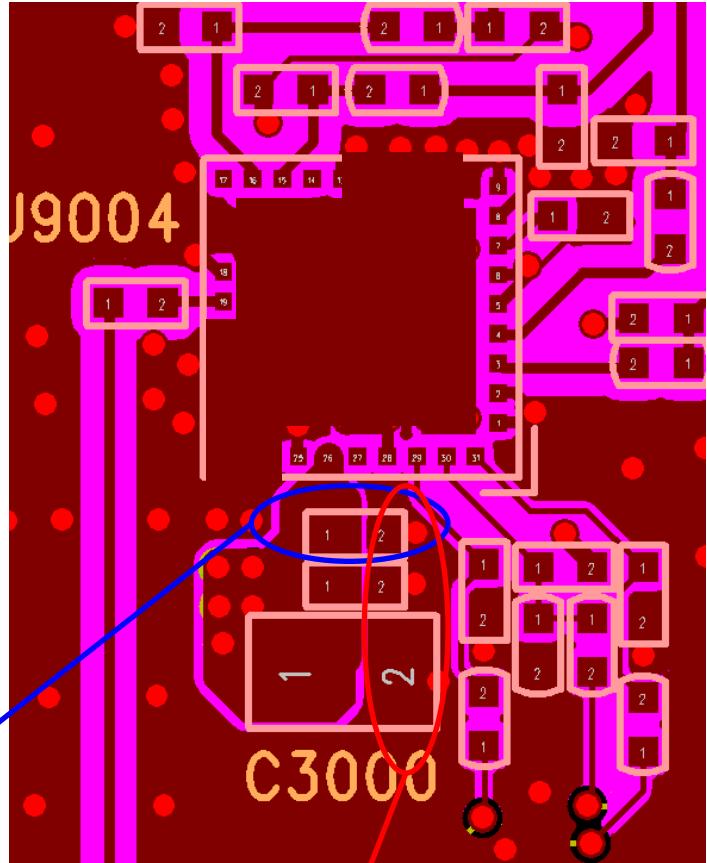
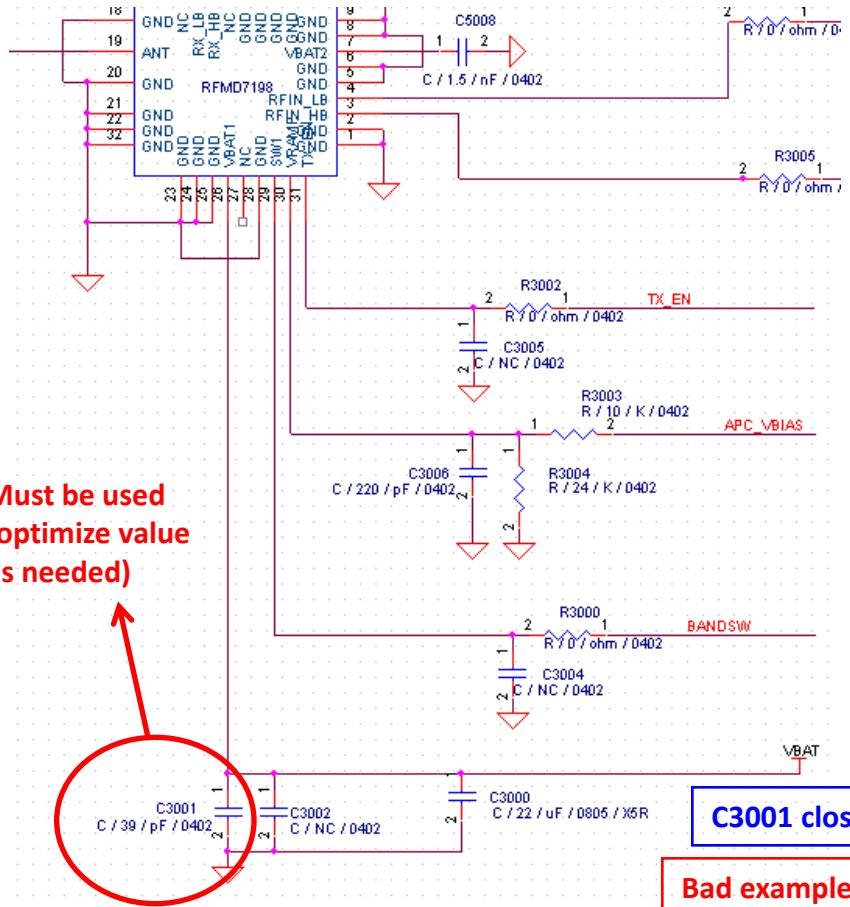
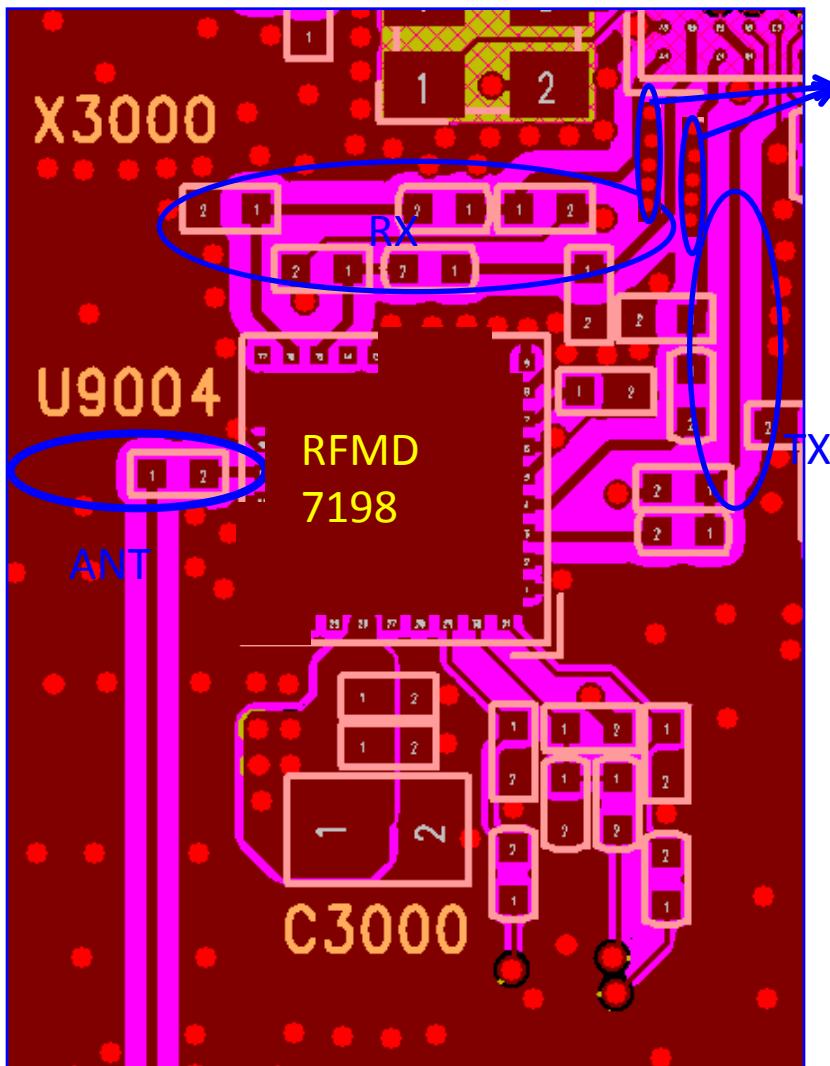


Figure 2. Recommended PCB top metal layer.

- Decoupling capacitors C3000 and C3001 on Vbat line are required.
- Capacitor C3001 must be close to TXM as much as possible.

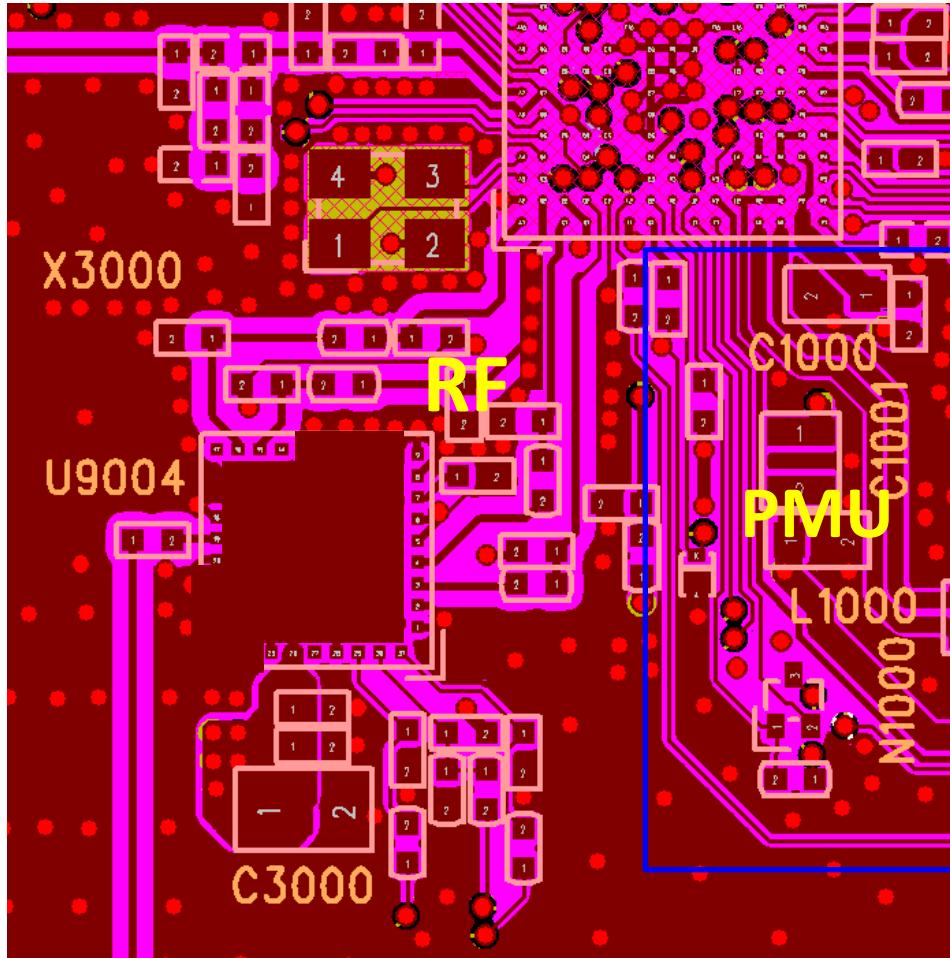


- Keep TX and RX singled ended RF trace good 50Ω



GND shall be added to avoid Xtal harmonics coupling to TX traces from RX traces, especially RXHB . The coupling interference may cause ORFS_Mod degradation.

- Using GND Wall with GND Vias between RF and PMU part to avoid noise coupling to RX-SAW-less .



MT2503 De-sense Design Note

De-sense Layout Rule

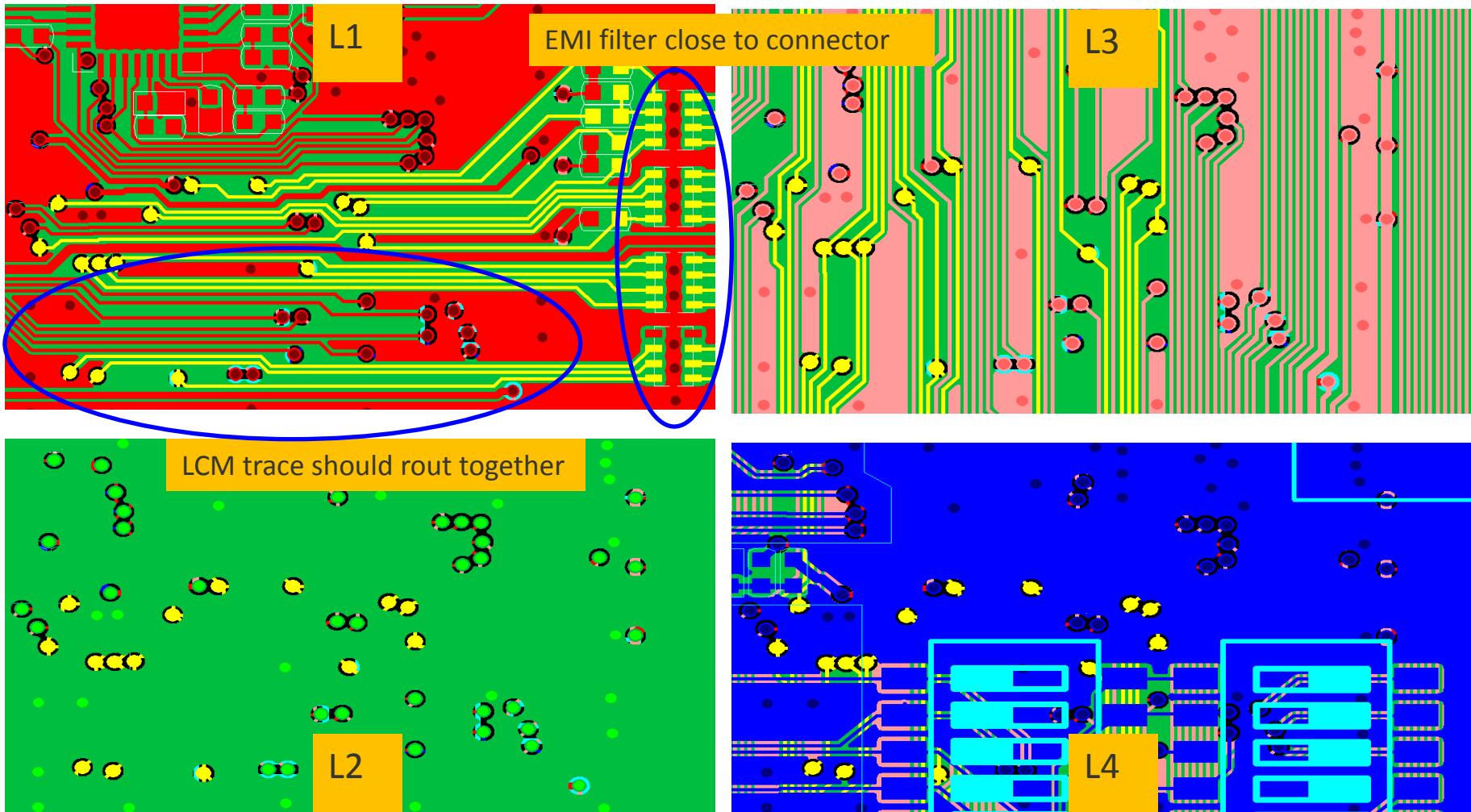
MUST Read

LCM	LCM data traces (ex: LCD_DB0~DB8) should rout together and prevent cross or parallel with other traces to couple noise
	LCM EMI filter should close to LCM connector
	LCM connector GND pin should connect to GND to prevent noise
	LCM back GND should contact to main GND with good contact
Camera	Camera data traces (ex: LCD_DB0~DB8) should rout together and prevent cross or parallel with other traces to couple noise
	CMMCLK and CMPCLK should use Guard trace to prevent CLK couple to other trace
	CMMCLK should reserve RC and close to MT2503
	CMPCLK should reserve RC and close to camera module
	Camera data pin which reserve EMI filter should close to camera module
MSDC	MSDC data traces (ex: LCD_DB0~DB8) should rout together and prevent cross or parallel with other traces to couple noise
	MSDC data pin which reserve EMI filter should close to MSDC connector
	MCCLK which reserve RC should close to MT2503
Memory	VSF should shunt a cap which close to Flash to prevent Flash noise couple to power trace
	Memory should be perfect as possible to achieve good return path
	Memory should close to main IC and with good GND, and prevent Flash trace which with noise couple to other trace
Charge Pump	FLYN, FLYP, VBOOST which GND under L2/L3 should be separate to prevent desense
	The cap of FLYN, FLYP, VBOOST should close to MT2503
26MHz Buffer	FREF1 Trace should rout in inner layer and use Guard trace to protect 26MHz desense

- Please note:

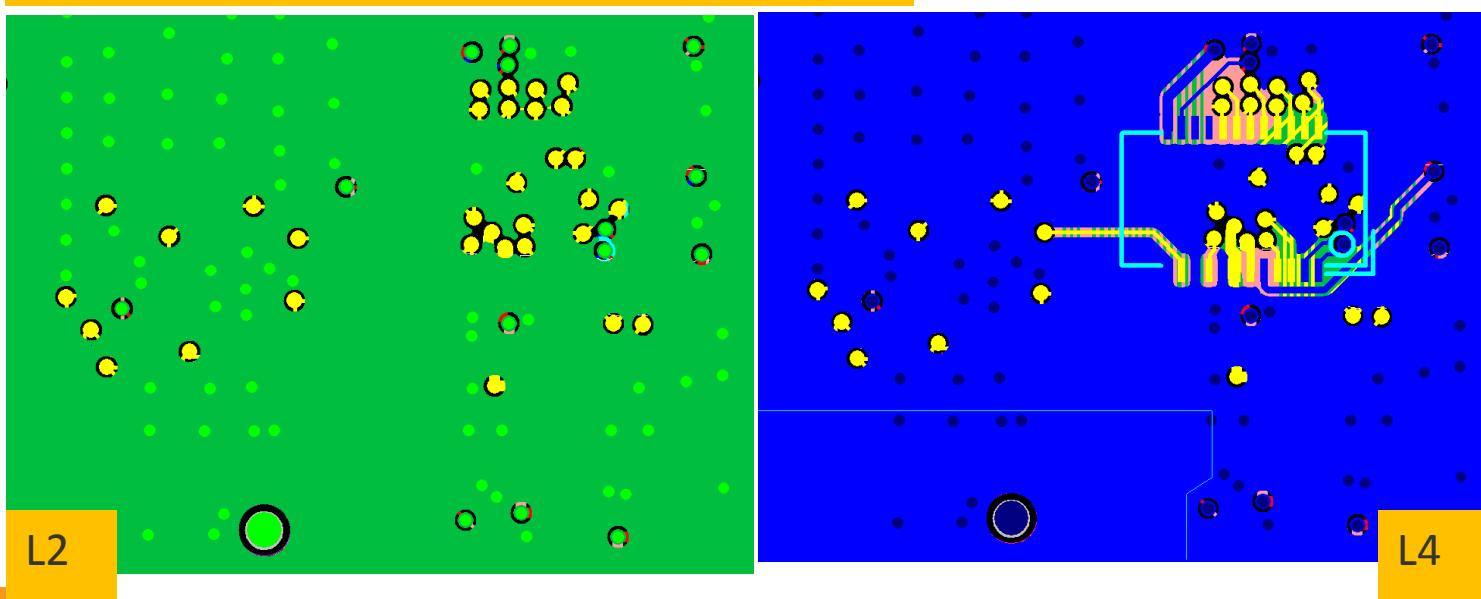
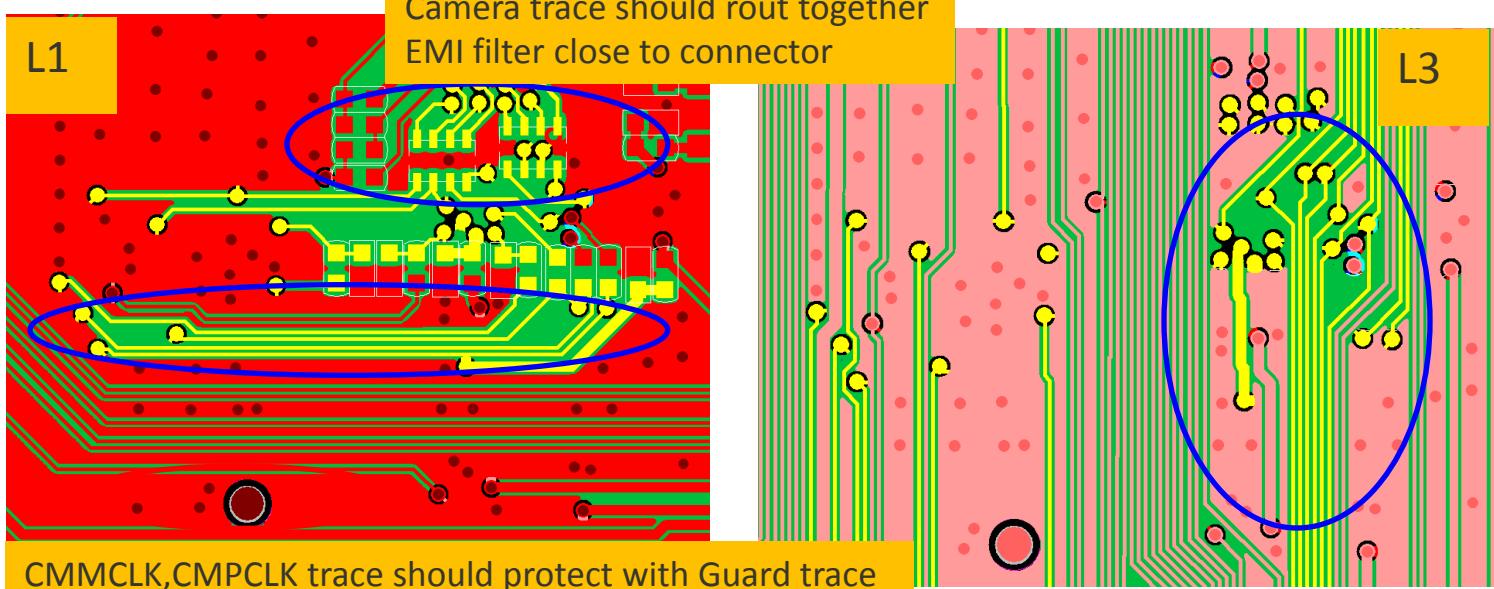
If customer has de-sense concern, 4-L PCB is suggested, de-sense design note here is taking 6260 4-L PCB as example

LCM (with good Gnd protection)

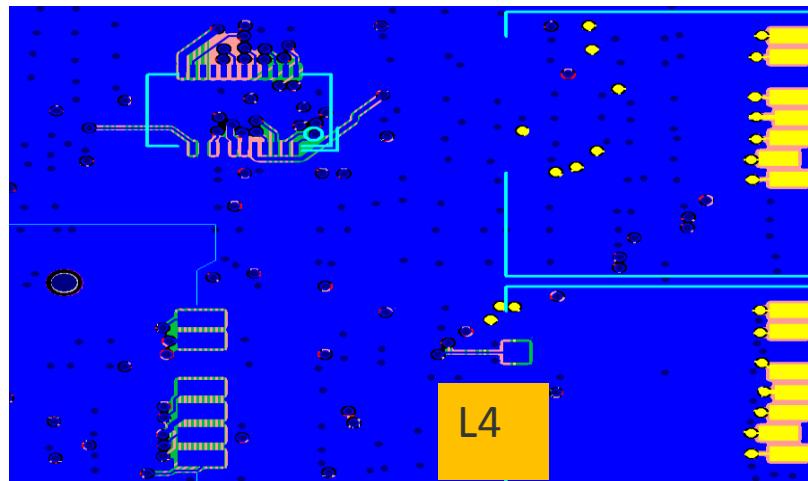
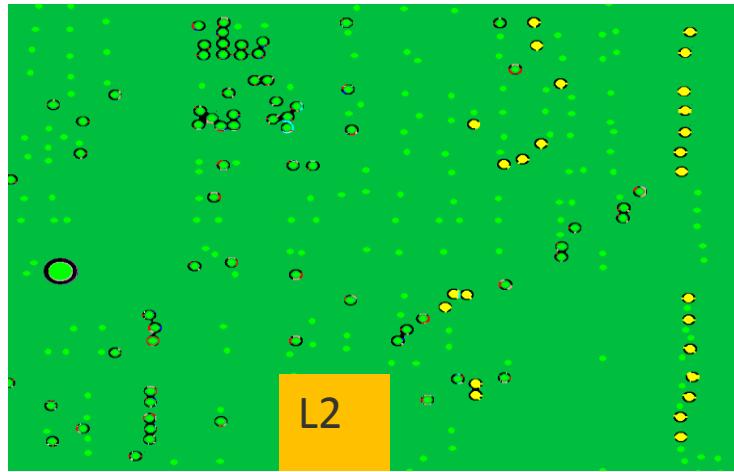
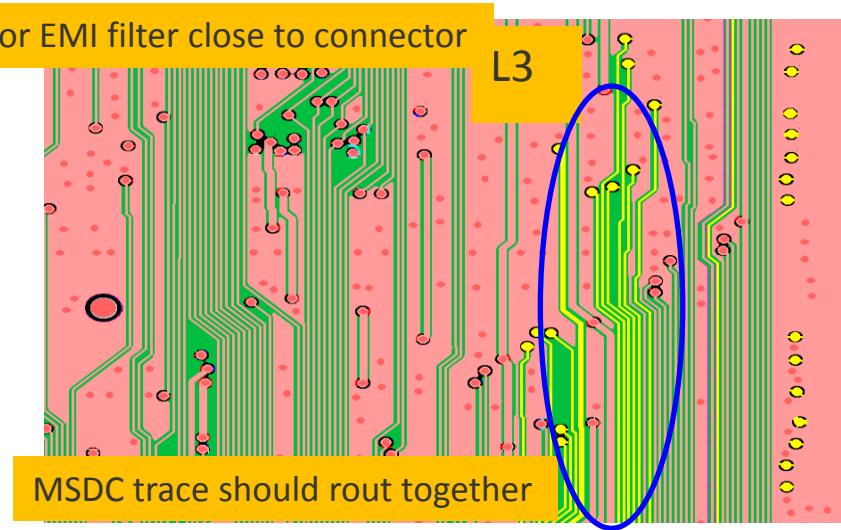
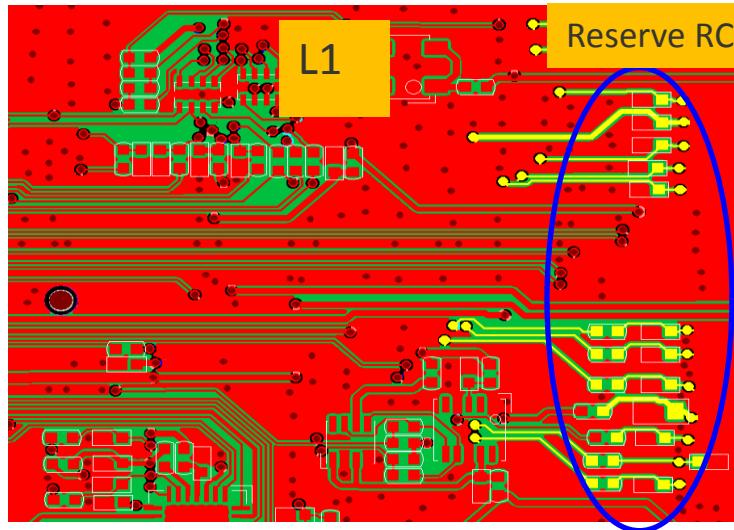


* LCM back GND plane should connect with Main GND

Camera

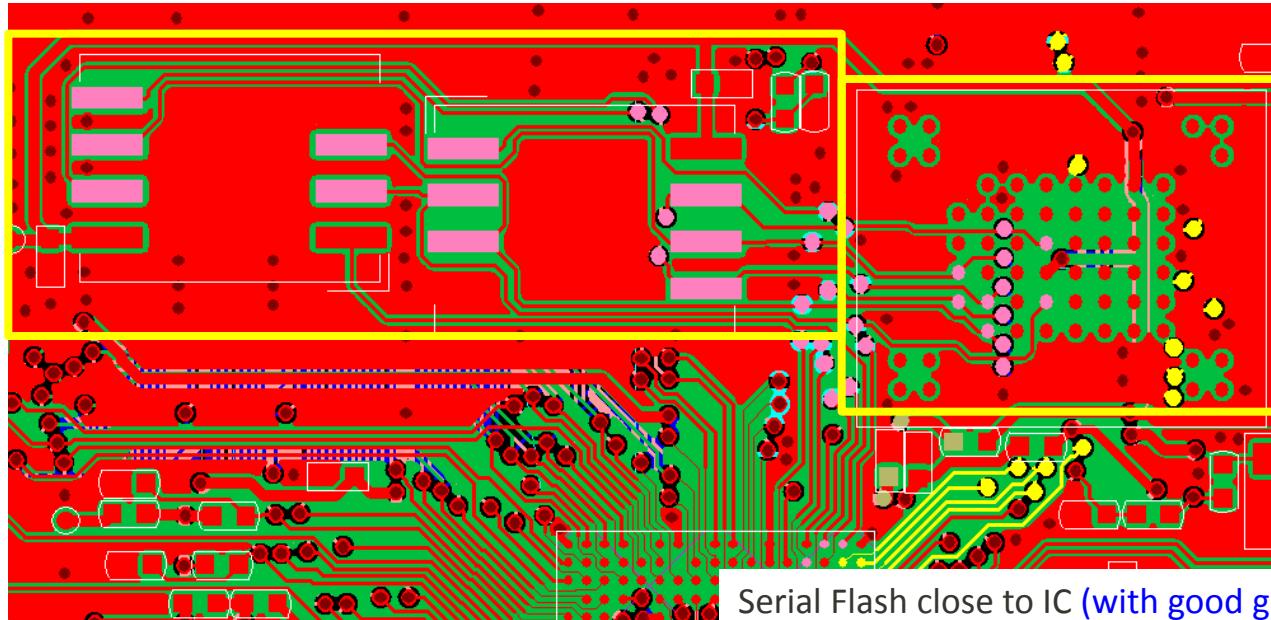


MSDC



Flash

L1



Serial Flash close to IC (with good ground return)

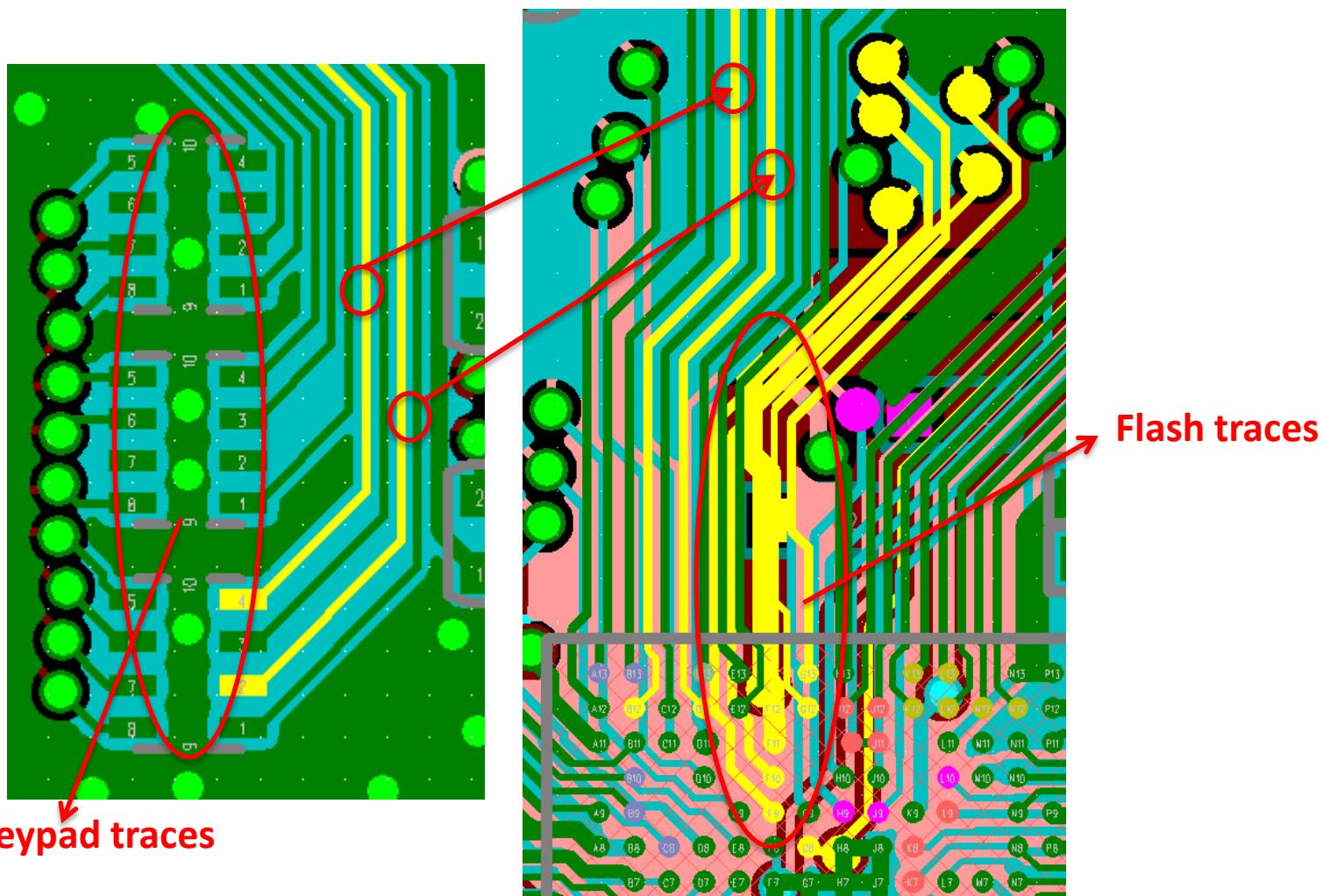
As short as possible to prevent the noise couple to other trace

L2



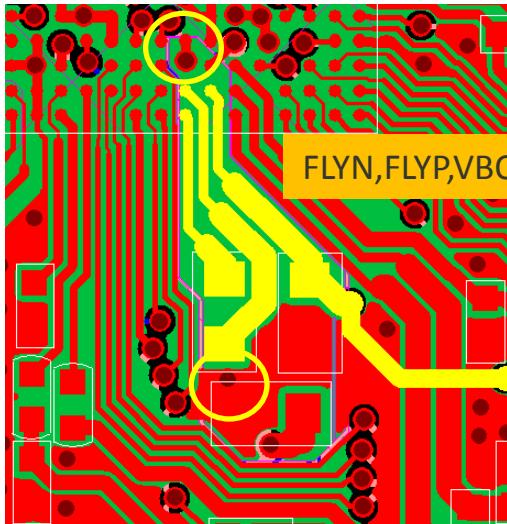
Flash (cont)

If layout cant prevent coupling, it should be reserved the EMI filter Pad, EX: Keypad traces



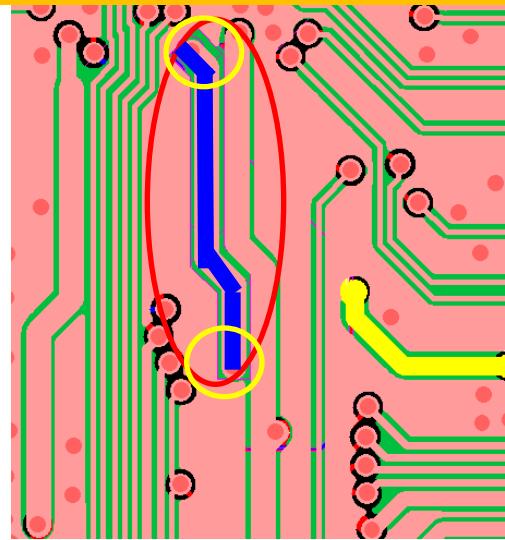
Charge Pump

L1



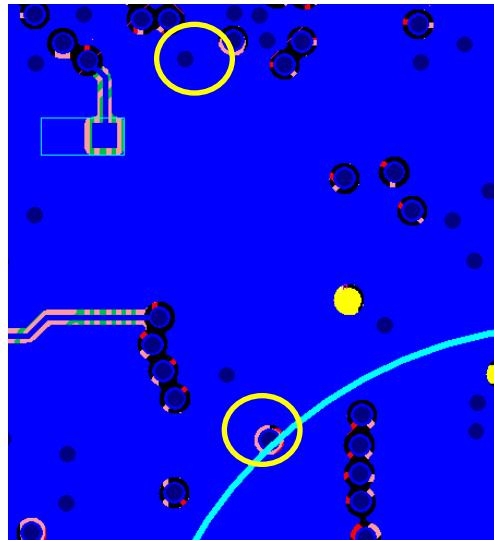
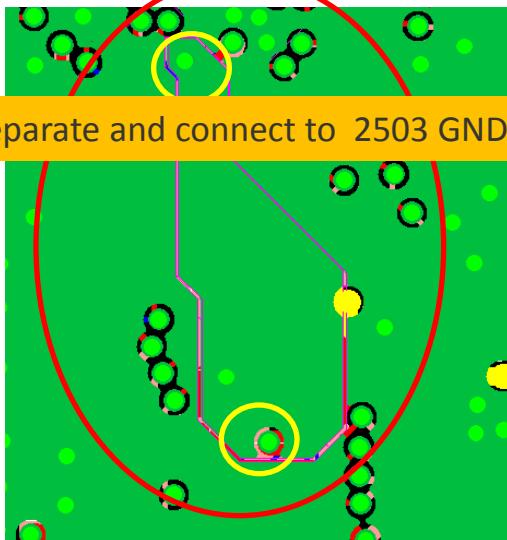
Separate GND, connect to MT2503 GND

L3



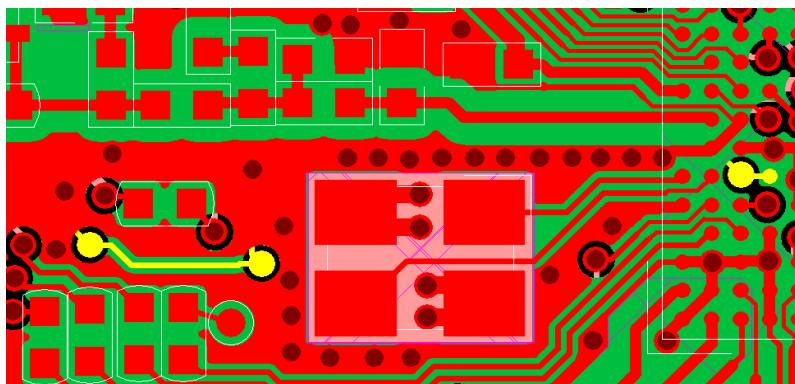
L2 GND separate and connect to 2503 GND

L2

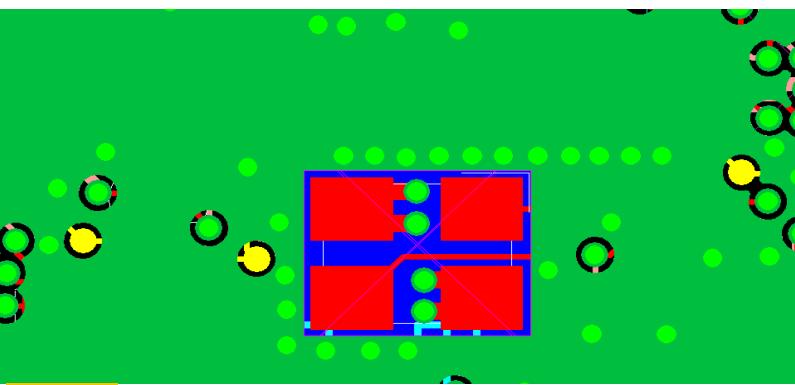
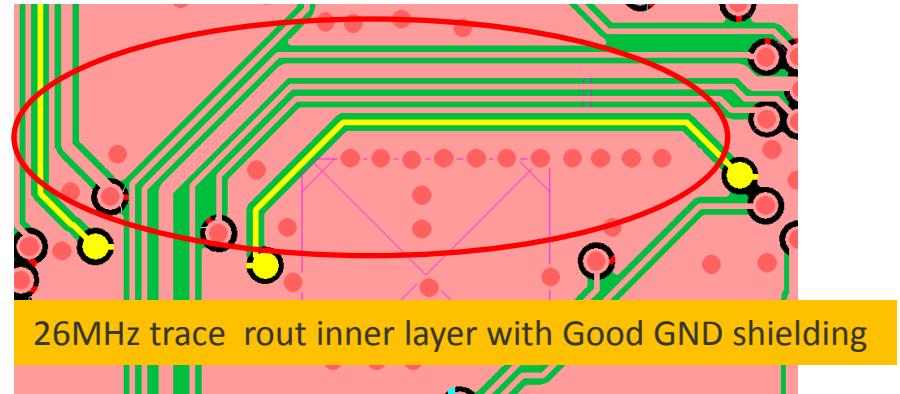


26MHz Buffer

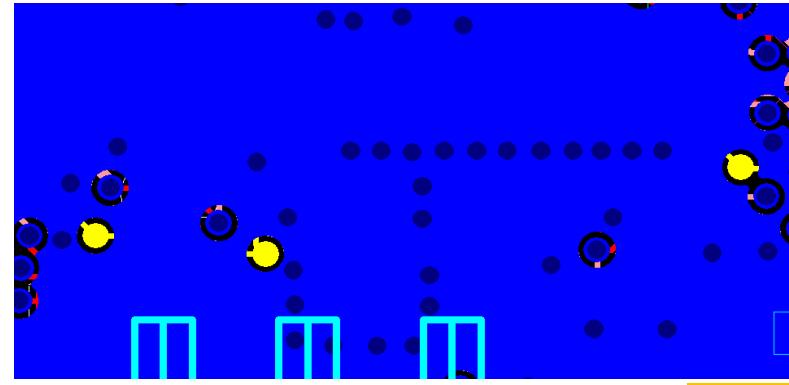
L1



L3



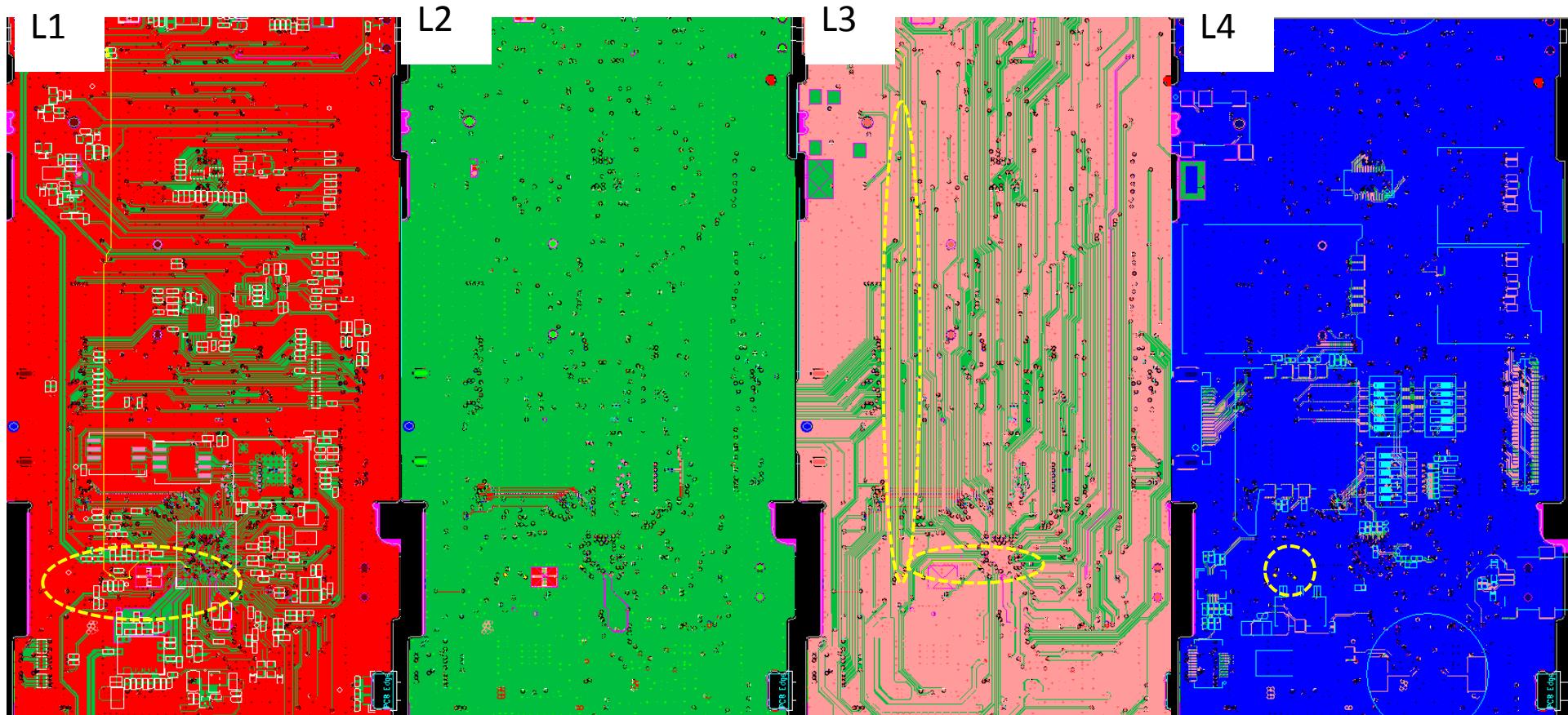
L2



L4

26MHz Buffer (cont)

- When use FREF (B6) for WiFi or ATV co-clk, the trace should be shielded in inner layer and kept away from power trace. Besides, the length should be < 5cm



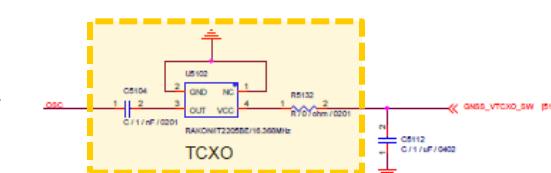
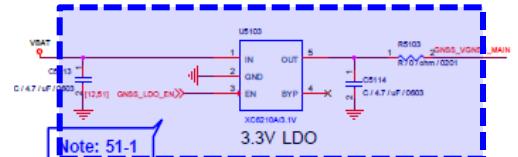
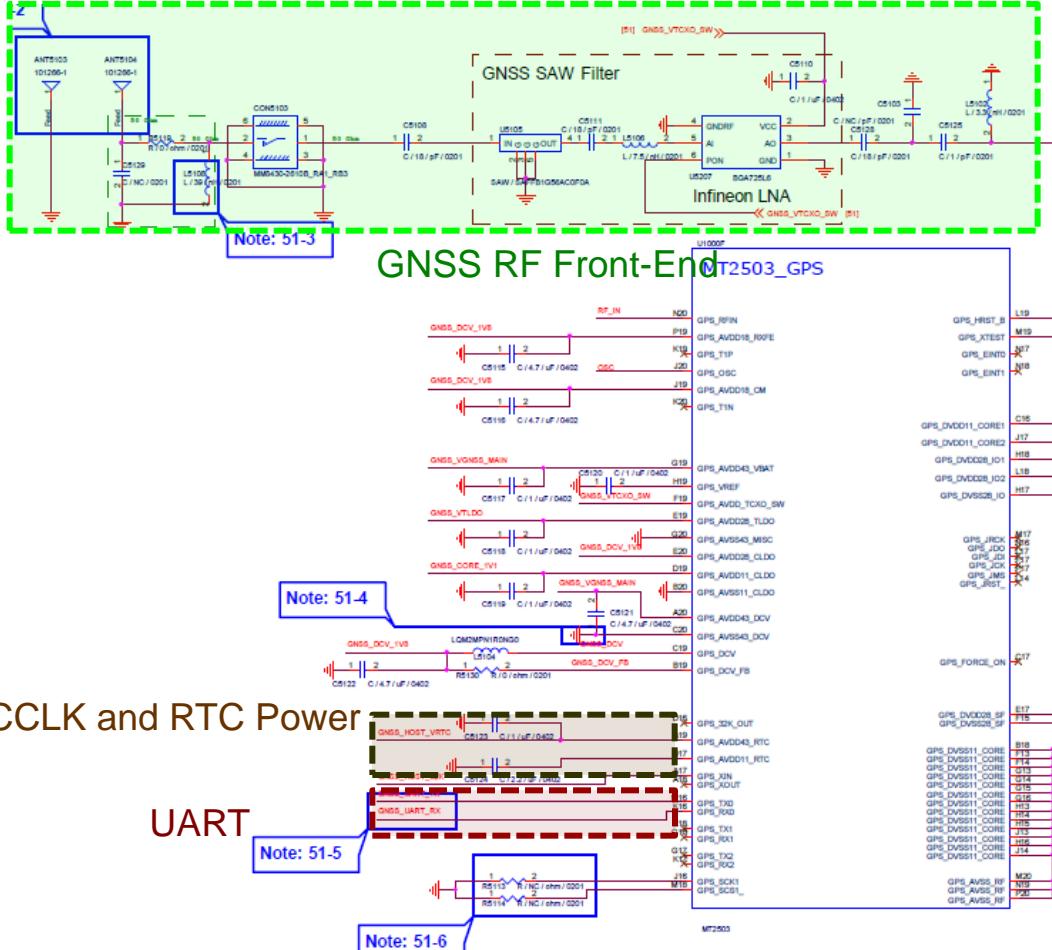


CONFIDENTIAL B

Design Notice - GPS



MT2503 GPS Reference Schematics



RTCCLK and RTC Power

UART

Note: 51-5

Note: 51-6

51_CONNECTIVITY_GPS

MT2503 GPS Schematic design notice

1. Do not change the host connection between MT3333 and MT6261. (refer to page 8)
2. GPS Reference Frequency Selection:
only pin-strap on J16 and M18 is needed. No software modification is needed.

MT2503 GPS Performance Summary

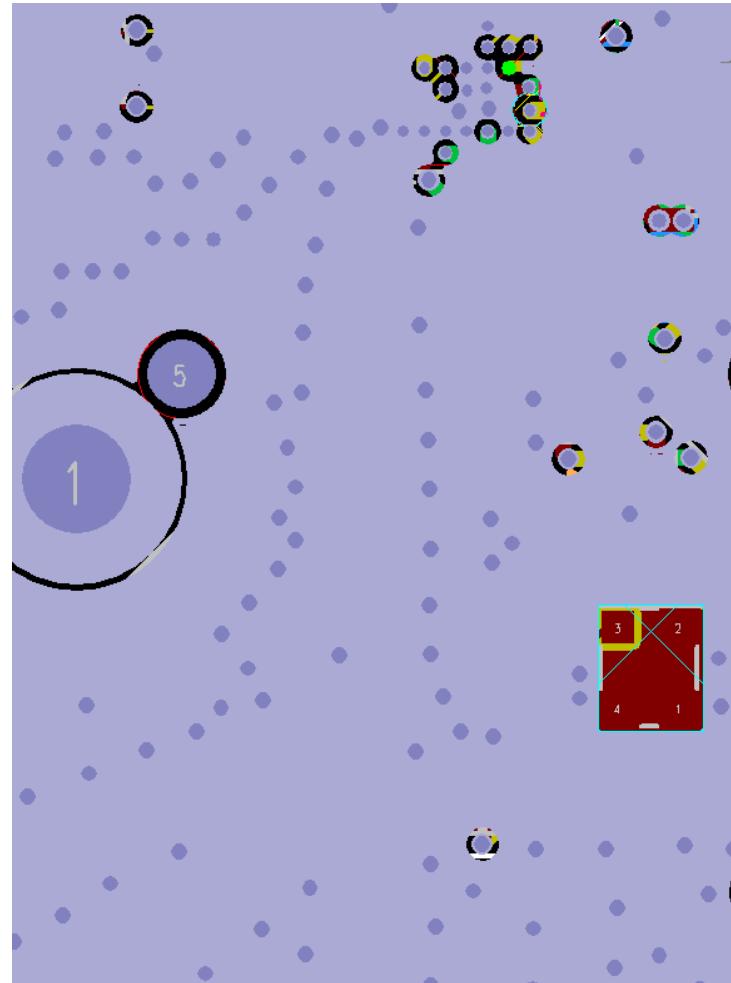
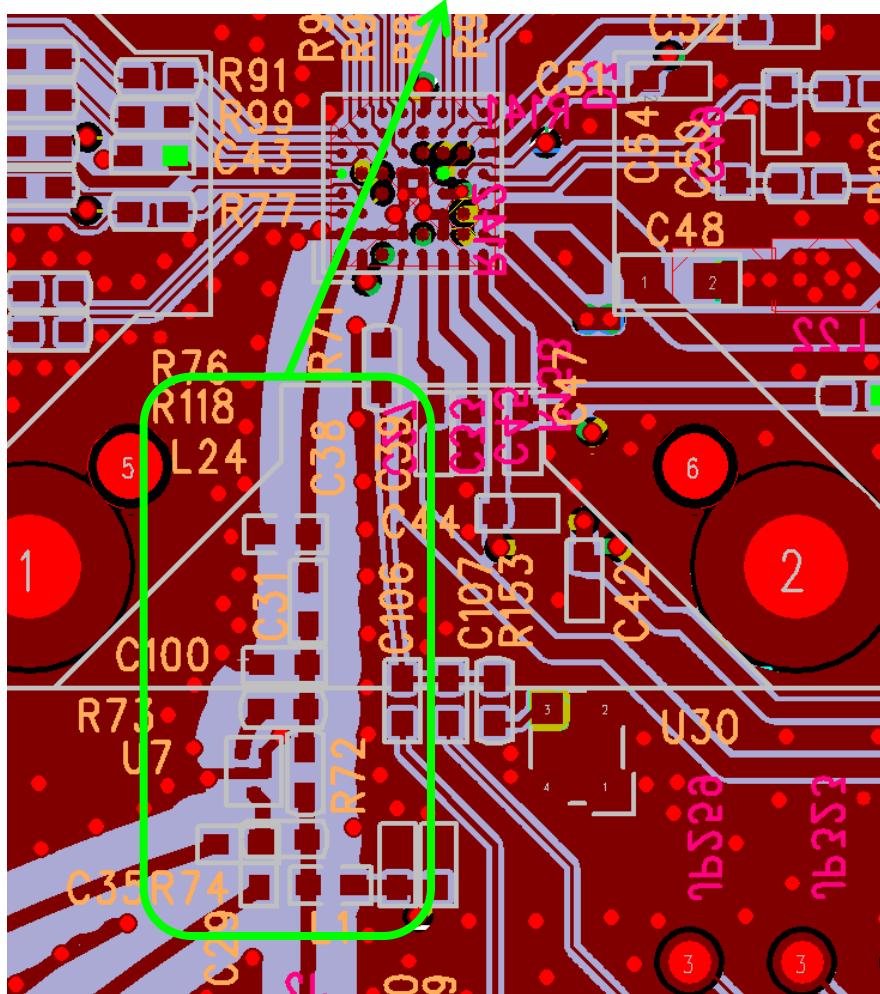
	GPS+GLONASS	GPS only
CTTFF	28s	31s
WTTFF	24s	31s
HTTFF	<1s	<1s
Tracking sensitivity	-165dBm	-165dBm
HTTFF sensitivity	-163dBm	-163dBm
WTTFF sensitivity	-151dBm	-151dBm
CTTFF sensitivity	-148dBm	-148dBm

- Lowest power consumption : 10mA tracking

MT2503 GPS PCB Layout Guide (1/5)

1

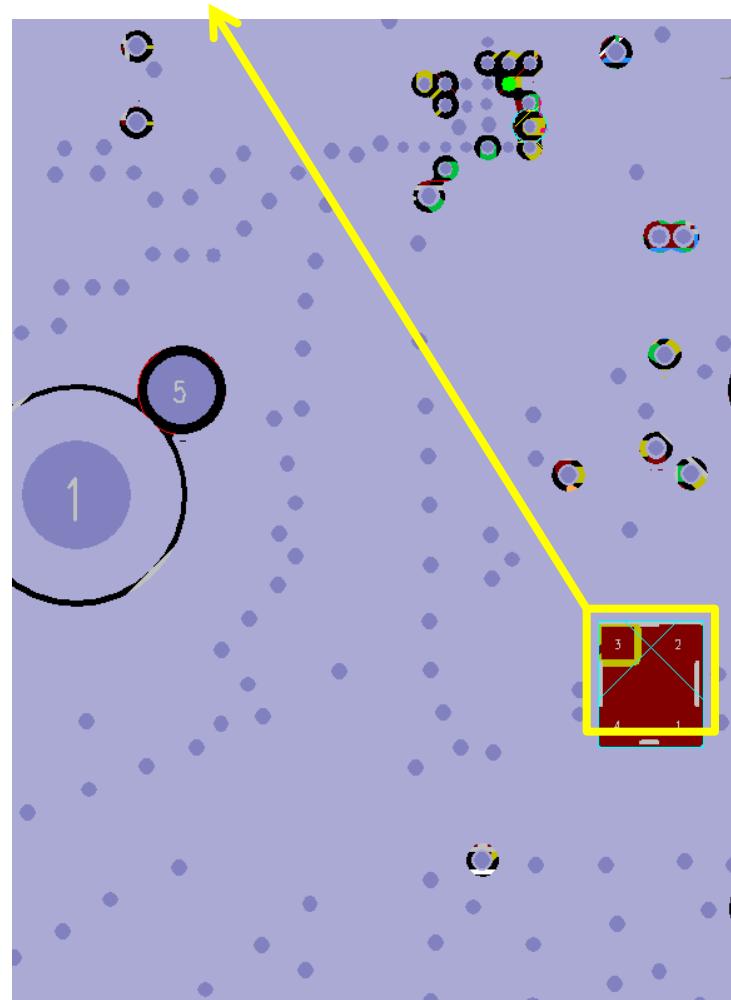
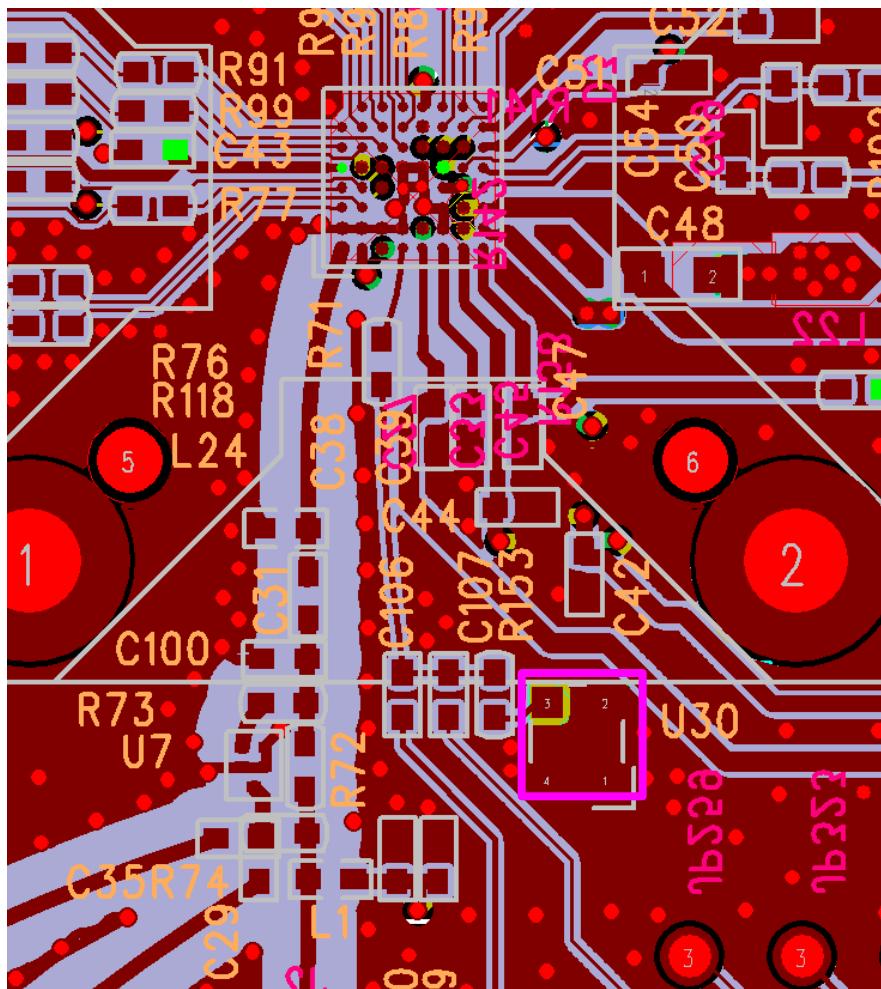
- Keep the RF path (from MT2503 to GPS antenna) as short as possible to reduce RF path loss.
- Rout RF trace to be 50Ω strip-line @ GPS band, shield it by GND plane nearby the trace and under the trace.
- Keep the GPS antenna as far from the interference source as possible.



MT3333 PCB Layout Guide (2/5)

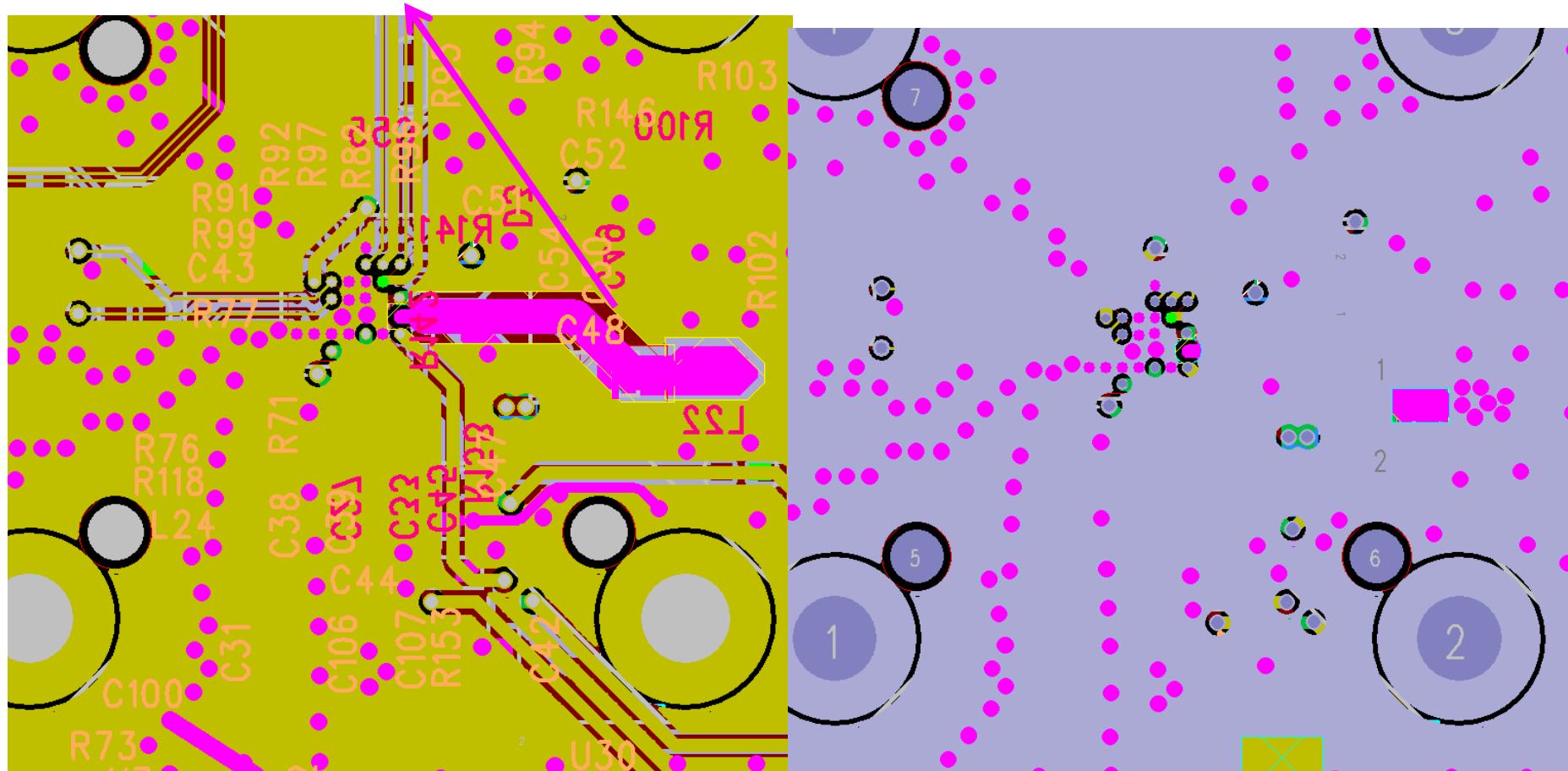
2

Space nearby (Layer-1) and under TCXO (Layer-2) should be empty to improve TCXO clock stability performance. (Improve the thermal isolation)



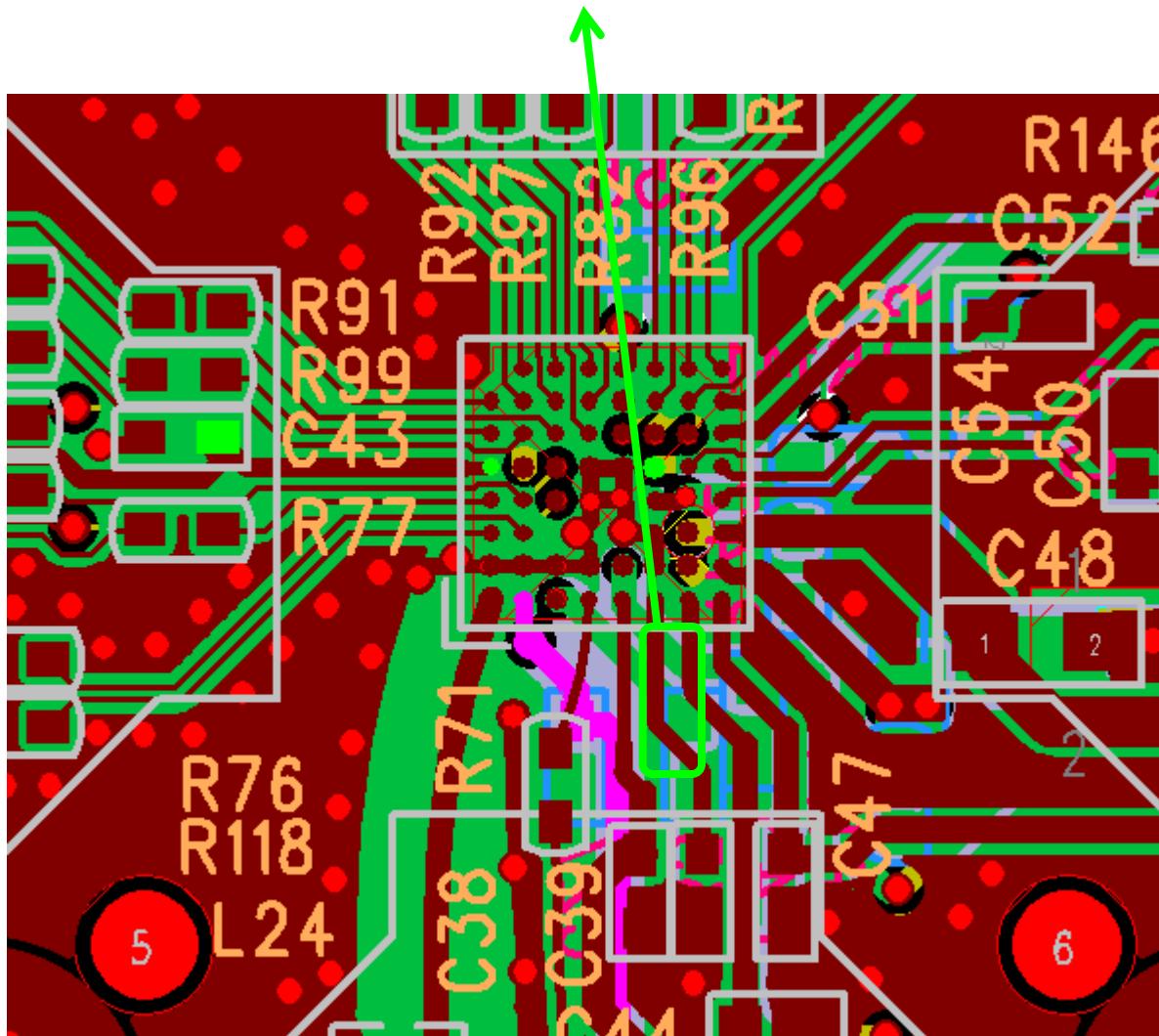
MT3333 PCB Layout Guide (3/5)

- ③ Pin14 (AVSS43_DCV) rout to GND of bypassed capacitor first, then connect to main GND.
(Improve the built-in BUCK performance)



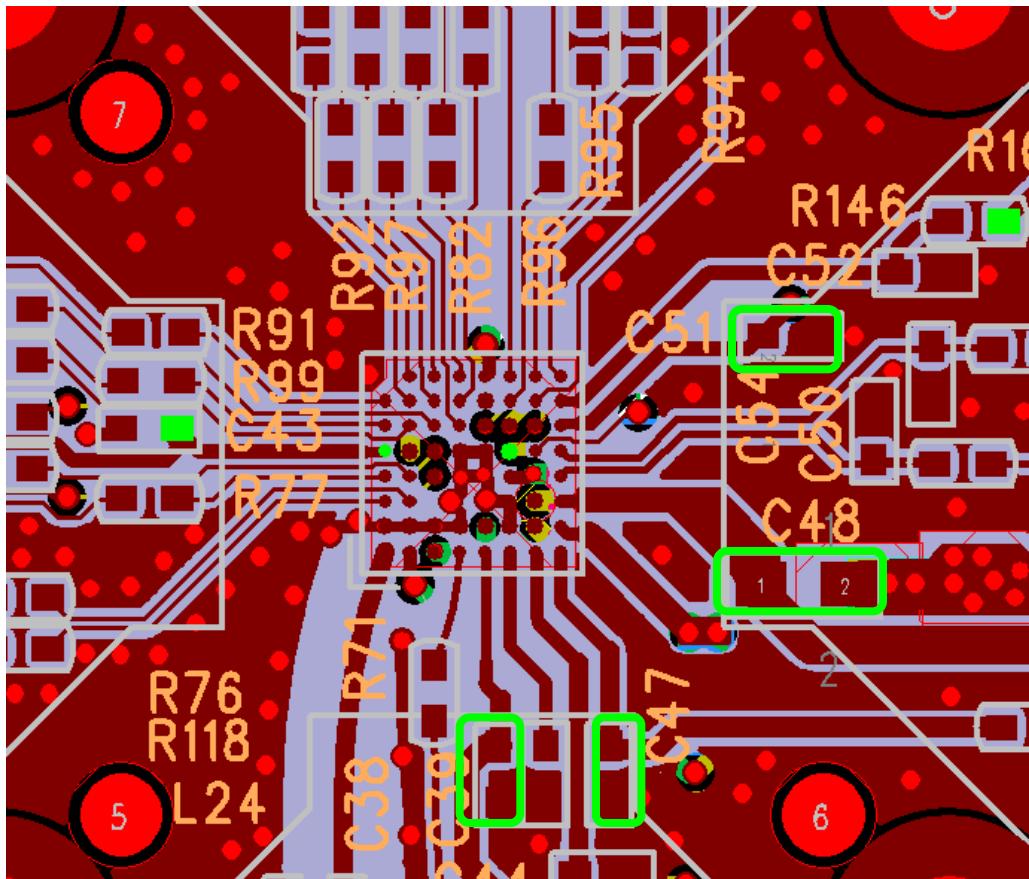
MT3333 PCB Layout Guide (4/5)

- ④ Put at least 1pcs 4.7nF capacitor near AVDD18_RXFE/AVDD18_CM pins.

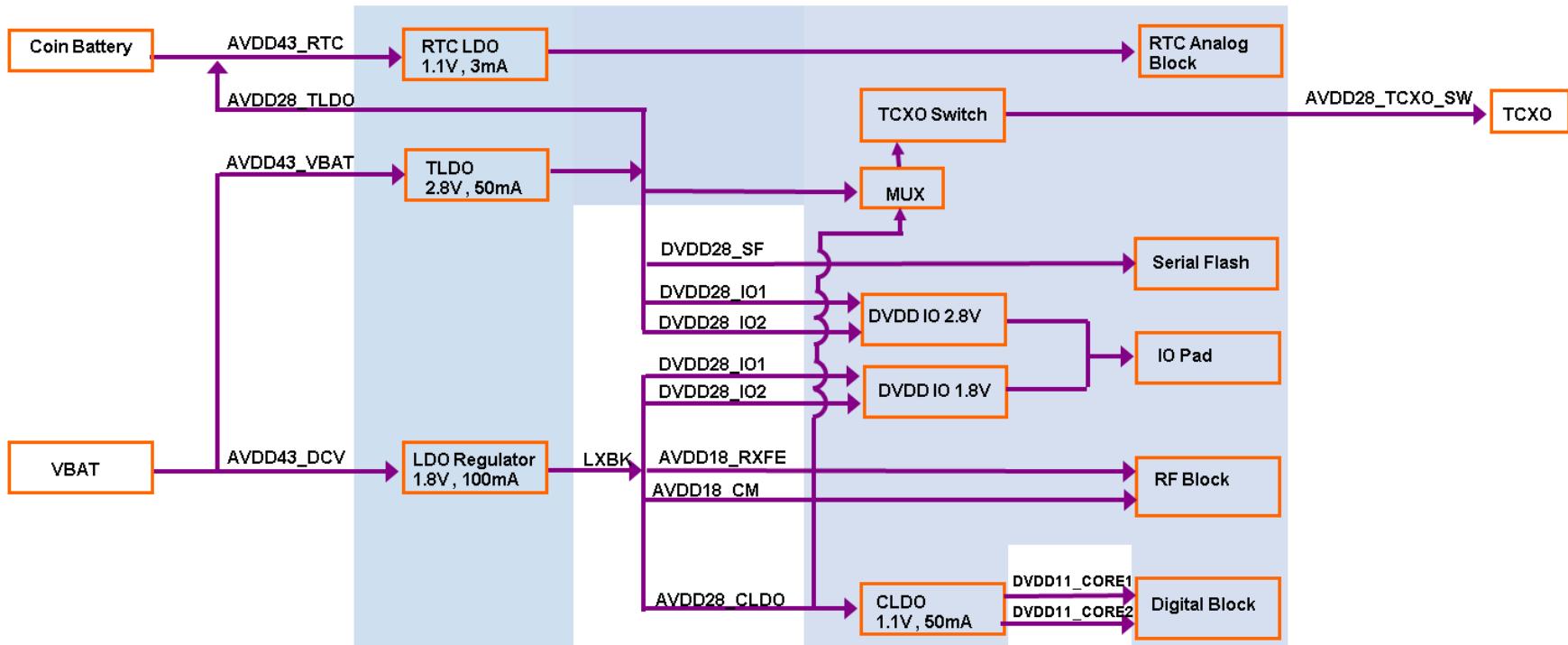


MT3333 PCB Layout Guide (5/5)

- 5 Put bypass capacitors near input / output pins of built-in LDOs.



Power Scheme – Buck mode



: Shadow area means inside MT3333 IC



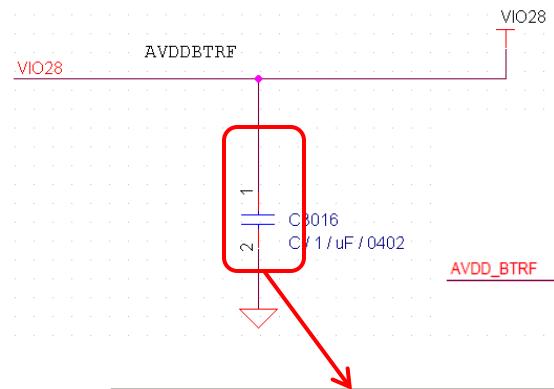
CONFIDENTIAL B

Design Notice - Bluetooth



MT2503 BT Reference Design Circuit

Power

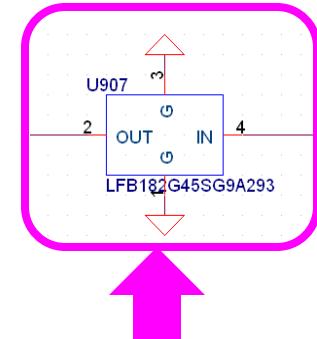


To get better rejection,
please use MTK QVL BPF

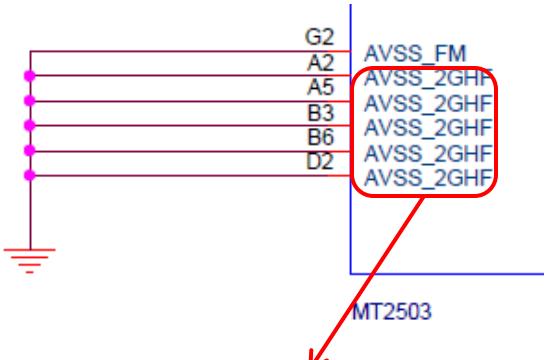
Must Read



[BT RF Trace]
Keep 50ohm impedance

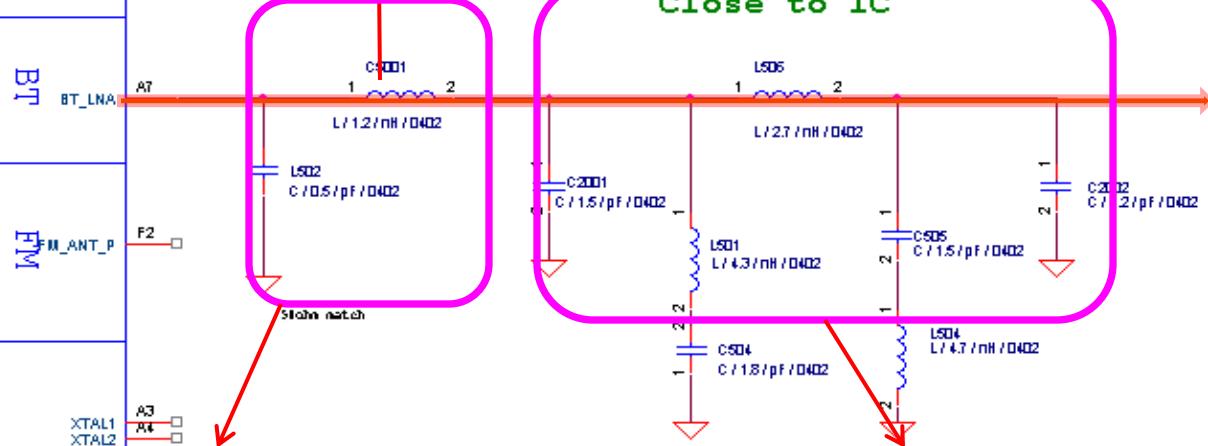


GND



[AVSS_2GHF]
- AVSS_2GHF should connect together
and then connect to main ground

RF



[BT 50ohm Matching]

- Must close to MT2503 IC
- The value of 50ohm Matching component need to be fine tuned on different layout.

Close to IC

[BT LC filter/bandpass filter]

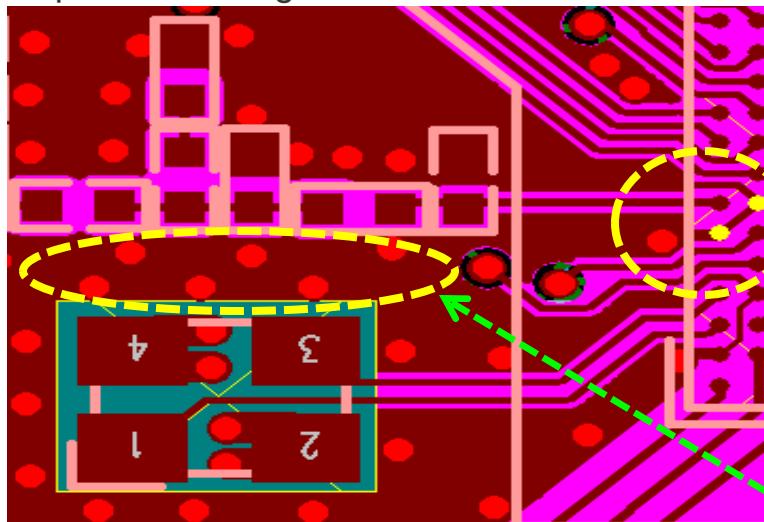
- Must close to MT2503 IC
- The value of LC filter component need to be fine tuned on different EVB layout.

MT2503 BT Layout Guideline (1/4)

Must Read

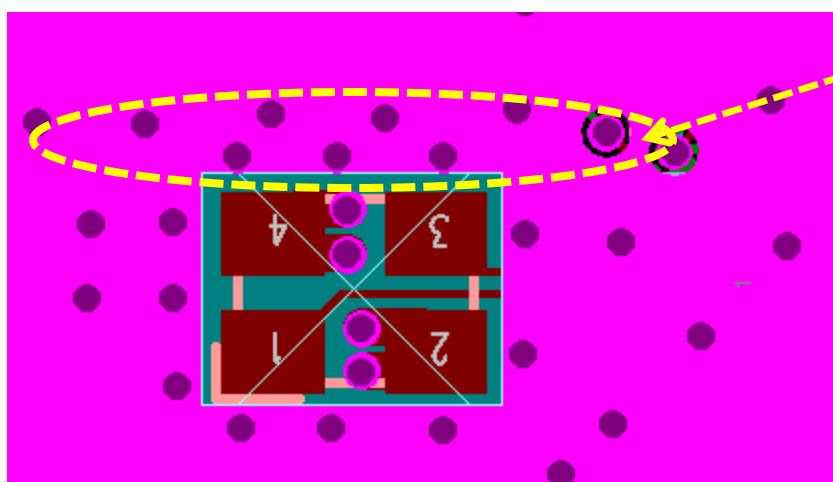
- BT GND pins should connect together first, then connect to the main ground plane through enough GND via to prevent from ground noise. It should **NOT** be merged with other ground traces, pads, or planes.

Layer 1



Don't connect with other GND on L1.

Layer 2



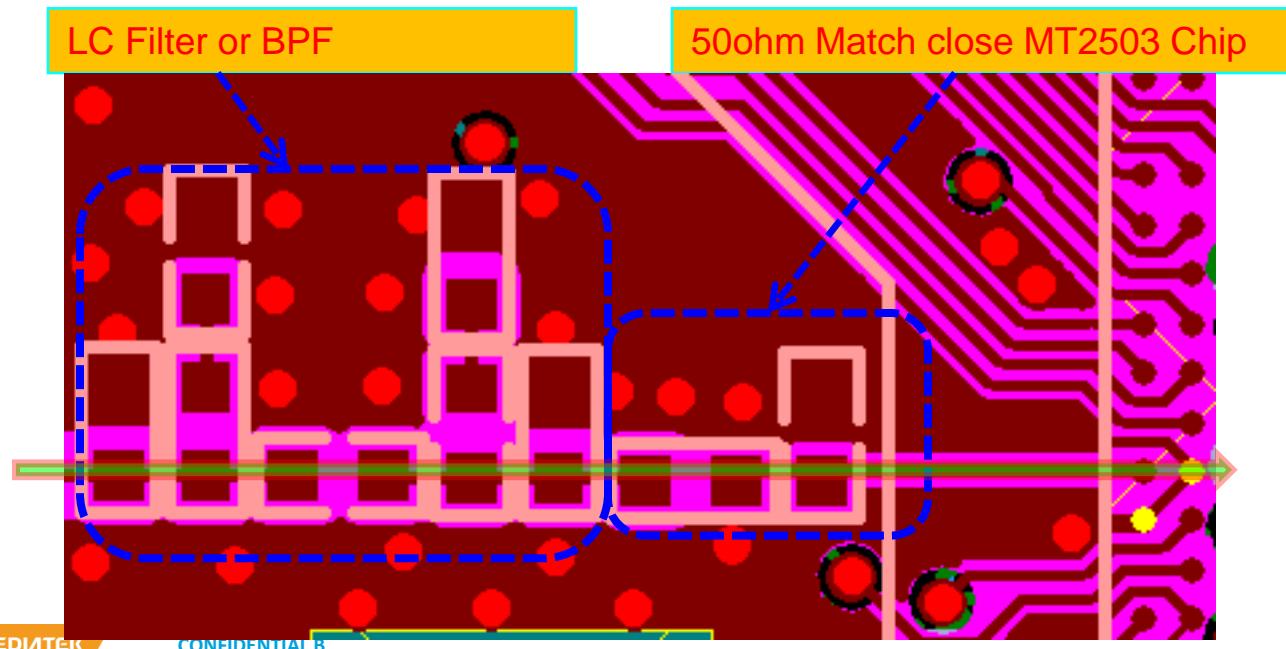
Ground and GND via between BT RF trace and 26M Crystal

MT2503 BT Layout Guideline (2/4)

Must Read

➤ RF/Analog Part :

- A. The line width and ground layer reference for RF traces should be kept for better impedance control, which **is close to 50ohm line**.
- B. Because of MT2503 BT RF pin without integrate 50ohm Match, so **external 50ohm Matching is must need**, which must close to chip as possible for better impedance control
- C. The BPF or LC Filter should be placed **as close to chip as possible** for better RF performance.
- D. Using **qualified** the BPF which is single-in and single-output.
- E. The **GND plane** under RF trace should **keep integrate**, and without crystal /26MHz clock /digital trace overlap.

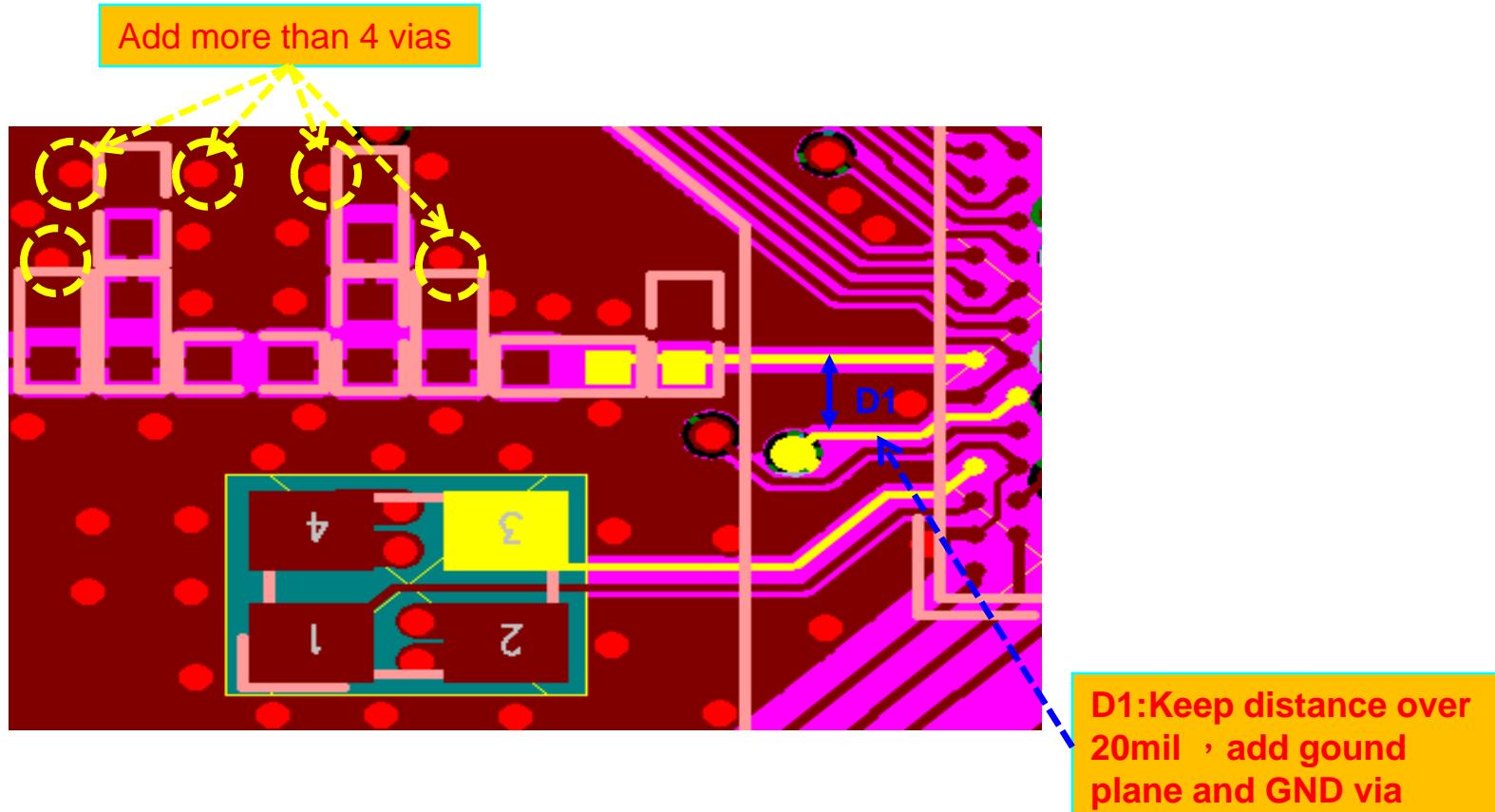


MT2503 BT Layout Guideline (3/4)

Must Read

➤ Matching and LC filter Part :

- A. To avoid **26MHz de-sense**, need to keep **distance D1 as long as possible** between Pin A6(BT RF) and Pin C5(26M clk) trace, add GND plane & via between the two trace.
- B. The **GND plane** under Power trace should **keep integrate** , and without crystal /26MHz clock /digital trace overlap.



MT2503 BT Layout Guideline (4/4)

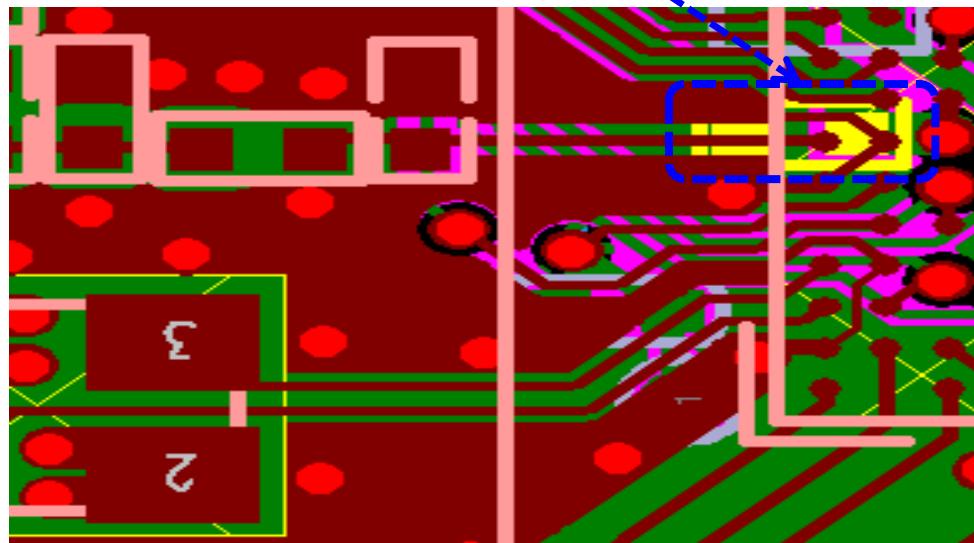
Must Read

➤ Power trace:

BT power by PMU VIO28 :

put a 1uF cap close to the AVDD_BTRF ball

decoupling cap should be put
close to the MT2503

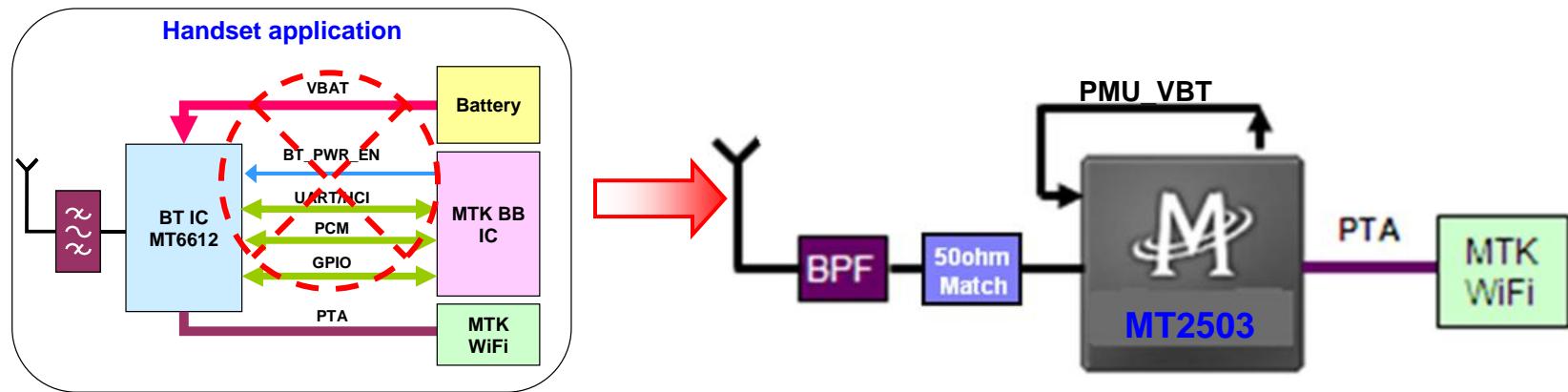


MT2503 BT Interface Design

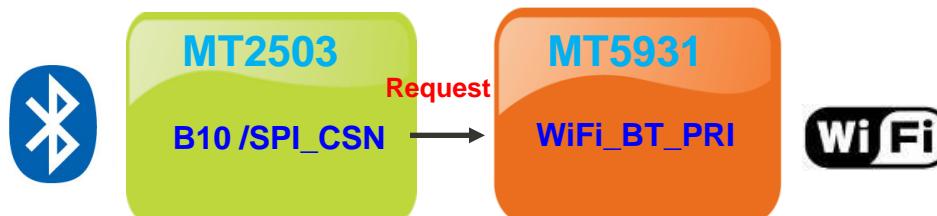
MT6612/MT6622

MT2503

- Since the MT2503 features a highly integrated Bluetooth transceiver, **no need external interface to connect with Host**.

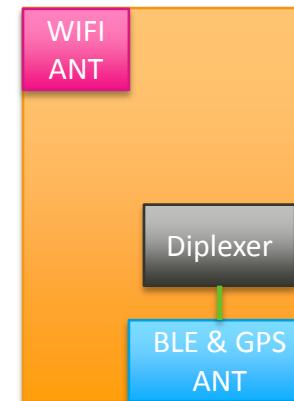


- MT2503 PTA interface.
 - MT2503 MTK WiFi solution: support **Proprietary One-wire** protocol with proper configurations.



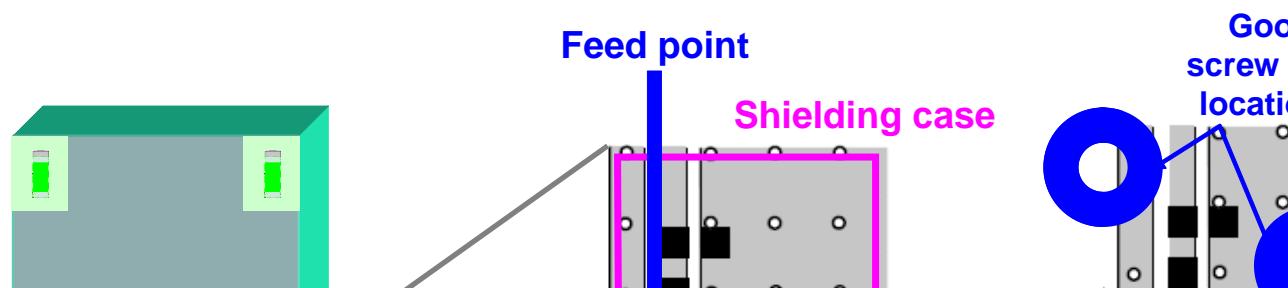
MT2503 BLE Solution Notice

- If a 3rd party BLE solution is used, do not share WIFI antenna with BLE. Because BLE chips without Packet Traffic Arbiter (PTA) pin can not make a handshake with WIFI chip for Time-sharing.
- It is recommended that BLE should have a separate antenna which should be kept away from WIFI antenna as far as possible, or BLE and GPS share an antenna with a diplexer.



BT Antenna Placement Guideline

- Place the BT antenna at the corner of the PCB.
- The feed point is directly connected to the antenna.
- Reserve enough distance between the antenna, ground and the shielding case.



MT2503 BT LC Filter Design Note & Spec. (1/3)

Must Read

➤ LC filter Spec.

- Every design of LC filter need to meet the spec.

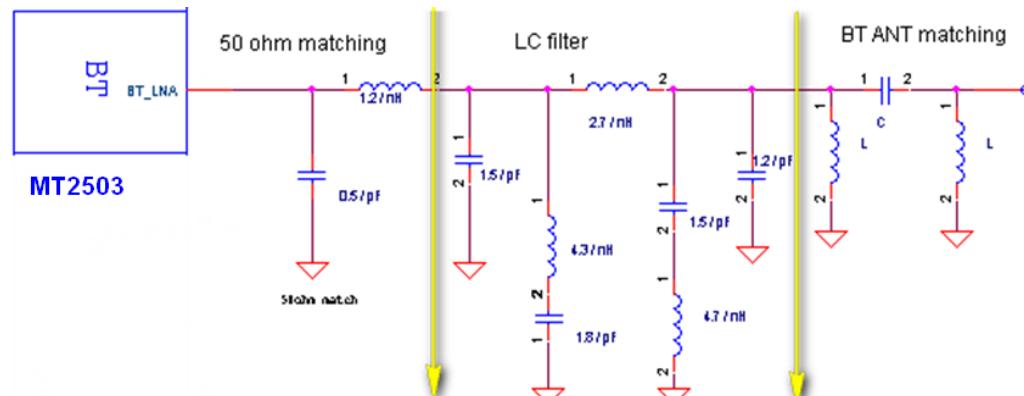
Frequency Band	Attenuation Spec.	PS.
1201~1240 MHz	8 dB	0.5xLO leakage
1710~1990 MHz	>15 dB	BT De-sense by DCS/PCS
2400~2500 MHz	<2 dB	In-band insertion loss as low as possible
3600~3720 MHz	15 dB	1.5x LO leakage
4800~4980 MHz	20 dB	2 nd harmonic of BT TX

➤ LC filter reference design & insertion loss

➤ Base on reference design, every design of LC filter need to be fine-tuned for different EVB layout (**Due to the board of the parasitic effect, can affect the characteristics of LC Filter, need to fine tune the Filter component values**)

➤ The variation of LC component: Capacitor< $\pm 0.1\text{pF}$; Inductor< $\pm 0.1\text{nH}$

➤ **In general, in-band loss of LC filter is about 1~2dB. If insertion loss is unacceptable, please use BPF(1.4 dB-loss)**



MT2503 BT LC Filter Design Note & Spec. (2/3)

Must Read

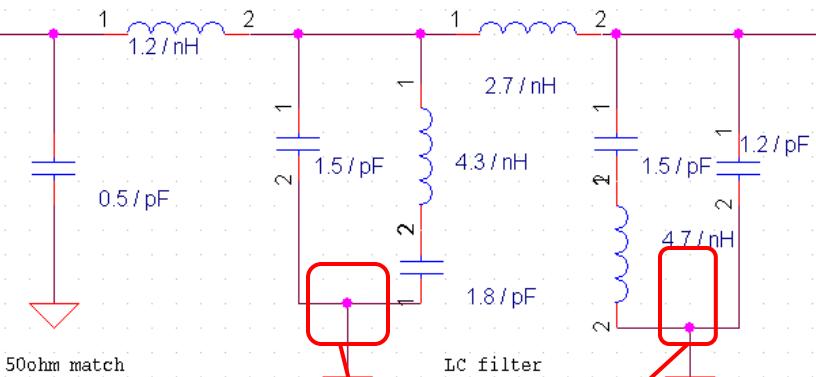
➤ Layout notice of LC filter:

➤ Grounding:

➤ LC filter ground pins should connect to main ground separately as soon as possible (by GND via)

(**The ground pin of LC filter component should be connect to GND separately, and add more GND VIA, then the GND VIA should be close to component ground pin.**)

➤ In order to reduce Mutual inductance effect, the placement of LC filter inductor should be vertical instead of parallel

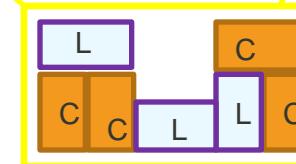
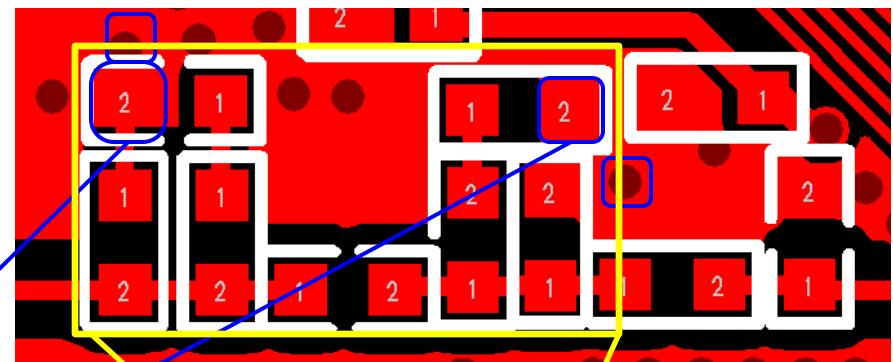


[Ground pad of LC filter]

- AVSS_BT should connect to main ground as soon as possible (by GND via)

(The ground pin of LC filter component should be connect to GND separately, and add more GND VIA, then the GND VIA should be close to component ground pin)

Connect to ground separately by different GND VIA

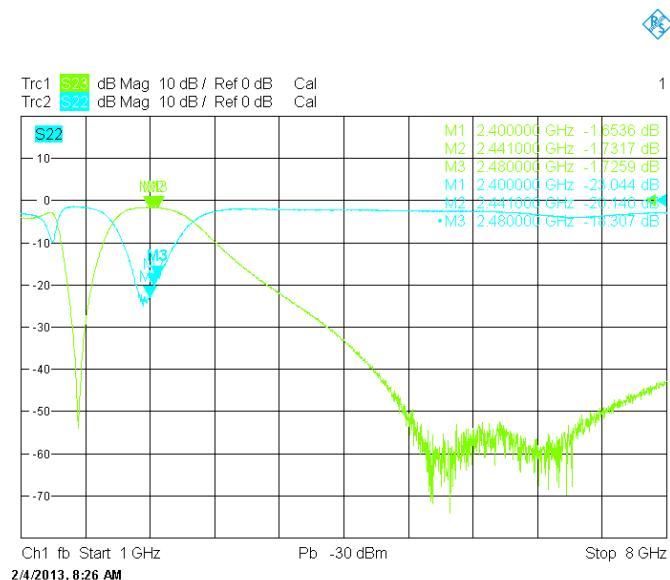
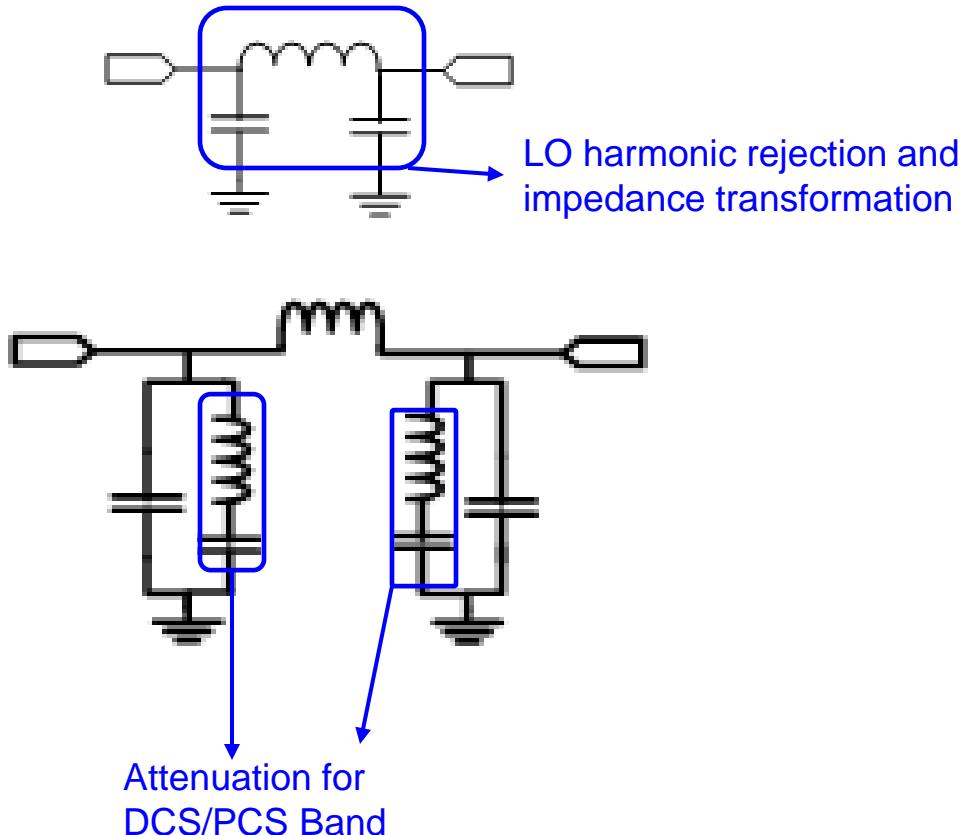


MT2503 BT LC Filter Design Note & Spec. (3/3)

Must Read

➤ LC filter tuning guideline

1. 2 LC notch filter for DCS/PCS band rejection
2. CLC Low-pass filter for LO harmonic rejection and impedance transformation





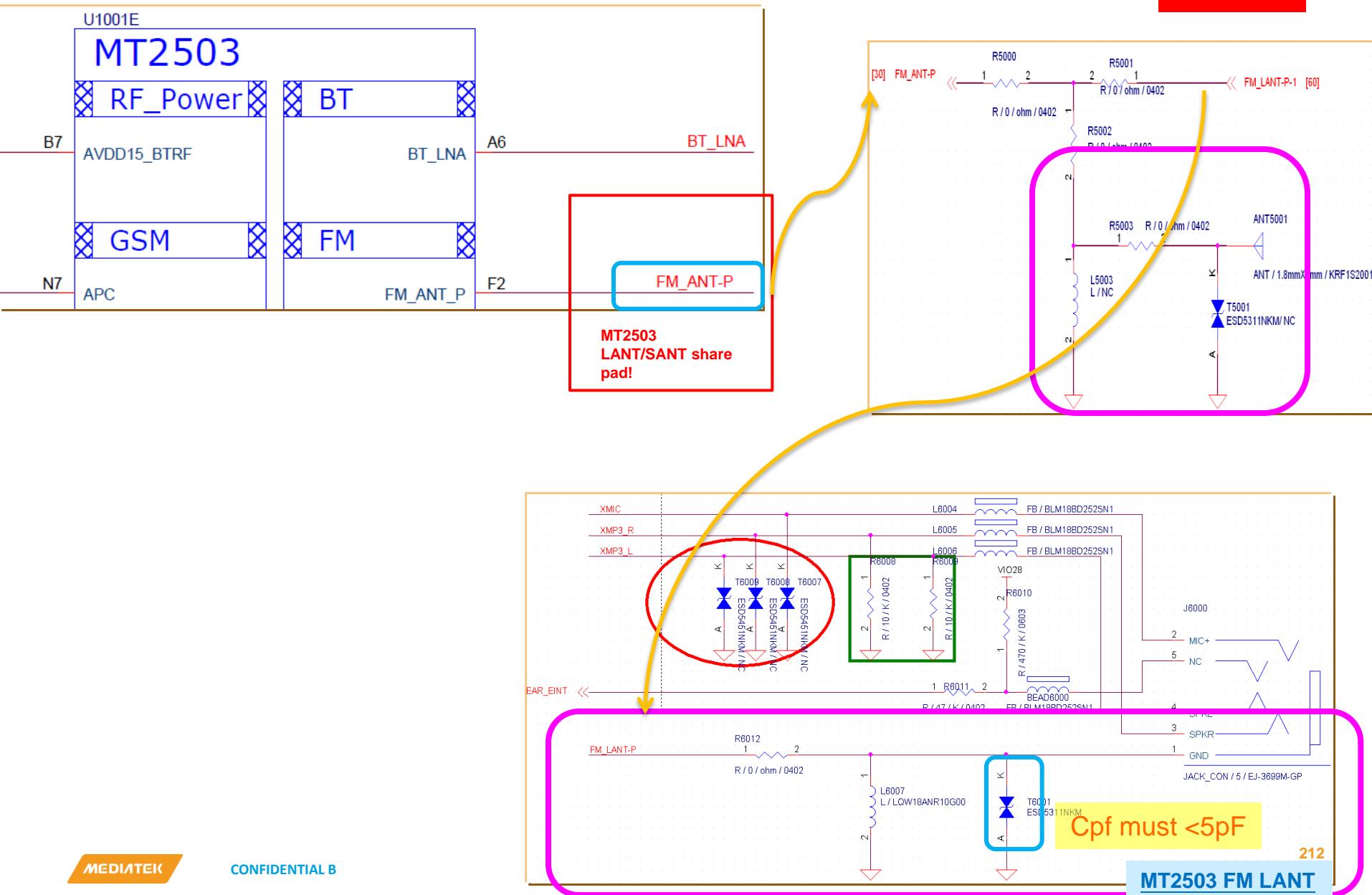
CONFIDENTIAL B

Design Notice - FM_Receiver



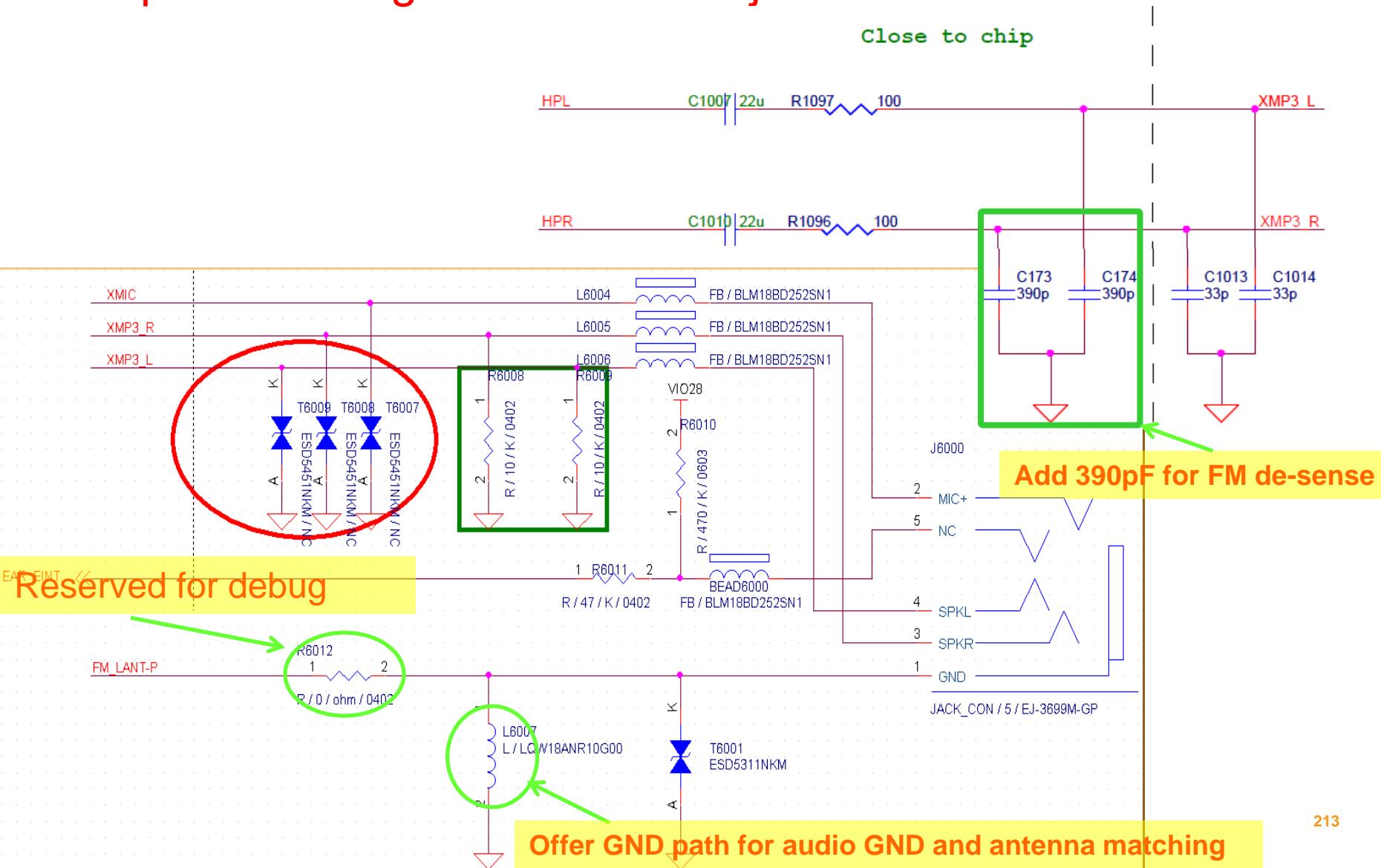
MT2503 FM ANT Circuit

Must read



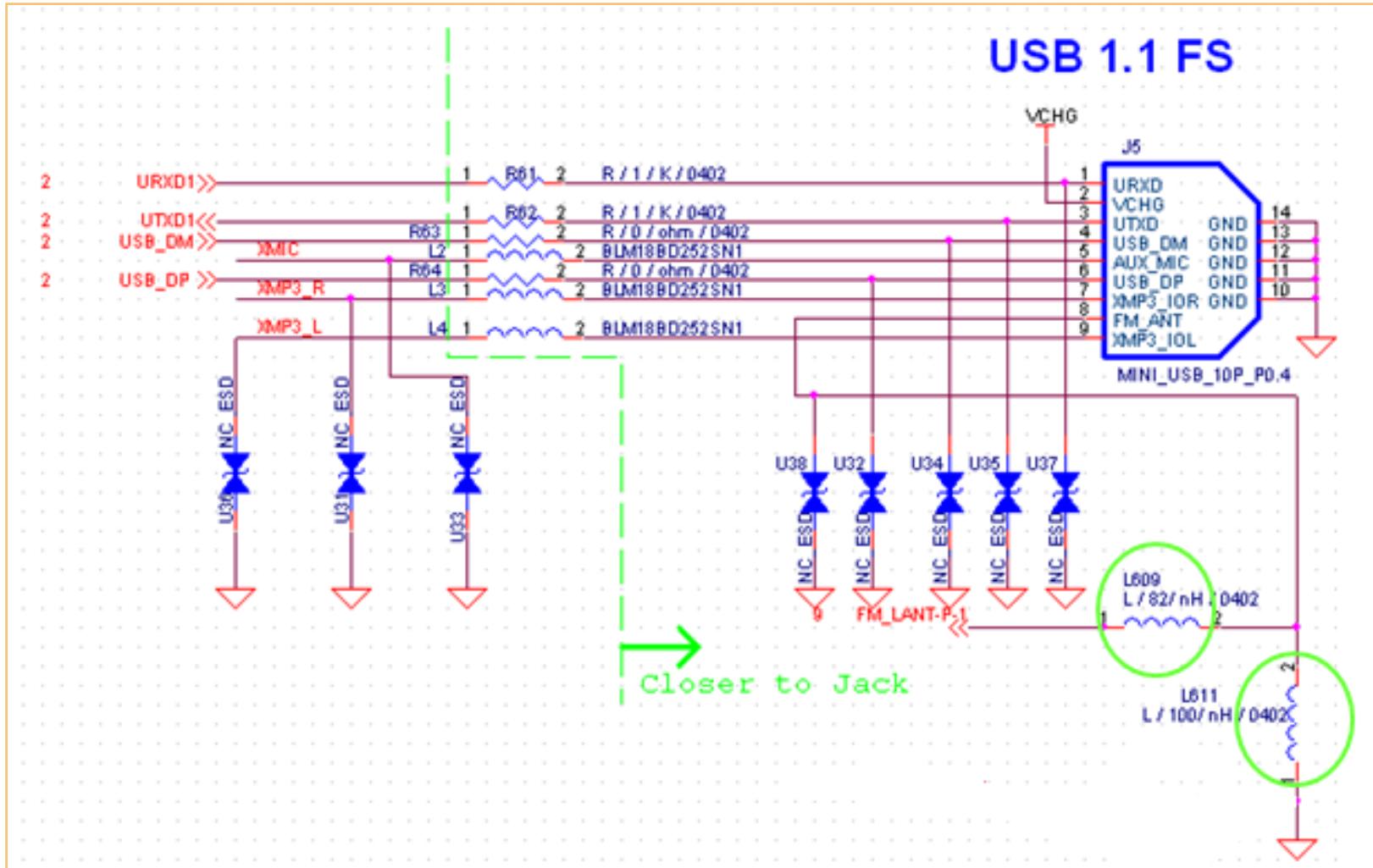
MT2503 FM Application Circuit (1/3)

- Option1: Using 3.5" EarPhone jack



MT2503 FM Application Circuit (2/3)

- Option2: Using USB as EarPhone jack



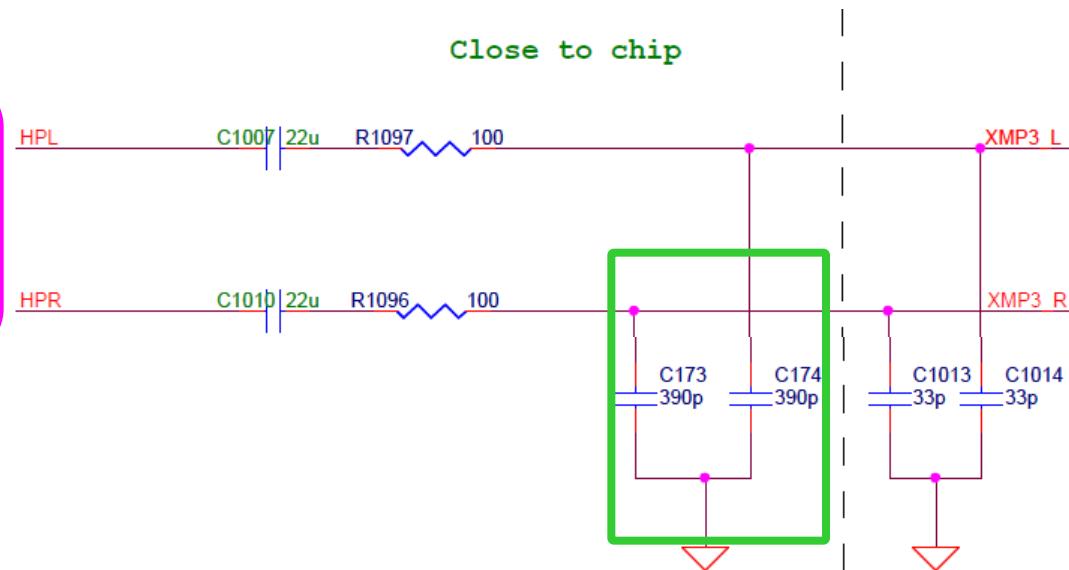
MT2503 FM Application Circuit (3/3)

Must read

- XMP3_L/R close to chip should add 390pF for de-sense.

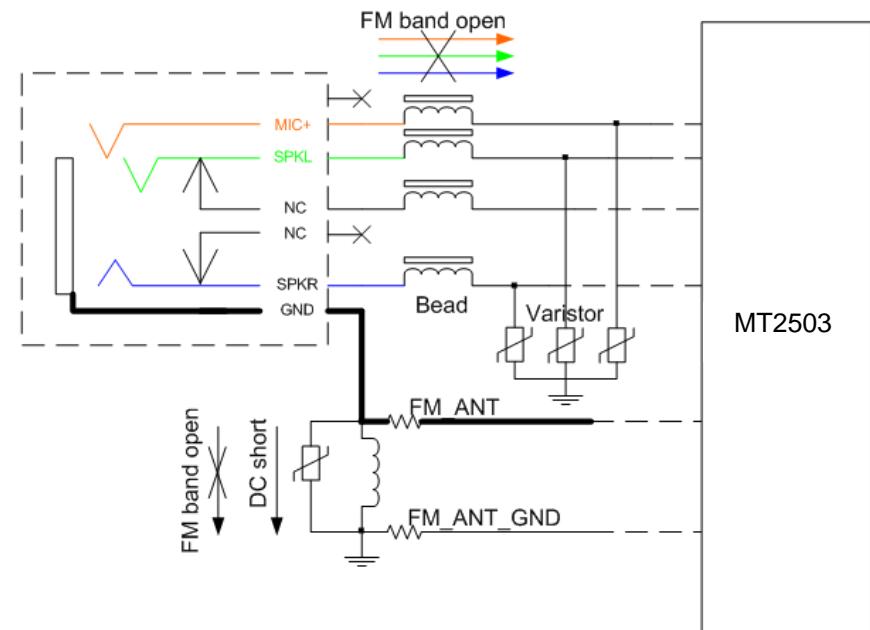
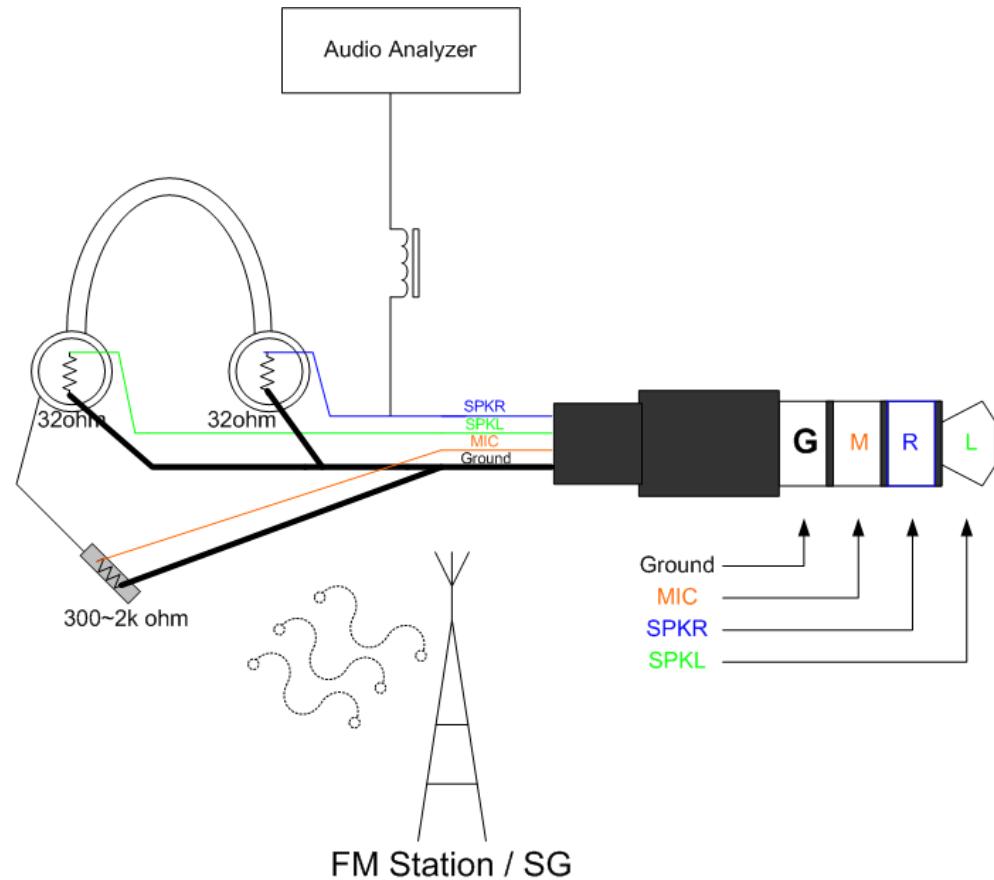
Note:

Total C load of Audio output
must < 500pF.



Earphone and FM Antenna Interface

- Using audio jack ground as FM antenna.



MT2503 FM ESD Design Guide

FM ESD Design Guide

FM trace

- FM Power/ANT Trace should be shielded in inner layer , and keep away from the board edge .
- FM Power/ANT Trace should be shielded by GND, and don't parallel with I/O 、 clk 、 power.... traces ,such as USB trace/keypad/Vbat etc.

ESD Component

- Reserve ESD component(TVS) on ANT trace with $C_{pf} < 5\text{pF}$.
- Place ESD component close to Interface, such as earphone Jack 、 SANT pad etc.
- Should let static electricity pass ESD component directly before entering IC.
- ESD component 's GND pin should be connected directly to global ground with enough via.

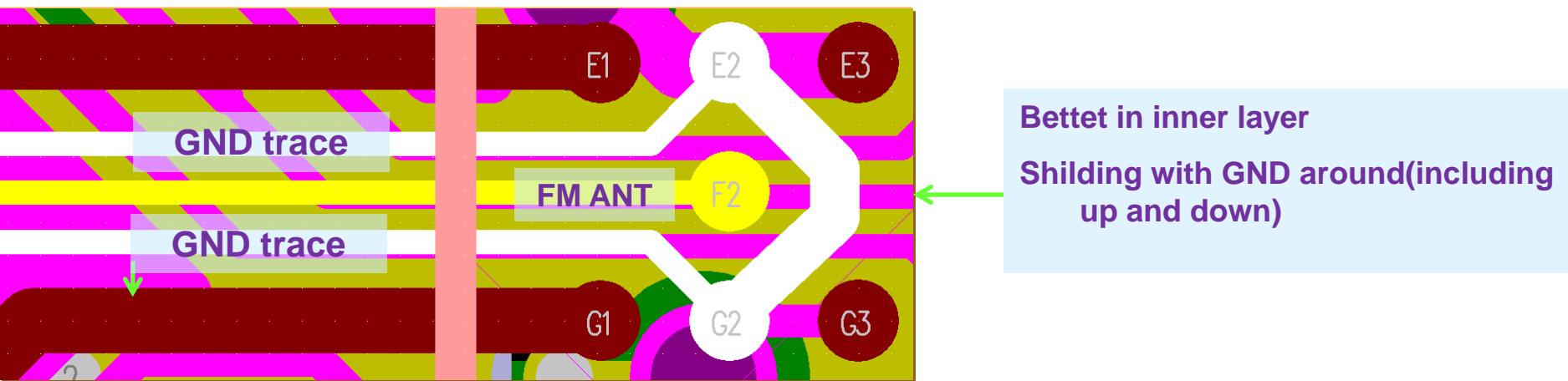
Factory Test

- Recommend to discharge of the earphone in time after plugging in/out for one cycle ,avoid headset charge accumulation too much, lead to damage phone.
- Please make ESD protection when factory use test fixture.

MT2503 FM Layout Design Guide

MT2503 FM Layout Guide (1/8)

- FM ANT RF trace should well grounding use GND E2/G2 , better in inner layer when using Multilayer boards.



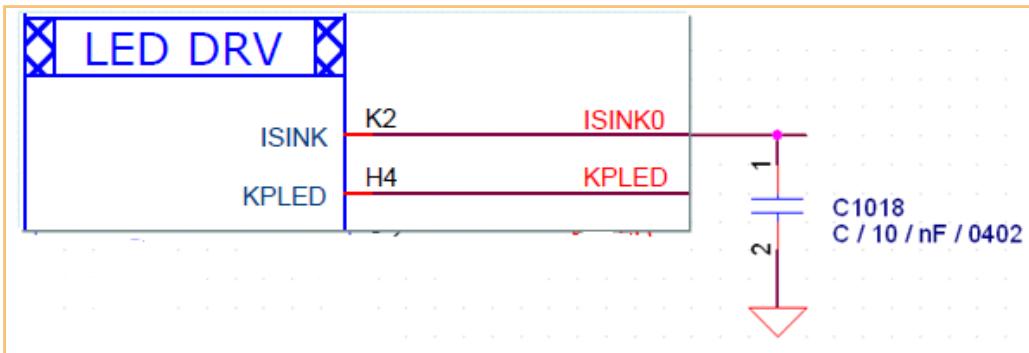
MT2503 FM Layout Guide (2/8)

Must read

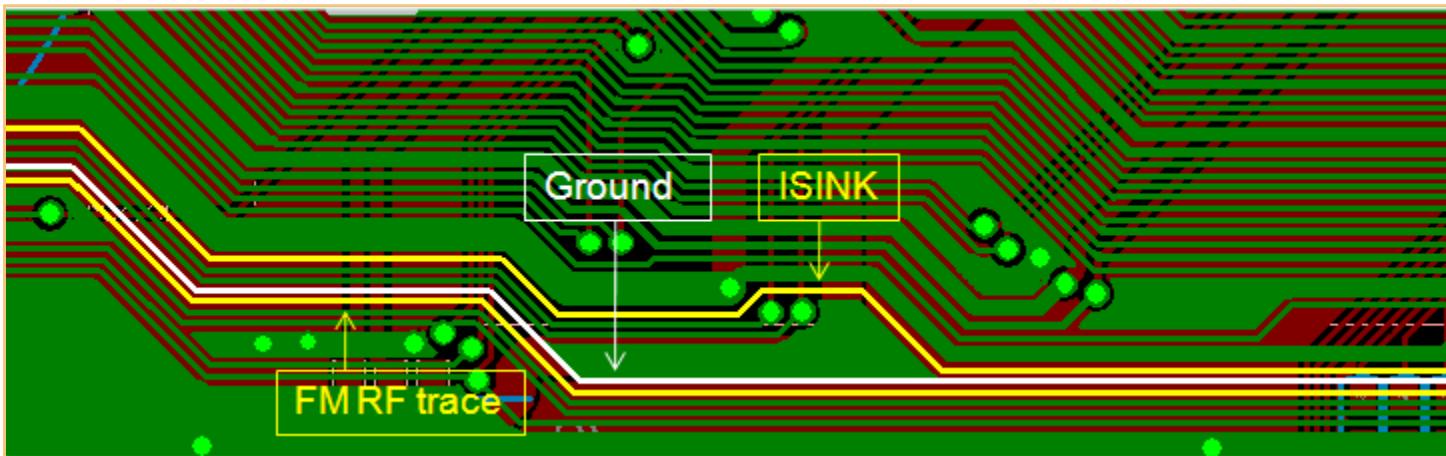
- shutdown 10nF cap at ISINK trace, except that:

1.ISINK trace and FM trace are far away

2.ISINK trace and FM trace are not parallel



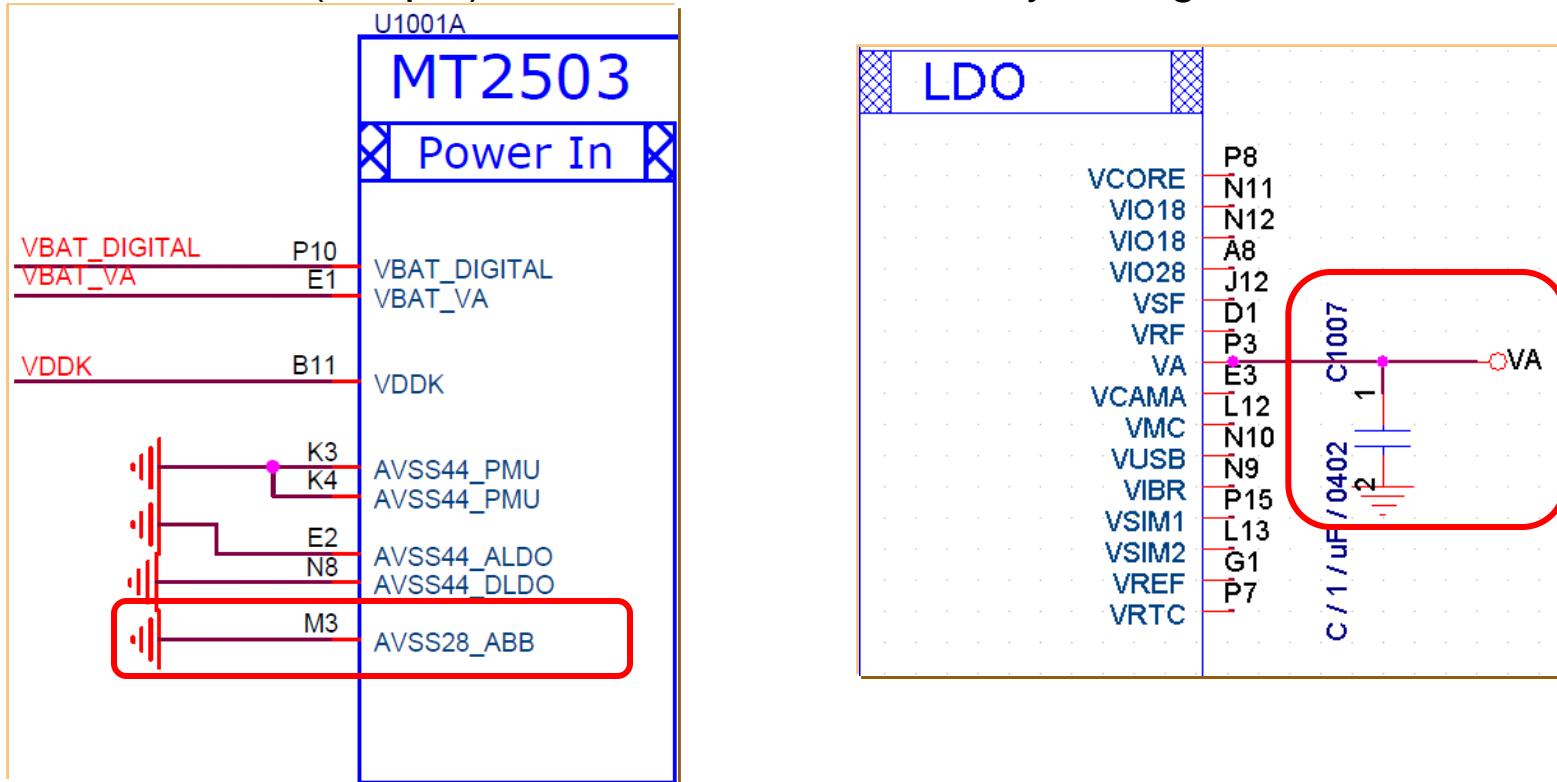
Below is a bad design:



MT2503 FM Layout Guide (3/8)

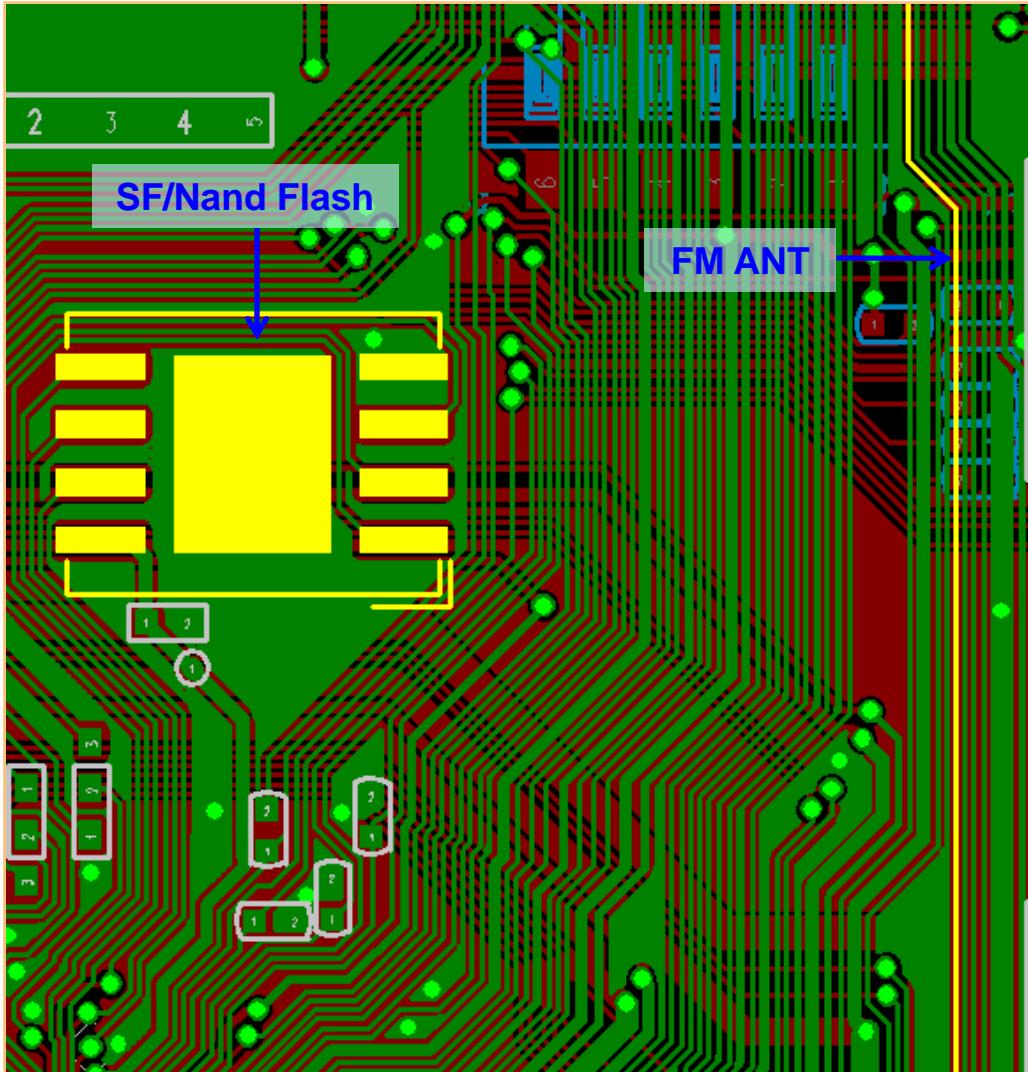
Must read

- Keep C1007 as close as possible to VA (P3 pin), It's better that C1007 connect to AVSS28_ABB (M3 pin) first then to Main GND by enough vias.



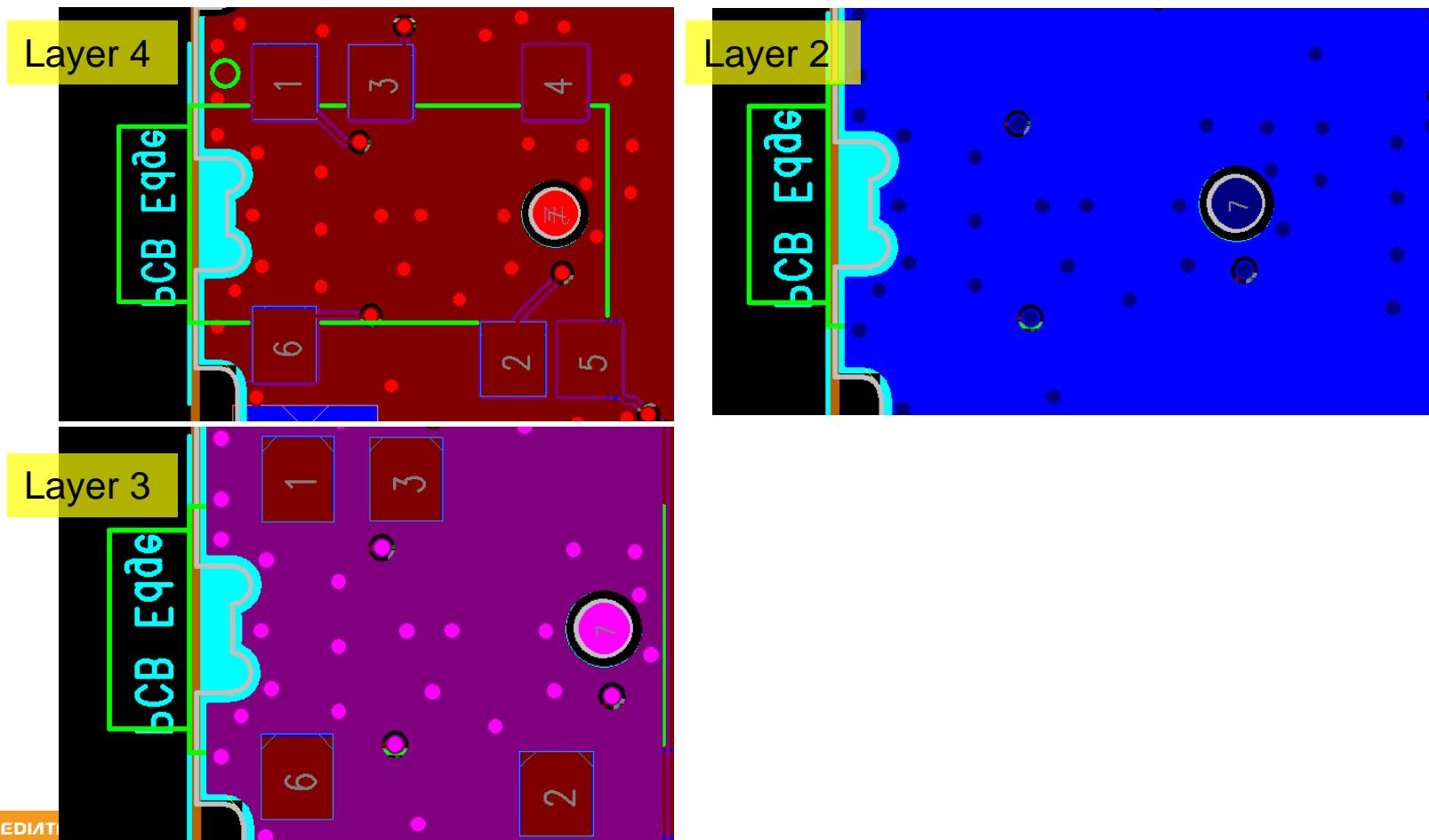
MT2503 FM Layout Guide (4/8)

- Make sure FM ANT trace far away from SF/Nand Flash trace.



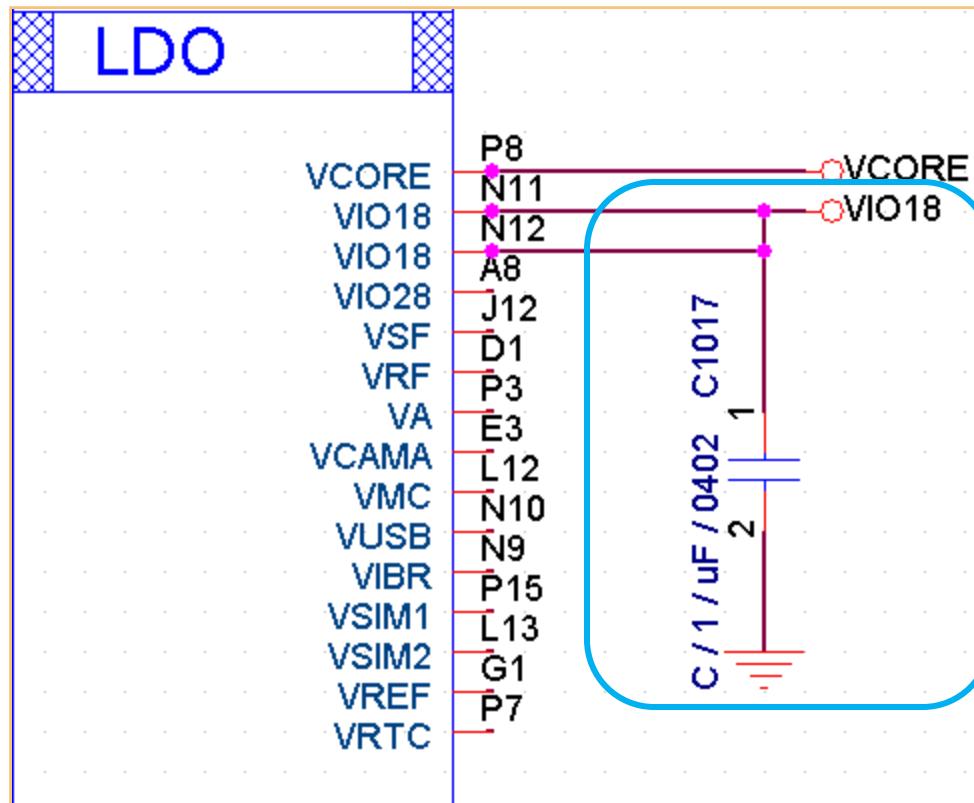
MT2503 FM Layout Guide (5/8)

- Treat Audio Jack pad as Antenna feed pad.
- Keep out L3 Audio jack pad (the layer under audio jack).
- Make sure L2 has complete GND.



MT2503 FM De-Sense Design Guide (6/8)

- Keep bypass cap(C1017) close to chip(N11/12 pin).



MT2503 FM De-Sense Design Guide (7/8)

- Earphone jack plays a role as FM antenna port and is not located near any noisy source including LCM FPC, un-shielding memory/LCM/USB bus, un-shielding boost/charge pump/class D amplifier/buck/backlight driver circuit, un-shielding PWM signal, etc.
- FM long antenna (LANT) trace between earphone jack and chip must be enclosed well with GND shielding
 - If LANT routs in inner layer, not only left and right GND shielding but also up and down GND shielding are necessary
 - GND shielding has to accompany with enough GND via
- FM short antenna (SANT) trace between chip and short antenna must be enclosed well with GND shielding
 - If SANT routs in inner layer, not only left and right GND shielding but also up and down GND shielding are necessary
 - GND shielding has to accompany with enough GND via
 - Short antenna placement should be far away from noise source as possible
 - FM_SANT trace is not necessary to be 50ohm

MT2503 FM De-Sense Design Guide (8/8)

- In order to suppress LCM radiation, proper PCB exposed GND area(1/4 LCM metal area at least is recommended) reserving for LCM metal solid grounding is recommended
 - Keep LCM FPC as short as possible
 - Well GND shielding FPC is appreciated
- Noisy sources or traces must be put in shielding cover or shield well with PCB GND layer
 - Noisy source includes LCM FPC, memory/LCM/USB bus, boost/charge pump/class D amplifier/buck/backlight driver circuit, PWM signal, etc
- Reserve FM band serial bead for possible couple path
 - Serial bead([BLM18BD252SN1](#)) close to earphone jack for each audio trace (Audio-L, Audio-R, MIC) ; Well GND shielding for these traces, especially between bead and earphone jack
 - Serial bead for PMU internal boost input VBAT path. Bead is put close to radiation source
 - Reserve serial 0ohm for parallel host I/F control signal path such as LWRB (write strobe) , LPA0(address output) and LPCEO(chip select)

FM Short Antenna Design Guideline

FPC Type FM Short Antenna (1)

- The FM Short Antenna is made of FPC.
- The material of FPC is flexible, easy to bend, and can be designed as arbitrary shapes. It is easy to fit different ID/ME design.
- It is suggested to paste the FPC on the inside wall of the housing or a plastic antenna carrier.
- Reserve the suitable space of FPC in ID/ME design phase.
- It is suggested to locate the FPC near the FM chip for shortening RF trace.

FPC Type FM Short Antenna (2)

- Suggestion of ID/ME Design

- FPC is perpendicular to PCBA
 - Distance 1~2mm from PCBA.
 - Distance 3~4mm from Battery.



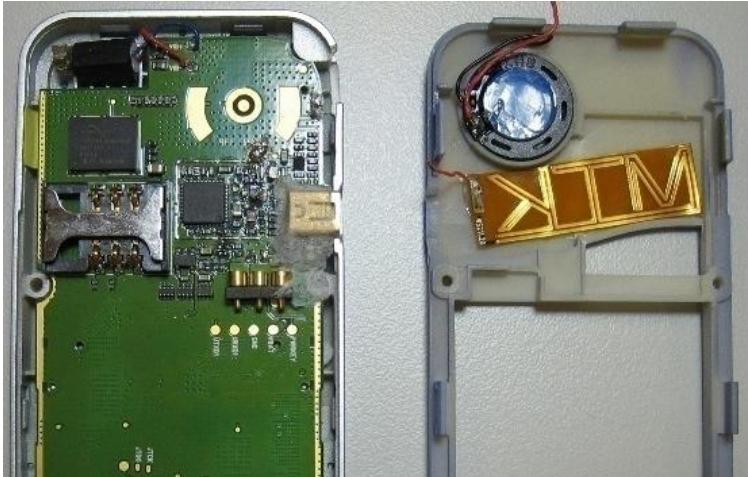
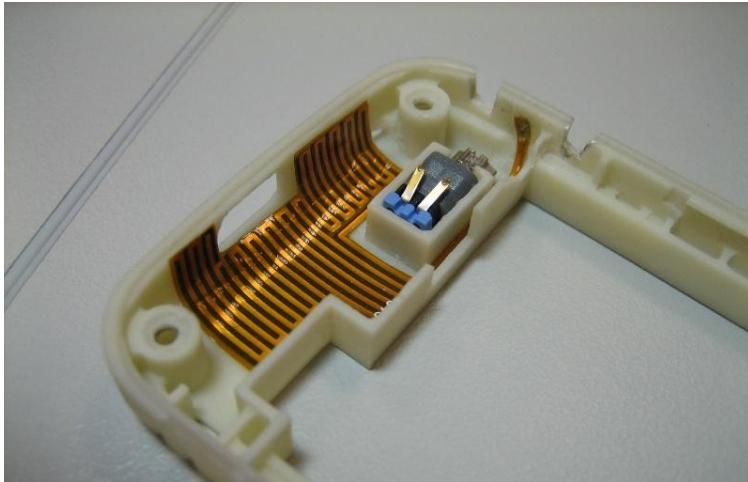
- FPC is parallel to PCBA
 - Distance 3~4mm from PCBA
 - DO NOT** overlap with Battery.



- Reserve over **300mm²** area for PFC.
- Keep away from any metal mechanical components, such as shielding cases, speakers, vibrators, card holders, and cameras.
- Only one feed point is enough for FPC type FM short antenna.
- For the layout on FPC, it is an around 500mm~1000mm long and 0.5mm wide strip meandering on the both side of FPC.
- The antenna operates as a monopole.

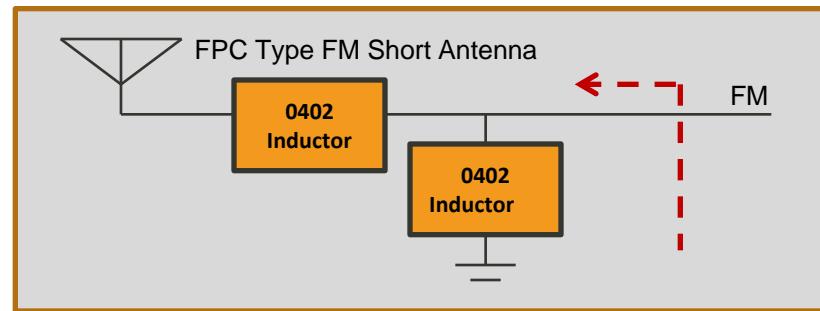
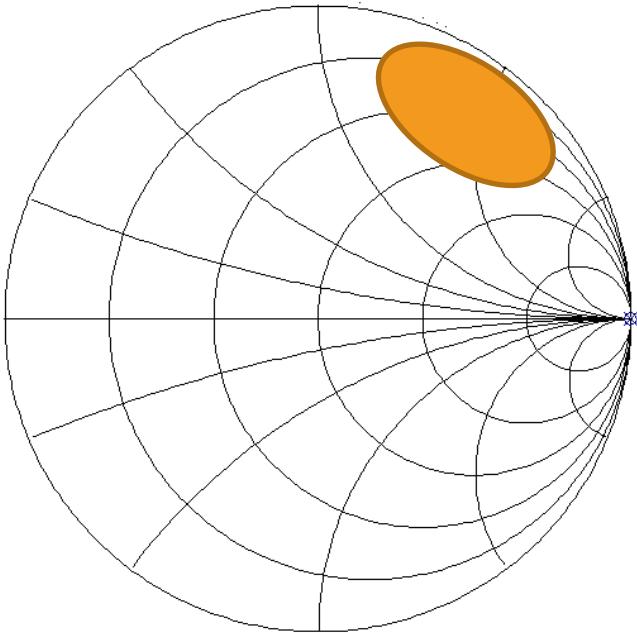
FPC Type FM Short Antenna (3)

- Examples of Implementation



FM Short Antenna Matching

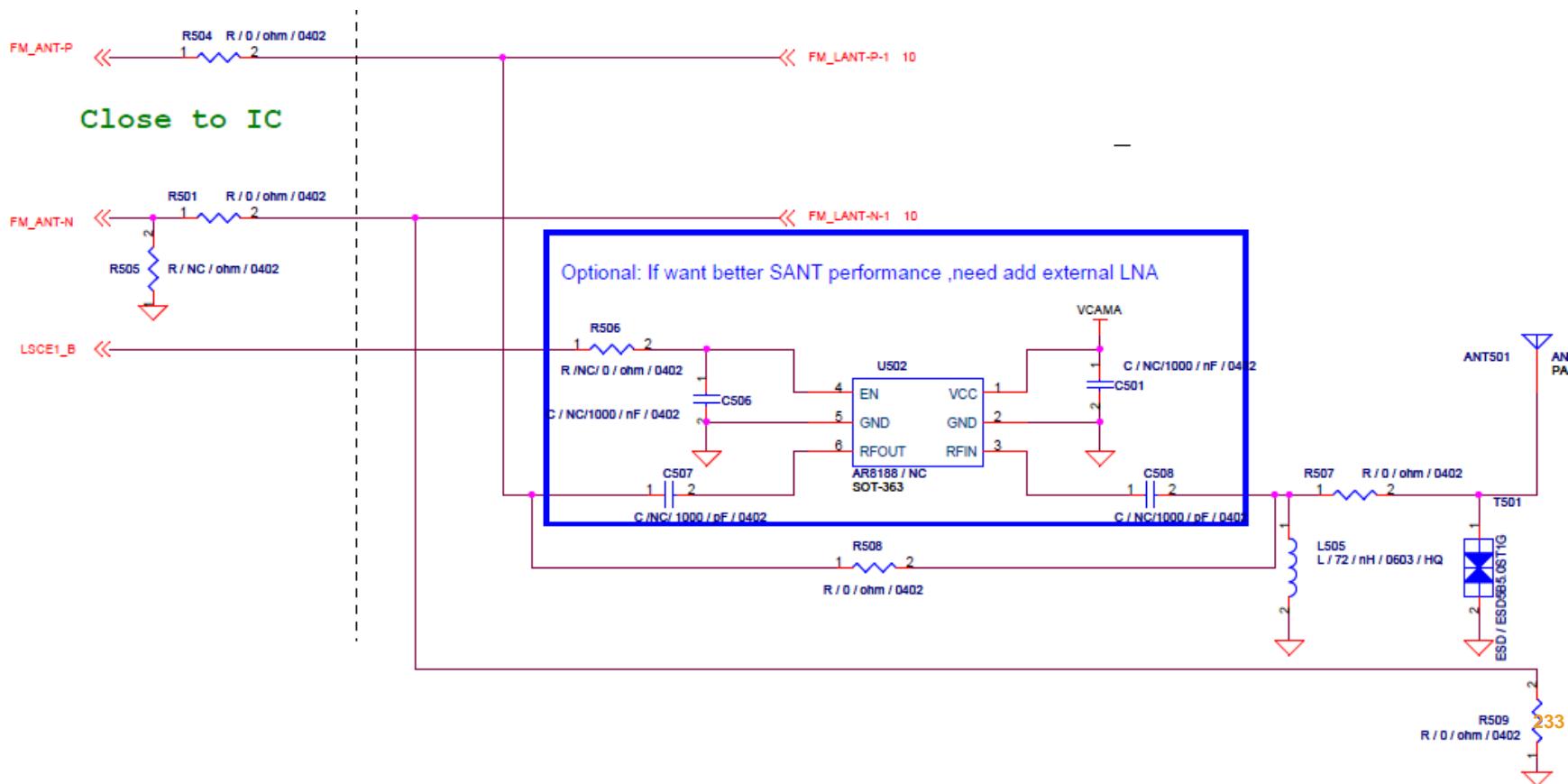
- The suitable region of FM short antenna matching on smith chart as shown below.



- Series 82nH and shunt 100nH is suggested.
- Put matching components near Short Antenna.
- Customers should double check the accuracy of the impedance.

FM Short Antenna Design

- Optional: If want better SANT performance ,you need add external LNA(AR8188).
- **Note:**Mediatek does't provide technical support for this kind of design , you can get technical support from **Airoha**.
- Airoha Contact:
 - Name: Raindrop Chang
 - Mail: RaindropChang@airoha.com.tw





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