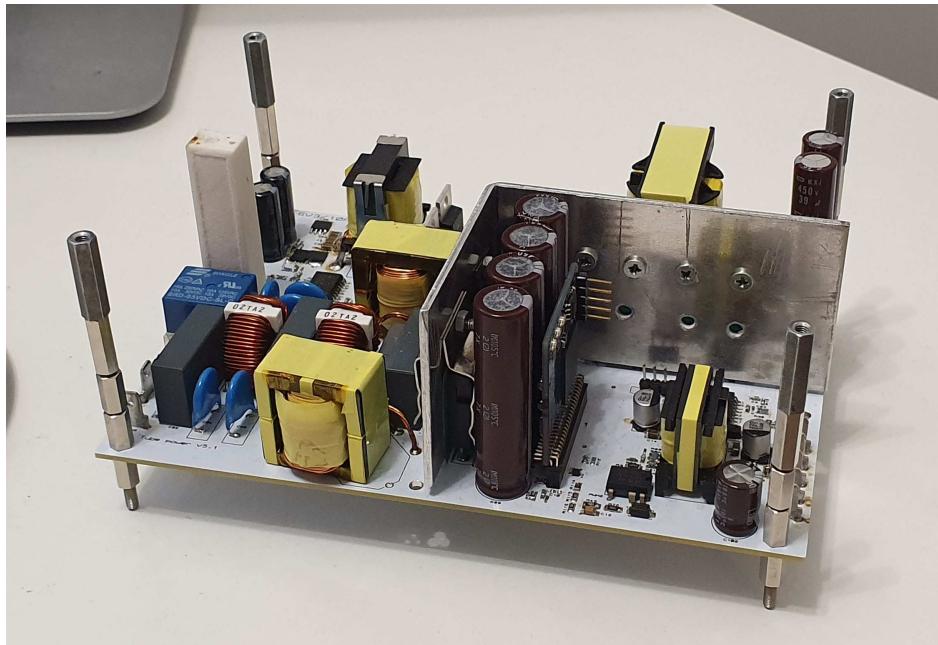




Lappeenranta
University of Technology

Jari Honkanen

DESIGN AND IMPLEMENTATION OF A TUBE AMPLIFIER POWER SUPPLY



Abstract

Jari Honkanen

Design and implementation of a tube amplifier power supply

Electronic tubes are still used for audio and musical instrument amplification. Tubes are relatively complex to drive, as they require several drive voltages ranging from 400 to 6 volts. A power supply for tube amplifier has thus requirement for providing various voltages with several power levels. The power supply designed for the tube amplifier requires a power factor correction unit, a heater power supply, high voltage power supply and auxiliary supply.

The best possible choices for the power electronic circuits were evaluated and a dual active half bridge converter was designed for the anode voltages, a resonant LLC converter was designed for heater supply, a DCM dual boost PFC was built and a quasi resonant flyback converter was designed for the auxiliary voltages.

For the feedback and system control an embedded control platform was developed. For the embedded controller a Field Programmable Gate Array was used. The power supply was built and tested with resistive loads in laboratory and the design was verified to be efficient enough in order to not require forced air cooling.

Keywords: digital control, power electronics, power factor correction

Contents

Abstract	2
List of Symbols and Abbreviations	3
1 Introduction	4
2 Auxiliary supply design	7
2.1 Flyback design	8
3 Power Factor Correction	11
3.1 Input current measurement	13
3.2 EMI filter design	14
4 Heater Voltage Supply	16
4.1 LLC converter design	18
4.1.1 LLC transformer design	18
4.2 LLC control	20
5 Dual Half Bridge Design	23
5.1 DHB design	25
6 Embedded control platform design	28
6.1 FPGA control platform design	29
7 Conclusion	33
References	35

Chapter 1

Introduction

Tubes were the first real application of electronic circuits as they could be used as an amplifier, thus were the original building block for communication circuits and for audio amplification. The electronic tubes are still used in audio and musical instrument amplification.

The tube construction is that of a glass bulb with indirectly heated cathode and high voltage anode between which a wire mesh called grid is placed. The grid allows the current between the cathode and anode to be controlled with an external voltage. In addition to the control grid, tubes also commonly have several other grid structures which offer higher gain and improve linearity or power. Typical tubes are triode, pentode and tetrode with 1, 3 or 4 grids respectively in addition to the anode and cathode. In order to control a signal with a tube, the typical voltages that are needed are anode voltage, heater voltage, a grid bias voltage and the drive signal.

The tube amplifier is designed to support all common tubes that have common octal socket. In order to support common tubes, the anode voltage is chosen to be such that the 6l6gc tube with the lowest anode voltage of 500 V can be safely used. In the power amplifier circuit, the anode is connected to the screen grid with a resistor, thus, the screen grid is also powered with the anode supply.

The bias voltage is designed to be such that the tubes can be completely shut off with bias. The highest negative voltage needed to offer zero anode current

is with 6550 tubes which require -60 V, thus -80 V is chosen to ensure safe turn off even with tube being off specifications.

The amplifier supports 4 power tubes and 5 pre amplifier tubes, thus the total maximum current consumption for the heater supply is less than 10 A. The highest load is when the power tubes are 4 x KT66 drawing 2 A each and the pre-amp tubes draw 300 mA each, which results in 9.5 A current drawn from the heater supply.

In addition to the control voltages, the power supply needs to supply auxiliary voltages for the power electronic circuits. The embedded system and measurements are supplied with a 5 V voltage and the gates of the switching mosfets are supplied with a 15 V voltage. The tube amplifier also needs -5 V negative control voltage. The voltages required from the power supply are listed in table 1.1

Table 1.1. Power supply output voltages

Anode voltage	410 V	1 A
Heater voltage	6.3 V	10 A
primary auxiliary voltage	5 V	0.2 A
primary gate voltage	15 V	0.2 A
secondary auxiliary voltage	5 V	0.2 A
secondary negative auxiliary voltage	-5 V	0.2 A
secondary gate voltage	15 V	0.2 A
Bias voltage	-80 V	10 mA

The total approximated maximum power of the bias, gate and auxiliary voltages is 10 W thus they are supplied with a single auxiliary supply power stage. The auxiliary supply voltages also have relaxed regulation properties as auxiliary voltages are used as raw voltages for downstream regulation, the embedded and measurement circuits are supplied with 3.3 V or lower voltages and the gate voltages have high margin for proper operation. The anode and heater supplies are relatively high power thus they have dedicated power stages.

In addition to the output voltages, the input voltage and current drawn from the mains needs to be controlled. The input current is controlled with a PFC. The complete power supply thus has 4 controllable power stages, anode sup-

ply, auxiliary supply, heater supply and PFC. The chapters denote the design and implementation of the embedded control platform design and the power supplies are described in their own chapters.

Chapter 2

Auxiliary supply design



Figure 2.1. Auxiliary supply

The auxiliary supply has three main design goals it needs to accomplish. It needs to provide the bias voltage for the power tubes, power the embedded control system and it needs to start when the DC link voltage is present. Since the auxiliary supply is by far the most common power supply as it is part of almost every mains powered power electronics system, the design methods are very well documented and understood. For low power multi-output design the flyback converter is the only viable option. The converter is very small, the extra outputs require minimal components with just a diode and a capacitor and it has relatively low losses due to zero current switching.

As with the high volume design, the auxiliary supply can be easily constructed

with an embedded controller housing all of different parts of the flyback converter. Since the auxiliary is so ubiquitous, several different ICs are available which accomplish all of the required functionalities

Desired features for the controller are integrated switch, minimal amount of extra circuit, integrated protection features and ability to start to highly capacitive load. As the maximum expected power level is around 10 W the part chosen was IW1818 from Dialog Semiconductor which has all of the required features. The IW1818 is protected from thermal stress, over current, over voltage and provides a quasi resonant switching for minimal EMI and low loss. The controller also features primary side feedback without any need for external feedback compensation. Thus the chip requires minimal design aside from providing the proper connections. Several similar chips are available from TI and Infineon.

2.1 Flyback design

The basic circuit is shown in Figure 2.2. The circuit is started when the capacitors C58 and C51 charge beyond 14 V. The initial charging is provided directly from the DC link with the 1 MOhm resistors R114-R116. The diode D10 is used to isolate the 220 μ F capacitance from the DC link pre charge resistors in order to provide faster start. As the start voltage of 14 V is reached, the voltage is ramped up against the maximum current set by the resistors R8 and R9, which set the current peak reference to 800 mA. The secondaries have 12 kOhm resistors providing small load for each output, which helps keeping the voltages of unloaded outputs from getting excessively high.

The resistors R64, R81 and R84 and R85 are used as a resistor divider to set the feedback voltage level. Since the IW1818 is designed to use the transformer secondary winding voltage directly as feedback, the voltage level is chosen to take into account the diode voltage drop. As a single switch flyback design is used a snubber circuit is required. However, the exact component values for the snubber circuit are not important as long as the capacitance is large enough. Voltage ringing is desired as it is used for providing a quasi resonant operation, therefore an additional resistance R72 is added to provide higher impedance to the RCD snubber circuit. The resistor is chosen so that

the peak 800 mA current flowing through the resistor leaves still ample headroom for the 800 V internal transistor when added to the 120 V designed snubber voltage. The peak transistor voltage with the series snubber resistor is thus 600 V.

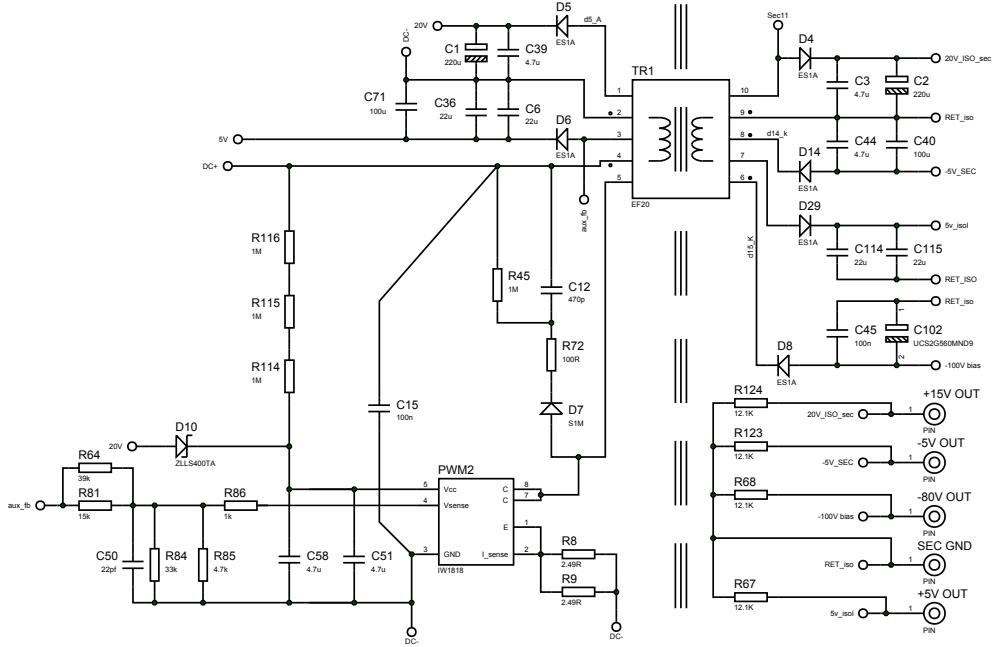


Figure 2.2. Auxiliary supply schematic

The transformer design was directly taken from Fairchild AN-4137 (Fairchild, 2003). The algorithm requires ripple factor, which determines the peak to average current ratio, the secondary voltages, maximum duty ratio, peak magnetic flux density, switching frequency and the transformer core geometry. The IW1818 operates at 72 kHz and the voltages are determined by the requirements of the power supply, thus the design only calls for deciding the core geometry, ripple factor and peak flux density. EF 20 core is the only reasonable choice for the transformer as the next size down is too small to allow for the total 6 mm border tape and the next size up is EF 25 which would be enough for around 20-30 W flyback.

The transformer was iterated by changing the ripple factor, minimum input voltage rating and core saturation flux density until a satisfactory design was obtained. A practical requirement was also that a standard air gap could be used to prevent the need to add the gap with tape. The final design for the

flyback transformer is given in table 2.1

Table 2.1. Auxiliary supply design factors

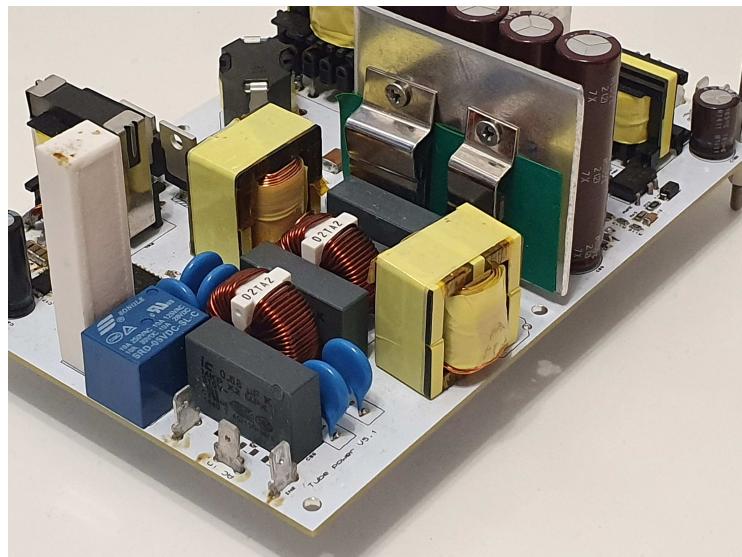
Core geometry	EF20
Primary turns	52
5V winding turns	3
15V winding turns	8
80V winding turns	42
Switching frequency	72 kHz
Peak transistor current	806 mA
Peak transistor voltage	520 V
Ripple factor	2.35
Peak magnetic flux	330 mT
Primary inductance	614 μ H
Core inductance factor	175 nH

All of the windings are wound with three parallel strands of awg 34 wire with a total area of 0.06 mm^2 . With a typical 4 A per square millimeter rating, all of the secondary windings are very conservatively rated at 240 mA . Since the transformer has requirement for reinforced isolation, the coilformer is taped with 3 mm border tape to provide end-to-end creepage distance of 6 mm between the primary and secondary windings. Additionally, 4 layers of tape is added between the primary side and secondary side windings to reinforce the primary to secondary isolation.

The flyback was tested to work as intended with minimal iteration. No extra effort was made to minimize the stray inductance, which in a flyback decreases the cross regulation between different windings. However, since the feedback is from the primary winding directly without any filtering, all secondary voltages are effectively fed back as they are seen at the flyback voltage. This helps to balance the variation of different voltages.

Chapter 3

Power Factor Correction



Power factor converter can be accomplished with several power electronic circuits. The possible circuits for PFC are boost converter and active front end with full bridge. The other possibilities with filtered low distortion current waveform are Cuk, flyback, and single-ended primary-inductor (SEPIC) converters (Fardoun et al., 2012) (Bist and Singh, 2015), (Jovanovic and Jang, 2005). An active front end design with GaN switches was evaluated, but was abandoned due to the space requirement for 2 isolated gate drivers. The half bridge GaN design was successfully adopted to a single phase inverter design.

The circuit design for the PFC was chosen as bridgeless boost converter. The schematic for the designed PFC is shown in Figure 3.1 along with the EMI filter and charge resistor. The PFC is protected with a standard diode bridge denoted by DB1 in the schematic. The high frequency current does need a return path which is provided by the diode bridge and additional X capacitors C64 and C66 which are in parallel to the low side diodes of the diode bridge.

The bridgeless boost has all of the desirable features of a boost converter, mainly the gate drivers are ground referenced, and with the use of SiC diodes the boost has very low losses. The bridgeless boost does require two input inductors, but they can be designed for half of the current which keeps the size down. Since there is no input diode bridge, there are only 2 semiconductors in the current path, which affords the best conduction losses offered by any design (Singh et al., 2003).

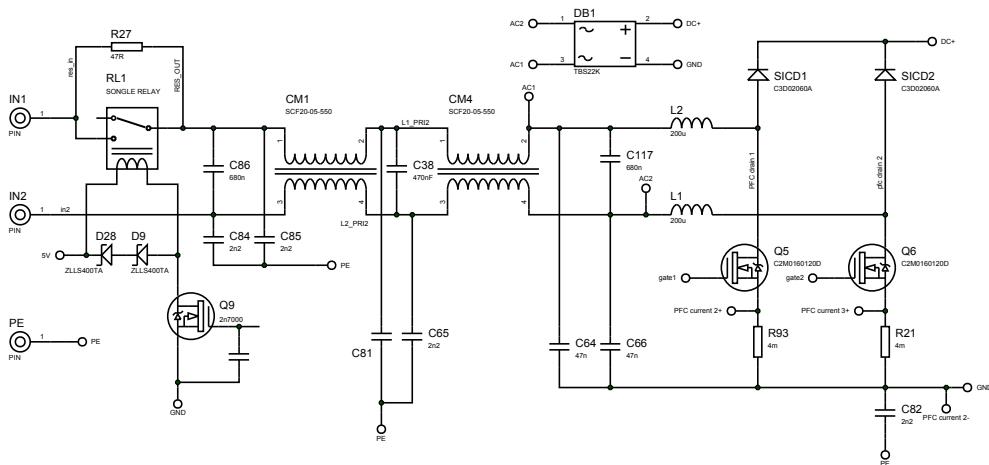


Figure 3.1. Bridgeless power factor correction schematic

The boost converter is designed to be operated in discontinuous conduction mode for 230 VAC mains voltage. The inductor was sized to be as big as possible, that can be easily fit in the PCB. The best design was experimentally tested to be constructed with 2 stacked EF 25 cores and the coil was wound on top of the cores without coilformer. The ferrite core was taped with several layers of capton tape to protect the windings against friction against the cores. The inductor was designed to be $200\text{ }\mu\text{H}$, which allows partial continuous conduction for powers over 400 W. In order to get continuous conduction for the pfc, either the switching frequency would need to be significantly increased, or the inductor would need to be several times higher in inductance. This

would be possible with powder core inductors, but they are not available for normal customers from any of the common suppliers like Mouser, DigiKey or Elfa. As of writing this, Mouser has recently stocked distributed gap amorphous toroid cores manufactured by Hitachi, that could be used for continuous conduction inductors with $500\ \mu\text{H}$ or higher inductance.

3.1 Input current measurement

The input current measurement was designed using a shunt current measurement from the source of the PFC mosfet. The shunt was chosen as it is extremely small and can be very easily fit in the PCB. The shunt current measurement is in the gate drive path and the gate drive current is seen in the current measurement, but since the current is sampled with an ADC that has a sample and hold amplifier front end, the sample is simply timed after the gate is already charged.

Since the voltage of the first X capacitor, C117 is measured, the current which is used for feedback is determined based on the input voltage. This has the extra benefit that the measured current is AC instead of rectified AC which is typically used for PFC current measurement. The significance of the AC voltage measurement is that the control sees AC current and standard grid tied inverter control design can be used for the PFC control.

The average current from discontinuous current waveform can be calculated from the a sample taken at the middle of the current waveform as shown in (Gusseme et al., 2005). As the middle point sampling is commonly used in both conduction modes, the DCM PFC control was not deemed a significant issue. The AC current measurement was tested with the PFC switches being switched at 780 ns constant pulse width. Since the minimum pulse is the worst case for the measurement, if the measurement works with minimum pulse it will work with all other pulselwidths also. The synchronous measurement with minimum pulse is shown in Figure 3.2 with the current measurement obtained from the FPGA via an UART. Due to the open loop operation, the half cycles show significant difference in amplitude. When the converter is in DCM conduction during open loop operation, a small difference in the filter inductance values cause a significant difference in the converter input current.

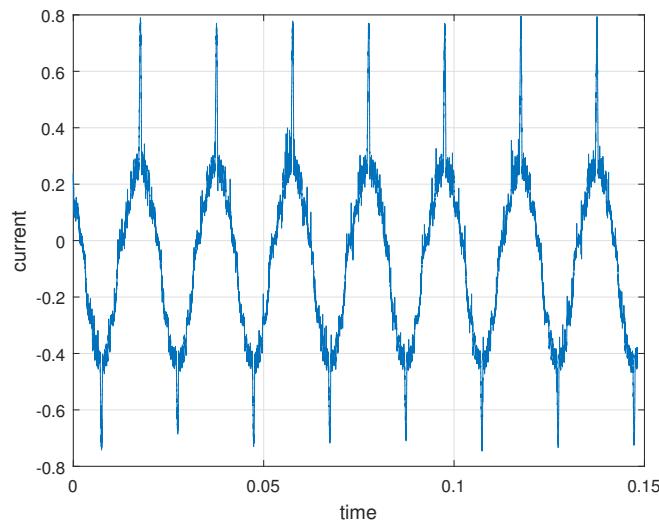


Figure 3.2. AC current measurement test with minimum pfc pulsewidth

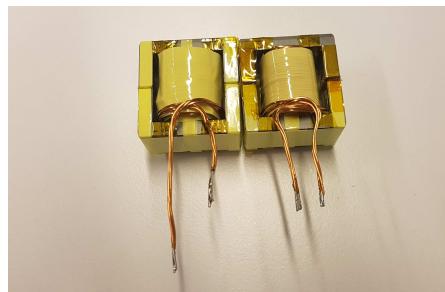


Figure 3.3. PFC inductor coils built using stacked EF 25 cores

3.2 EMI filter design

The EMI filter was designed with the stray inductance of the common mode inductors providing the inductance for the LC filter. The common mode inductors were measured to have $20 \mu\text{H}$ stray inductance. Since the X capacitors are in parallel, the capacitive load was designed to be under 35 VA which provides a power factor of over 95 with real power over 100 W. The EMI filter design was iterated to provide maximum possible attenuation for the switching frequency with the given inductors and a maximum of 35 VA capacitive loading. The best possible design that could be constructed with the

minimal number of X capacitors are three 680 nF X capacitors and extra 47 nF capacitor placed in parallel with the diode bridge.

The EMI filter design was measured with a Venable model 3120 vector analyzer. The measured response shows a -65 dB attenuation at the PFC switching frequency which was set to be below the minimum 150 kHz defined by CISPR 13. Since no LISN, nor an EMI measurement setup was available, no actual EMI filter measurements were made. Significantly higher attenuation is not possible with the designed EMI filter without increasing the total amount of X-capacitors which would reduce the power factor. Therefore if higher filtering was required an additional EMI filter would need to be constructed, or one of the common mode inductors changed to differential mode.

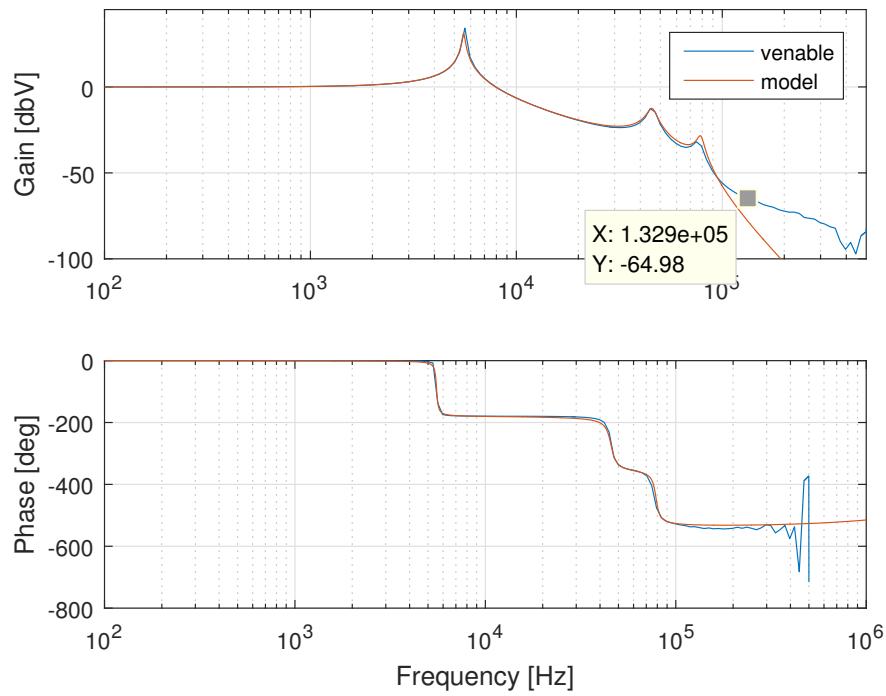
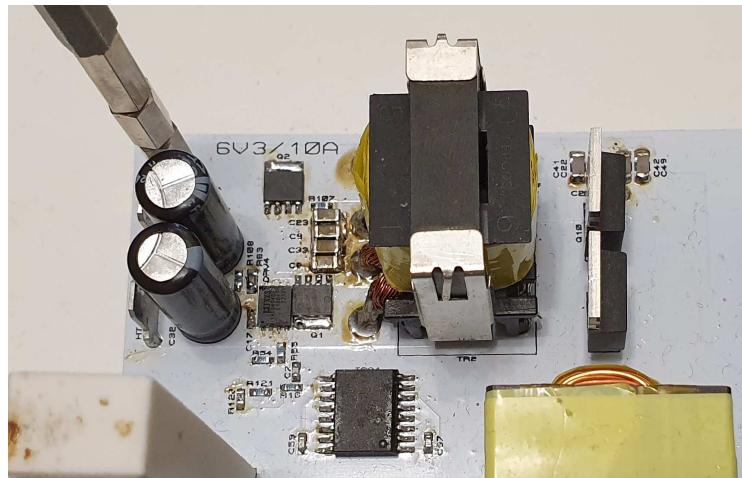


Figure 3.4. Modeled and measured emi filter input to output voltage response

Chapter 4

Heater Voltage Supply



The heater supply is needed to heat the cathode of a tube to high enough temperature, for the cathode material to start producing a space charge on top of the cathode element. The low heater voltage is directly applied to the tube, thus low noise in the heater voltage is beneficial in keeping audible hum and noise from disturbing the amplifier operation. Since the current is relatively high at 10 A diode rectification is impractical and thus synchronous mosfet rectifier is chosen. Since hard switching has much higher EMI, only soft switching power supplies are considered.

Soft switching options for the heater supply are active clamp forward and flyback, asymmetric half bridge converter with current doubler and flyback

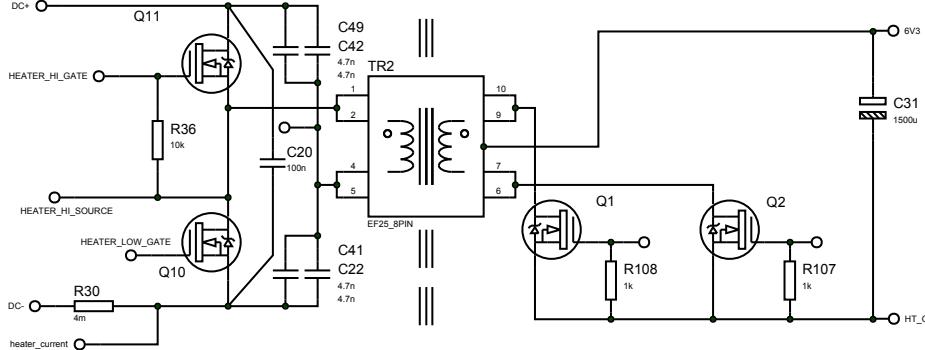


Figure 4.1. Schematic for the chosen llc topology. The primary is standard half bridge and a full wave secondary with synchronous mosfet rectifiers is used for minimal conduction losses.

secondary and a half bridge LLC converter. The active clamp designs have a significant issue with voltage strain for the input switches as the clamp capacitor voltage swings on top of the DC link voltage. The forward converters also have an inherent issue with the secondary side voltage peaking. Every transformer isolated converter where the switch is between the transformer winding and an inductor has an inherent problem with voltage ringing. Since the transformer secondary has some stray inductance, the switch drain-source capacitance must be able to store the energy of the transformer stray inductance.

The flyback secondary has the benefit that it has the output capacitor directly connected to the transformer winding through a rectifier, thus voltage ringing is not an issue, however the secondary side has high current peak as the current is only conducting half of the transformer period. Due to the shortcomings of all other possible topologies, the LLC converter is chosen.

The LLC converter is a series/parallel resonant topology. The transformer integrates both the series and parallel inductors and the half bridge capacitors act as the resonant capacitor thus the converter has a very simple structure with minimal number of components. The secondary is built with split secondary windings allowing the secondary fets to be ground referenced for simple gate drive. A standard charge pump with flying capacitor is used for the primary gate drive. The schematic is shown in Figure 4.1.

4.1 LLC converter design

LLC is a resonant topology with a series and parallel resonances. The nominal resonance frequency determined by the LC resonance of the series inductance and the half bridge capacitor. The other resonance is determined by the LC resonance of the combined inductance of the magnetizing inductance and the stray inductance together with the half bridge capacitor. The lower resonance frequency determines the lowest frequency at which the LLC can operate and the nominal resonance frequency determines the operational range. Among the benefits of the LLC is that the stray inductance can be designed to act as the series inductance of the resonance circuit and the magnetization inductance can also act as the parallel resonant inductor. Thus the transformer provides both inductances and the half bridge capacitor can be used to form the resonance capacitor.

The LLC converter transformer is designed to provide high enough magnetization current to guarantee zero voltage switching for the primary side. The secondary side switches rectify the resonating current, thus the current commutes the secondary switches. As the magnetization current does not flow through the secondary, as long as the switching period is longer than the resonant period, the resonating current has enough time to reset to zero. With the operational frequency kept lower than the primary resonance frequency, the secondary switches have both soft turn on and turn off.

4.1.1 LLC transformer design

Since the LLC has very low losses, the transformer is designed based on the assumption that no voltage is lost in the converter. The topology offers boost to the voltage with operational frequencies below the main resonance. Small boosting is desired as it sets the maximum switching frequency below main resonance which also guarantees that the converter is operated with zero rectifier switching losses under all operational conditions. The very high efficiency of the converter also give lots of freedom to choose the core geometry since the operational frequency has very small impact on overall losses. The core geometry was chosen to be EF25 as it could be easily fit in the PCB.

Since the half bridge circuit halves the input voltage, the transformer needs to have a voltage ratio of 200 V/6.3 V which is close to an integer ratio of 32/1. The practical options for the transformer are thus 1, 2 or 3 turn secondaries with primary having 32, 64 or 96 turns. The operational frequency of the converter is determined by the stray inductance of the transformer since the magnetizing inductance can be tuned by simply increasing the air gap of the core and the capacitor can be chosen arbitrarily. Practical values for magnetization inductance are 6 to 12 times the stray inductance. The inductance ratio determines the range of frequencies at which the converter is operated as the magnetization inductance determines the lowest frequency at which the converter is still soft switched. The amount of voltage swing in the resonance circuit determines the gain of the converter with higher peak resonating voltage offering wider operational voltage range for the converter. The capacitor value is thus determined by the load current.

There are several methods to calculate the required stray and magnetic inductance and resonant capacitor. Since the stray inductance is difficult to design, the LLC converter design was iterated by building the transformer and measuring the stray inductance. The 32 turn primary design was determined to yield a stray inductance under 5 μ H and an operational frequency beyond 500kHz and thus was abandoned. The 64 turn primary designs were tested with straight winding, the secondary sandwiched between two 32 turn primaries wired in series and secondary between 2 64 turn primaries in parallel. The resulting transformers are given in table 4.1. When operated be-

Table 4.1. LLC transformers

Core geometry	EF25
64 turn flat winding	62 μ H
32 turn primary windings in series	24 μ H
64 turn primary windings in parallel	42 μ H

low the resonance of the magnetization inductance, the LLC is no longer soft switched. Based on simulations, the parallel primary design for the transformer was chosen. An off the shelf core with gap of 1 mm gives a magnetization inductance of 320 μ H and an inductance ratio of 8 and high enough magnetization inductance to guarantee soft switching in the primary side. The resonance capacitor was chosen as 22 nF which results in a resonance fre-

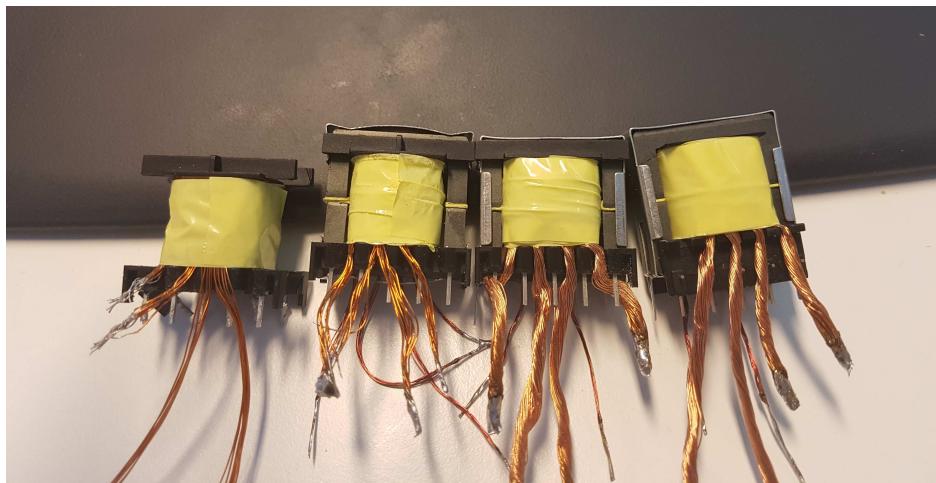


Figure 4.2. LLC transformer test units. The transformers are 32 turn primary with 1 turn secondary, 64/2 turn flat wound primary, 32 turn primary windings in series with 2 turn secondary and two 64 turn primaries in parallel with 2 turn secondary.

quency of 220 kHz and the converter was designed to be controlled with a switching frequency between 270 kHz and 150 kHz. The high frequency is needed at startup to limit the current drawn by the empty secondary capacitors.

4.2 LLC control

Since all of the stored energy is transmitted through the transformer inside one transformer period, the dynamics are very fast. Because the LLC offers fast intrinsic dynamics, the PI control is tuned experimentally.

Above the resonant frequency, the synchronous rectifier is controlled with same gate drive signals as the primary. Below the resonant frequency the rectified current is zero for part of the half cycle. The synchronous rectifier needs to be turned off before the period ends or the current will swing negative which increases conduction and switching losses. There exist several papers to model the synchronous rectifier operation, however the typical performance boost is fractions of a per cent which is mostly irrelevant for the heaters. Therefore a constant maximum conduction time is used for the

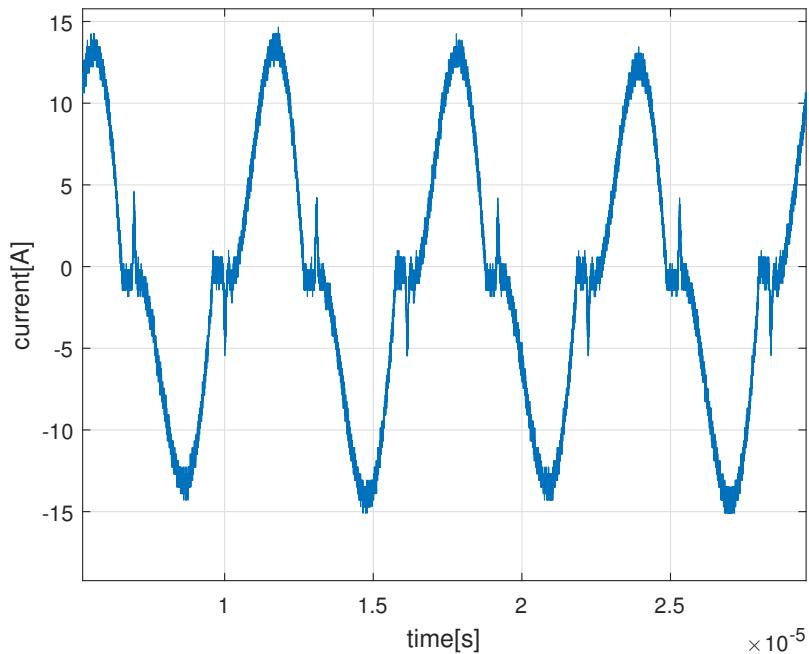


Figure 4.3. LLC current at 6.5 A current

synchronous rectifier. Since the main resonant frequency flows through the transformer directly, the conduction time for the rectifier is determined to be the half period of the 220 kHz resonant frequency. Since there is delay from the switches, gate drivers and isolation the maximum conduction time was experimentally measured to be 680 clock cycles which corresponds to 2.65 us. Longer than that, the current would swing negative and extra conduction losses would occur.

The LLC secondary current at 6.5 A is shown in figureFigure 4.3. The current is measured from the secondary windings with two Rogowski coils. The initial current spike just before the main current waveform is caused by too early synchronous rectifier conduction. This can be mitigated by delaying the secondary fet pulse by the amount of reverse conduction.

Last issue with the LLC converter is the startup. Due to the relatively high transformer turns ratio, the secondary has 33 times higher current than the primary. The 40 uH stray inductance limits the primary current at the initial

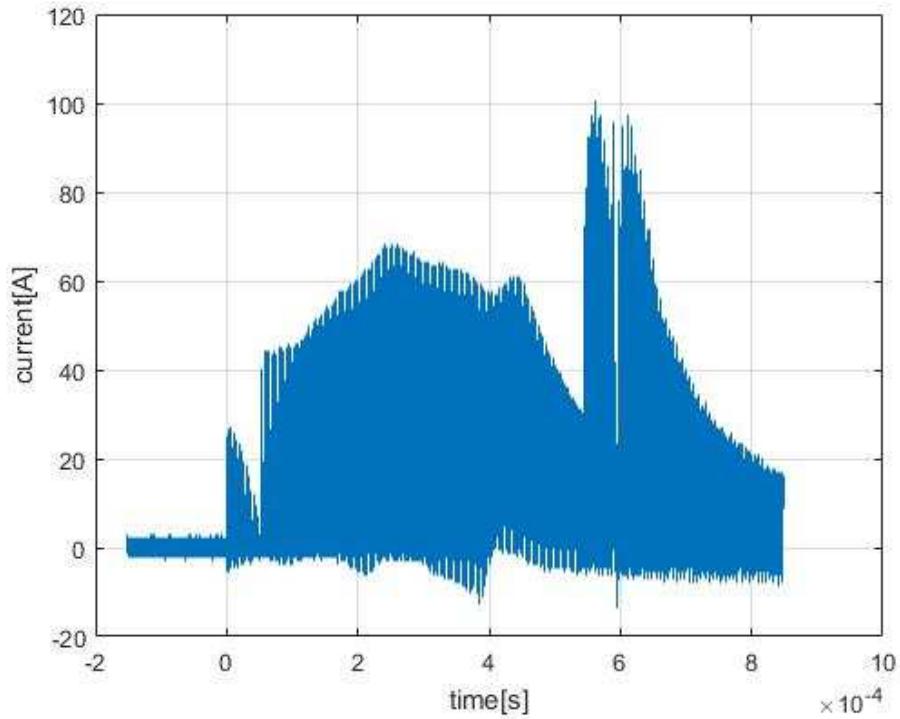


Figure 4.4. LLC current startup

270 kHz switching frequency to less than 5 amperes, but the secondary has over 100 A current spike. The initial high current spike is still within specifications, but it is limited by ramping up the pulse width. The startup current with pulse width ramp up is shown in Figure 4.4. The highest peak current is 100 A which is still well within the specification of the ceramic capacitors used for secondary.

Chapter 5

Dual Half Bridge Design

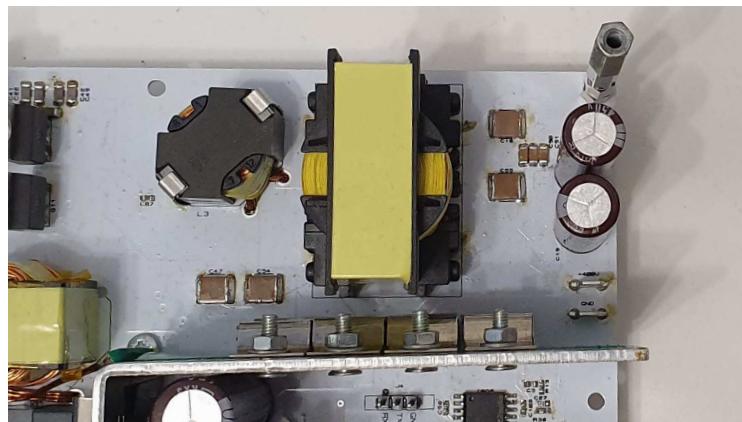


Figure 5.1. Anode supply

As the nominal DC link voltage is 400 V and the desired anode voltage supply is voltage designed to be 410 V, there are are much more limited options for the high voltage supply. This practically rules out all variations of single quadrant flyback and forward converters as they inherently have voltage stress higher than the DC link voltage. Any converter with DC inductor in either side of the transformer is also practically out of the question as the inductor would need to be extremely high in value due to low current output as well as the basic issues with voltage spiking due to transformer stray inductance.

The options for the high voltage supply are thus the LLC converter and a dual

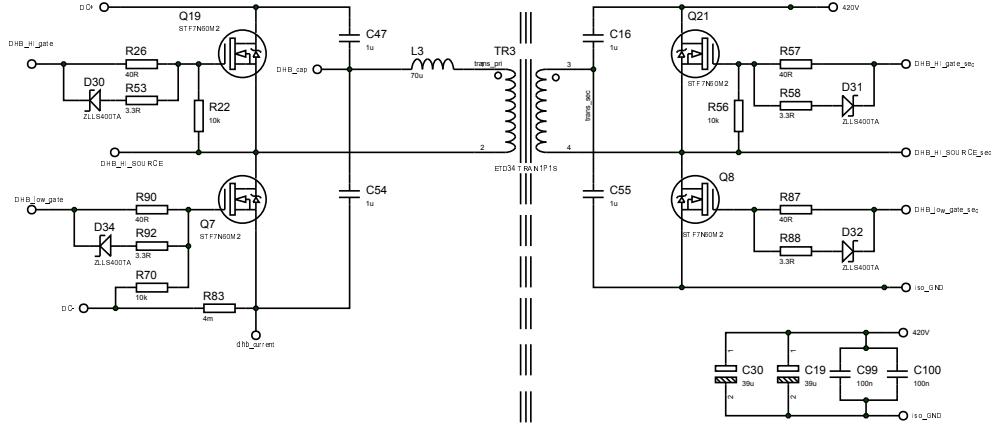


Figure 5.2. Dual half bridge schematic

active bridge. The load can vary from zero to full load with the music being played, thus in order to keep the output voltage steady, a bidirectional converter is chosen. If voltage is too high and load is small, with a bidirectional converter the output can be actively pulled down faster than would be possible with just the load current discharging the extra voltage from the capacitors. The only viable option is therefore the dual active bridge converter.

Since the power levels are low, the dual active bridge is built with half bridge in the primary and secondary side. Even at the full load, the current is only 1 A or less, thus the half bridge construction allows doubling the current of the active bridges. The double current helps the system to remain soft switched for wider load range, which lowers the switching losses at low load.

Typically the dual active bridge soft switched only when load current is high enough that the stray inductance energy can charge the switch capacitance during dead-time. In order for the dual active half bridge to remain in soft switching for the entire load range an air gap is introduced to the transformer. The air gap which allows the magnetization current to be increased to the point that it alone is enough to force the system into soft switching even at zero load. This allows the half bridge which magnetizes the transformer to remain in soft switching for the entire load range.

5.1 DHB design

The design for the DHB consist of choosing a turns ratio and size of the inductance. The transformer is designed to have a maximum of 1 W core losses which is accomplished with using a minimum of 26 turns. Since the converter needs a slight boost as the secondary voltage is designed to be 410 V thus the turns ratio is chosen as 26 turn primary and 29 turn secondary. This sets the nominal voltage at 446 V which accommodates for voltage lost in the charging and discharging the transistor drain-source capacitance and the inductive voltage divider formed by the external stray inductor and magnetization inductance. A ETD 34 core with 0.1 mm gap is chosen as it yields a magnetization inductance of $530 \mu\text{H}$. The gapped core which with a switching frequency of 135 kHz guarantees a 700 mA peak magnetization current and soft switching for the primary side bridge.

The initial startup of the DHB is accomplished by using a half length first pulse on the primary. Since the secondary is at zero volts, the amount of phase shift does not have any effect on the current, thus the control cannot increase the current excessively. The current is limited only by the stray inductance. The high side gate driver is powered with a bootstrap capacitor which does not have enough time to charge during the initial pulse, therefore the LC filter formed by the half bridge capacitor and the transformer oscillates for a few times during the startup. The external inductor has high enough winding capacitance that the current has high levels of current spiking and oscillations.

The full load current at 700 mA is shown in Figure 5.4. The current shows significant amount of ringing during the phase shift period, due to high winding capacitance of the external ac inductor. The power supply however does not produce significant losses, thus the ringing is mostly a probable EMI issue. The current ringing is several times higher in the primary than the secondary, implying that the transformer also has excessive winding capacitance. The transformer was constructed with a layer of tape put between every winding layer and extra 5 layers of tape was put between primary and secondary. The tape also decreases the magnetic coupling between windings, which is not an issue with the DHB topology as more often than not external inductor is needed regardless.

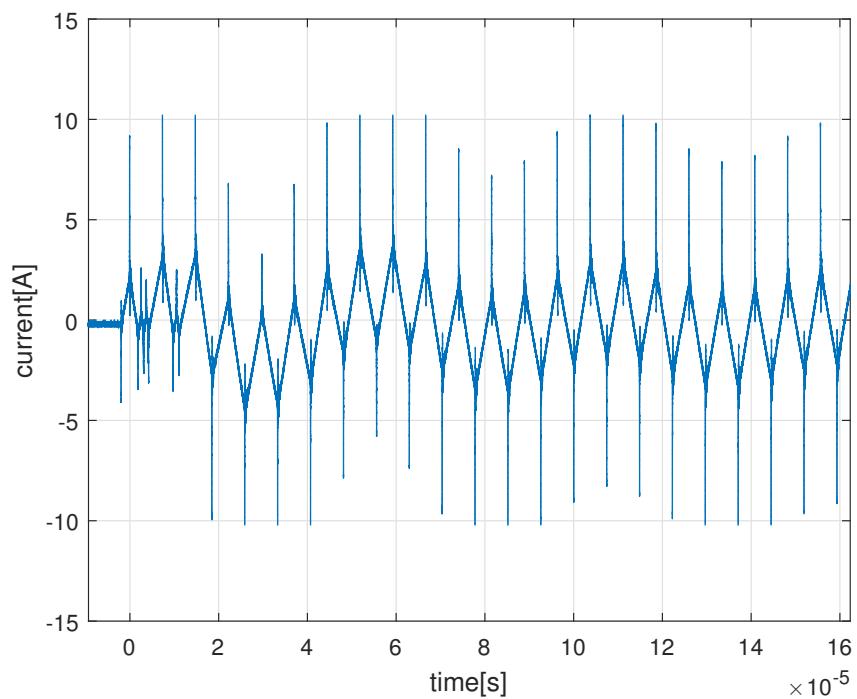


Figure 5.3. initial startup of dhb converter. The bootstrap capacitor does not have enough time to charge during the first 2 pulses, which prevents proper startup with minimal transient and oscillations.

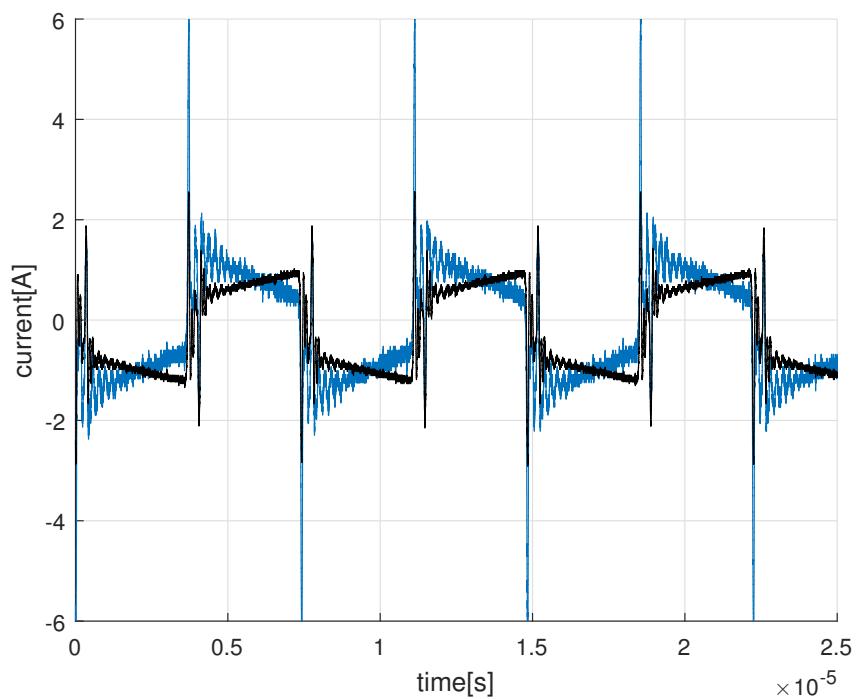


Figure 5.4. Full load current of the dual half bridge. Primary current is slightly higher than the secondary current due to the magnetization current and because the transformer has turns ratio of 26:29.

Chapter 6

Embedded control platform design

The option for controlling the power supply is with either a microcontroller or an FPGA. Usually micro controllers are thought to be a much easier solution than custom hardware design as much of the peripherals are ready made and operable with only a configuration. C2000 series micro controllers were evaluated for the embedded platform as they are specifically designed for power control purposes, however after several attempts the dsp design was abandoned due to the limitations of the hardware and the final issue being the required timing. The power supplies are operated at 135 kHz and all of the power supplies require both current and voltage controllers along with the modulators, protection features and controlled soft starts. Even with the highest performance c2000 core running at 200 MHz there is less than 500 clock cycles to be used for controlling each of the power supplies at the switching frequency. Since the power supply requires communication for debugging the embedded system would also require a real-time operating system to allow for better resource utilization for slow and fast time scale operations. It was thus apparent that fully custom hardware would be significantly easier to build and design than to use a microcontroller.

The first version of custom hardware was a control card with both, a C2000 series microcontroller with an additional processing core and a FPGA to be used for timing and modulation, but this design was also abandoned due to the loss in performance given by the the communicantion between the processor and FPGA. Since the additional core cannot directly communicate with the FPGA, the communication between FPGA and two processor cores was too



Figure 6.1. Control card with Texas F28035 and Lattice MachXO3LF FPGA



Figure 6.2. Cyclone 10 LP FPGA card with on board dual ADC and analog multiplexers.

slow. The fpga is also housed in a microbga package for which the pcb requires costly via plating and $70\text{ }\mu\text{m}$ trace widths, thus making the control pcb much too expensive for the low performance it offered. This design was however needed, to learn how to use FPGA and to port the existing code base to from C and assembly to VHDL.

6.1 FPGA control platform design

The control platform was designed to be self contained by having on board ad-converters and analog muxes offering dual 7 channel adc IO for the control measurements and 32 general purpose digital IO designs. The embedded control platform is shown in Figure 6.2. The basic features are three rgb leds in the top left corner, jtag and flash memory on the top right corner. The underside has the analog section with two analog multiplexers, ad converters and on-board power supplies which regulate the 5V voltage to 3.3 V IO voltages, 1.2 V core voltage and 2.5 V PLL voltage used by the FPGA.

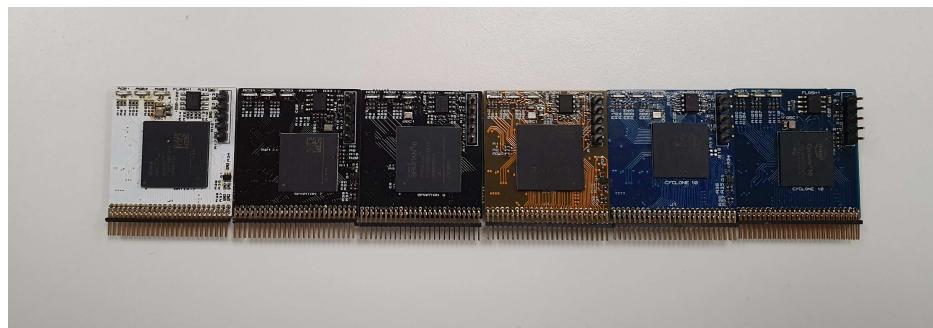


Figure 6.3. Different FPGA design evaluated for power supply control. The FPGAs from left to right are Artix 7, Spartan 7, Spartan 6, ECP5, Cyclone 10 LP with 12 bit adc and Cyclone 10 LP with 14 bit adc converters.

As the VHDL is easily portable across different vendors devices and as of writing there exists only Intel, Xilinx and Lattice as FPGA supplier, all of the available FPGAs in a similar price range were evaluated. The evaluated FPGAs are the Artix 7, Spartan 7 and Spartan 6 from Xilinx, ECP5 from Lattice semiconductor and Cyclone 10 LP from Intel. The evaluated FPGAs are shown in Figure 6.3. The same basic design for the embedded platform was used, and since all of the FPGAs are offered in a similarly sized ball-grid array packages, changing the FPGA device was relatively straightforward. As the author had practically zero experience with FPGAs or VHDL, the use and design with several different devices was undertaken to get a good grip on for how FPGAs are used, how systems are designed for reusable code and portability and how FPGAs in general perform.

The complete system design has main parts for initial DC link charging through resistor and resistor bypass, control and startup scheduling for PFC, LLC and Dual Half Bridge converters. The main design units of the design are

- System control
- On-Board ADC
- External ADC
- PFC control
- Dual Half Bridge control

- LLC control
- UART

Depending on the FPGA the total design takes from 1500 to 2300 FPGA logic units and requires 8 18x18 bit multiplier cores and has either 2 or 3 clocks depending on whether the 12 or 14 bit ADC is used. Even the smallest device available, which is the 4k Logic unit spartan 6 could fit the design with relative ease. The power supply control can be thought of being a small and simple design when compared to the fact that all of the devices can be bought with hundreds of thousands of logic units and hundreds of dsp cores. The evaluated VHDL code was not complete with some protection features and error handling features missing as well as general refactoring needed for the code base. However the final design would probably not have an uart as the guitar amplifier does not need to communicate with anything and the missing trip and protection features probably require less logic than the UART consumes. Thus the missing features would probably not significantly increase the total system size and would definitely fit inside a one size larger FPGA than the smallest available.

The embedded system design was successfully compiled to each device and all could meet the timing requirement for 256 MHz modulator clock and 128 MHz dsp clock design. The 7 series xilinx devices offered roughly 20-30 % higher maximum clock speeds for the design than the cyclone 10 and spartan 6 whereas the ECP 5 was within 10 % of the maximum supported clock speed.

As it would make very little difference in terms of system performance whether the modulators were operated at 256 or 350 MHz thus for this design the choice of specific device would be pricing and personal preference. The ECP5 is by far the cheapest device out of all of the possibilities being priced at less than 5 € with Xilinx devices being 3-5 times as expensive and Intel costing 20-30 % more.

The bulk of the design was tested and designed with the Cyclone 10 as the intel quartus tool is by far the fastest to compile the full design. The intel quartus software offered over 50 % faster compilation time than the Vivado which was slowest for the design at around 2 minutes, which is fast enough to be practically irrelevant. The quartus was also easiest to get started with

thus it still remains the first choice for FPGA designs for the author. The Lattice Diamond and Xilinx PlanAhead, which is used for spartan 6, were similar in compilation speed at around 1 minute and 30 seconds. The Intel Quartus, Xilinx Vivado and PlanAhead as well as Lattice Diamond are all scripted using TCL language, thus the different tools also are quite similar to use.

Since all of the tools were used with free licence, the IP selection could be a defining reason for tool and chip selection. Intel also has very high performance Nios II soft processor IP core, which was tested to offer 150 MHz core clock performance. Thus if the design would have needed a processor, the Intel Nios II could have been used. Lattice Diamond licence also supports the Lattice Mico32 soft processor ip, which offers maximum clock speeds up to 80 MHz. Neither of the Xilinx tools offer MicroBlaze soft processor without purchasing it separately, thus it was not evaluated. The Quartus is the only tool which does not support logic group placement with free licence, which in a more substantial system could be a significant issue. The soft processor was not used for the final design, but for much more complex design a soft processor would be mandatory if external processor was not used.

In addition to evaluating different FPGAs, different ADCs were tested for power supply control purposes. The three evaluated ad converters are 12bit Maxim MAX11115 and TI ADS7883, both of which support maximum of 2 MHz sampling rate and a TI 14 bit ADS7056 with 2.5 MHz sample rate. All of the ADCs offer less than 500 ns sampling time. All of the adcs have good enough linearity for having no missing codes meaning that all of the words appear when the input is ramped from 0 to 3.3 V. As the adc is part of a feedback loop even the difference between 12 and 14 bit adc was indistinguishable. The performance is comparable due to the low pass nature of a feedback system. Since the feedback signal energy is mostly in the control bandwidth, which is 1/100th to 1/10th of the sampling frequency, the quantization noise energy in the band is much lower than what the 12 bit adc word length implies. The selection of ADC is thus assumed to be mostly based on cost as long as the ADC has fast enough sample-and-hold amplifier front end.

Chapter 7

Conclusion

All of the converters were tested up to full nominal load of the 100 W guitar amplifier. All of the power supplies were over engineered for electrical and thermal performance. No thermal camera was available during the testing, but based on touch the LLC was not perceivably heating even with full load. The transformer core was slightly warm to touch but otherwise the heater supply is probably able to source several times higher current than rated. This is partly needed as the heater wire of the tube is much lower resistance than at operational temperature, thus the heater supply needs to supply 150-200 % of the nominal current during start up.

The dual active bridge was most difficult to get running without excessive heat rise. Since the transformer has very high ringin current riding in the primary and secondary, the transformer was wound with 0.1 mm stranded litz wire. Several tests were made and the final design was able to heat up only 25 degrees with full nominal amplifier load. The dhb is designed to supply up to 3 A peak load current, but thermally it needs to only withstand around 130 W of continuous load.

The PFC inductor was difficult to design due to the difficulty in procuring a proper core materia. Powder metal cores are mostly used as they have high saturation flux and offer high inductance to size ratio. The PFC inductor cores were constructed using stacked EF25 cores due to availability. RM8 and RM10 cores were considered but RM10 cores have roughly equal footprint as do the stacked EF25 cores, but have much smaller core window. The

RM8 was also considered, but the EF25 design offered around 20 % higher inductance, thus that design was chosen.

At the moment of writing all of the power stages have been tested to work and the thermal performance should be good enough to be able to be passively cooled. The highest heat rise of 30 degrees at full load was measured from the aluminum plate, which dissipates the heat from the PFC and DHB semiconductors. Assuming that the system was operated in a closed rack with 70 degree ambient temperature, there should still be thermal margin left even though the main power supply semiconductors would be operating at 100 degrees.

References

- Bist, V. and Singh, B. (2015), "Pfc cuk converter-fed bldc motor drive," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 871–887.
- Fairchild (2003), "Design guidelines for off-line flyback converters using fairchild power switch," Tech. Rep. MSU-CSE-06-2, Fairchild, URL <https://www.onsemi.com/pub/Collateral/AN-4137.pdf.pdf>.
- Fardoun, A.A., Ismail, E.H., Sabzali, A.J., and Al-Saffar, M.A. (2012), "New efficient bridgeless cuk rectifiers for pfc applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 7, pp. 3292–3301.
- Gusseme, K.D., de Sype, D.M.V., den Bossche, A.P.M.V., and Melkebeek, J.A. (2005), "Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 88–97.
- Jovanovic, M.M. and Jang, Y. (2005), "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications - an overview," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 701–708.
- Singh, B., Singh, B.N., Chandra, A., Al-Haddad, K., Pandey, A., and Kothari, D.P. (2003), "A review of single-phase improved power quality ac-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981.