REPORT

B12901022 廖冠豪

Registers for ALU

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
ready_reg	Flip-flop	1	N	N	Y	N	N	N	N
mul_on_reg	Flip-flop	1	N	N	N	N	N	N	N
div_on_reg	Flip-flop	1	N	N	N	N	N	N	N
out_data_reg	Flip-flop	64	Y	N	Y	N	N	N	N

Registers for MUL

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
tmp_B_reg	Flip-flop	32	Y	N	N	N	N	N	N
ready_reg	Flip-flop	1	N	N	Y	N	N	N	N
count_reg	Flip-flop	6	Y	N	Y	N	N	N	N
out_reg	Flip-flop	32	Y	N	Y	N	N	N	N
out_reg	Flip-flop	32	Y	N	N	N	N	N	N

Registers for DIV

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
over_reg	Flip-flop	1	N	N	N	N	N	N	N
div_reg	Flip-flop	32	Y	N	Y	N	N	N	N
count_reg	Flip-flop	6	Y	N	Y	N	N	N	N
ready_reg	Flip-flop	1	N	N	Y	N	N	N	N
rem_reg	Flip-flop	64	Y	N	Y	N	N	N	N