Released Notes

Rev. Code	Date	
1.0	2018-03-29	Author: Joe.Zhong Description: Draft
1.1	2018-06-05	Author: Joe.Zhong Description: 1. Remove R712, R713, R714, R715, R716, R717, R718, R719 2. Remove C611, C612, C68, C54 3. Remove R653, R652 4. Remove R302 5. Remove R610, R75 6. Remove R667 7. Remove C739, C740, C741 8. Remove R161 9. Remove R638, R144, R147, R148 10.Remove R112 11.Remove R629, R639 12.Remove R723 13.Remove C601, R33 14.Remove U509 15.Remove R632 16.Remove R108, R105, R98, R94, R109 17.Remove R304 18.Remove R5, R7 19.Connect PMIC_VSNVS and VSNVS_3V0 through a 0OHM resistor 20.Remove BT500, C590 21.Remove SW1 22.Remove D4 23.Remove R22 24.Remove R572, R571 25.Change the alias of pad G20 (EIM_D20) to GPIO3_IO20 All GOIO3_IO20s are changed to GPIO3_IO20, too. 26.Change the 5V_DC supply from MicroUSB(J513) to Connector (J514) Let GPIO5_IO09, GPIO5_IO10, GPIO5_IO11, GPIO5_IO12 and GPIO5_IO13 unconnected. Change J514.22, J514.24, J514.26, J514.28 and J514.30 to 5V_DC Delete J513 and let J501 to be DNP 27.CCC

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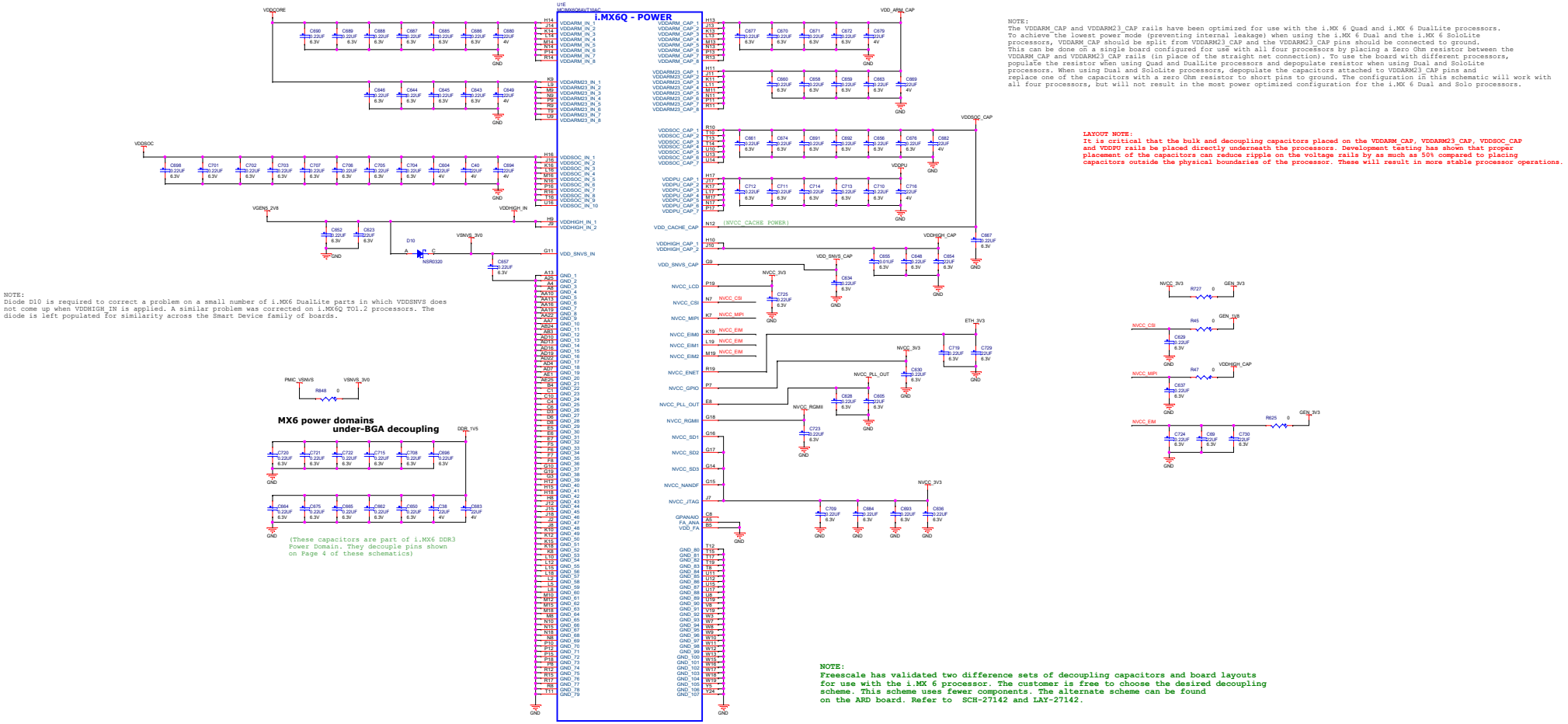

NOTE:
Diode D10 is required to correct a problem on a small number of i.MX6 DualLite parts in which VDDSNVS does not come up when VDDHIGH_IN is applied. A similar problem was corrected on i.MX6Q T01.2 processors. The diode is left populated for similarity across the Smart Device family of boards.

NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

NOTE:
Freescale has validated two difference sets of decoupling capacitors and board layouts for use with the i.MX 6 processor. The customer is free to choose the desired decoupling scheme. This scheme uses fewer components. The alternate scheme can be found on the ARD board. Refer to SCH-27142 and LAY-27142.

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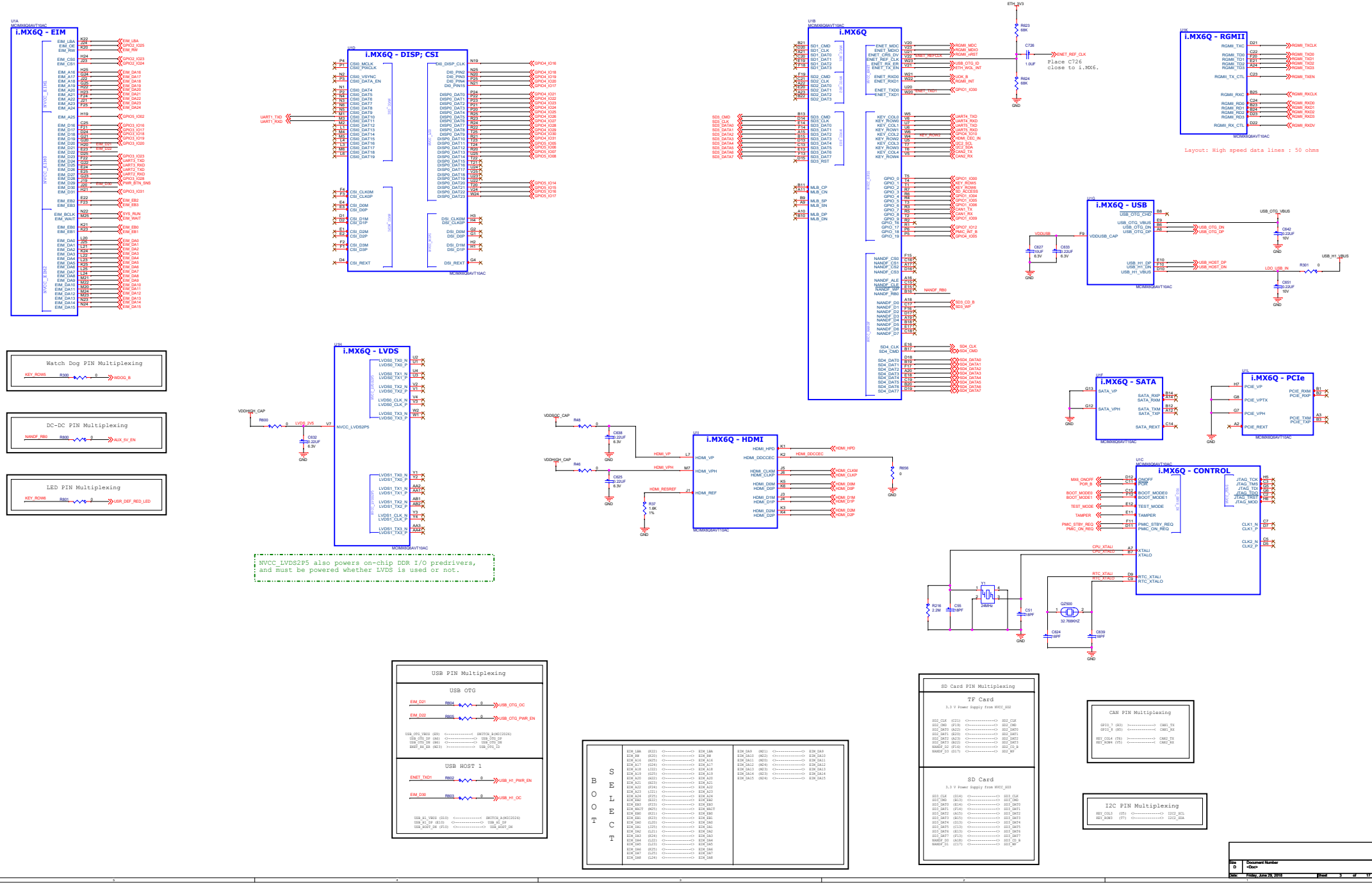
i.MX6Q - EIM
i.MX6Q - DISP; CSI
i.MX6Q
i.MX6Q - RGMII
i.MX6Q - USB
i.MX6Q - LVDS
i.MX6Q - HDMI
i.MX6Q - SATA
i.MX6Q - PCIe
i.MX6Q - CONTROL
Watch Dog PIN Multiplexing
KEY_ROW5
R300
WDOG_B
DC-DC PIN Multiplexing
NANDF_RB0
R800
AUX_5V_EN
LED PIN Multiplexing
KEY_ROW6
R801
USR_DEF_RED_LED
NVCC_LVDS2P5 also powers on-chip DDR I/O predrivers, and must be powered whether LVDS is used or not.
Layout: High speed data lines : 50 ohms
Place C726 close to i.MX6.
USB PIN Multiplexing
USB OTG
USB HOST 1
SD Card PIN Multiplexing
TF Card
SD Card
CAN PIN Multiplexing
I2C PIN Multiplexing
BOOT SELECT
Size D
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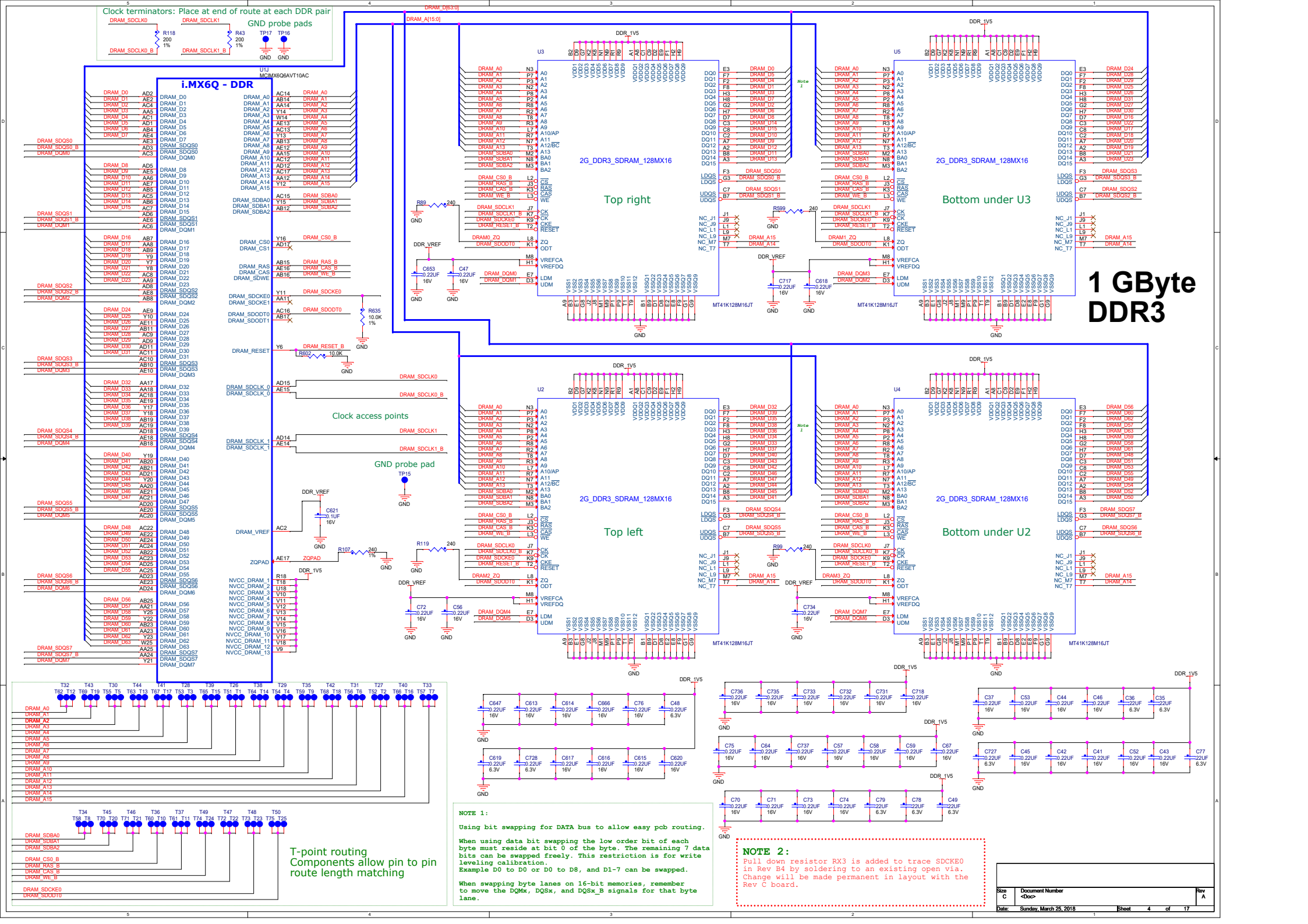
Clock terminators: Place at end of route at each DDR pair
GND probe pads
i.MX6Q - DDR
U1J
MCIMX6Q6AVT10AC
Top right
Bottom under U3
Top left
Bottom under U2
2G_DDR3_SDRAM_128MX16
MT41K128M16JT
1 GByte
DDR3
Clock access points
GND probe pad
T-point routing
Components allow pin to pin
route length matching
NOTE 1:
Using bit swapping for DATA bus to allow easy pcb routing.
When using data bit swapping the low order bit of each byte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write levelling calibration.
Example D0 to D0 or D0 to D8, and D1-7 can be swapped.
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.
NOTE 2:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.
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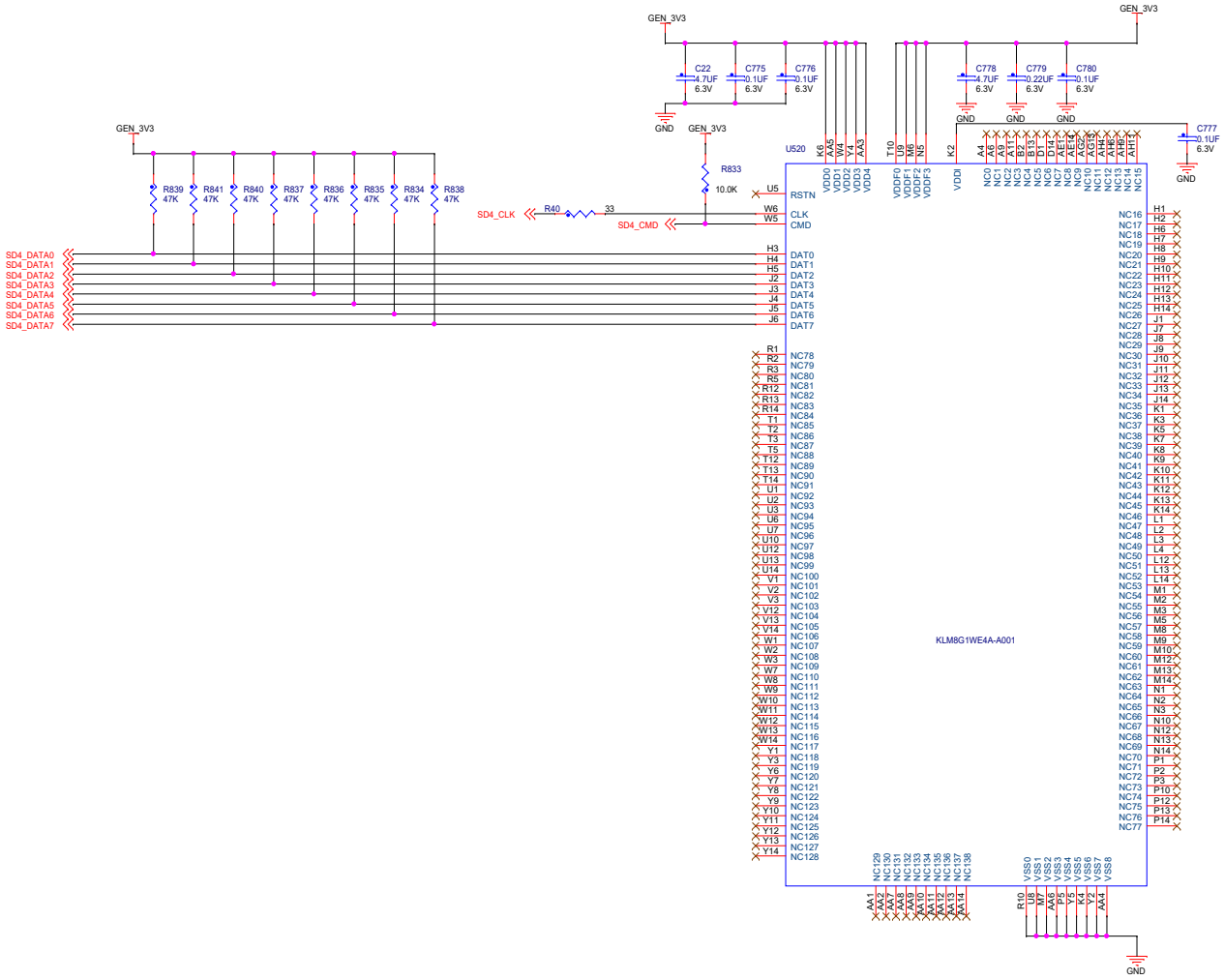
8GB eMMC MEMORY



Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

NOTE:
RST_B pin is not enabled by default. It must be turned on by software. Therefore, part with RST_B pin can be used in existing designs that do not connect this pin.

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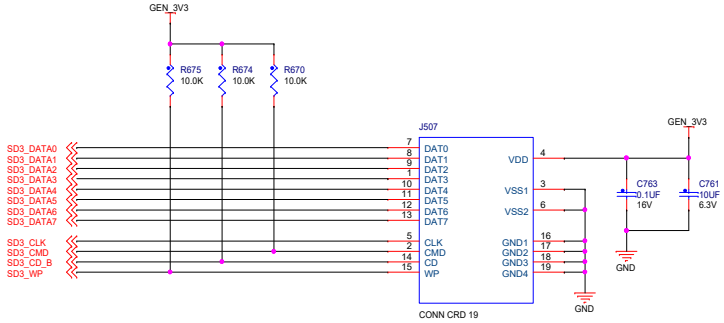
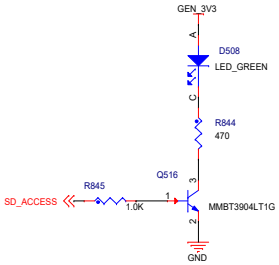
SD CARD SOCKET





Layout:
50ohm, SD signals(SD_DATAx, SD_CMD, SD_CLK) length equal

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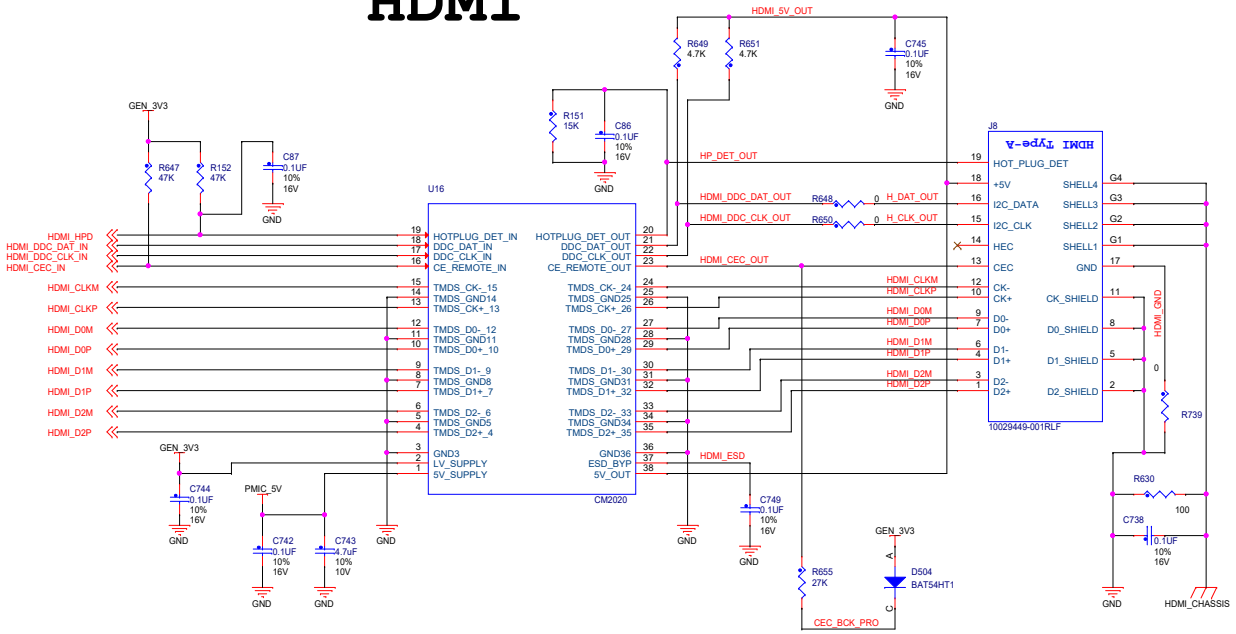
HDMI



Layout: HDMI 100 ohm differential pairs

NOTE:
When using HDMI, I2C2 bus is limited to 100 kHz
to read EDID values due to HDMI standards.
I2C2 bus speed should be limited to 100 kHz whenever
Hot Plug Detect is high.

LVDS Connector notes:
Pin 1: This pin is the Display Enable pin. It is used to
Enable/Disable the HannStar display.
Pin 5: This pin is the Display Brightness control. It
provides a PWM signal to the display to increase/
decrease display brightness depending on PWM
duty cycle. This signal is shared by all displays, so all
displays will change brightness together.

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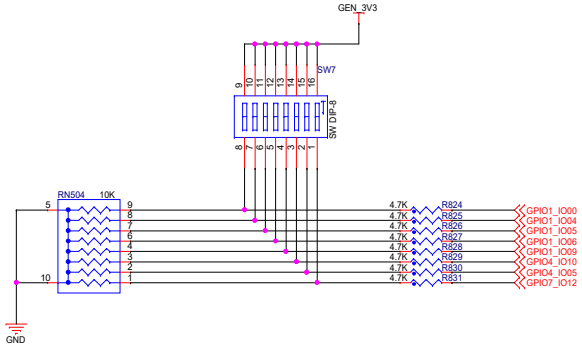

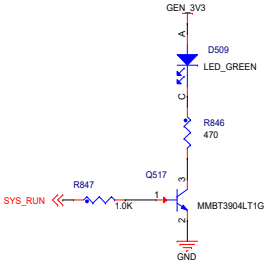

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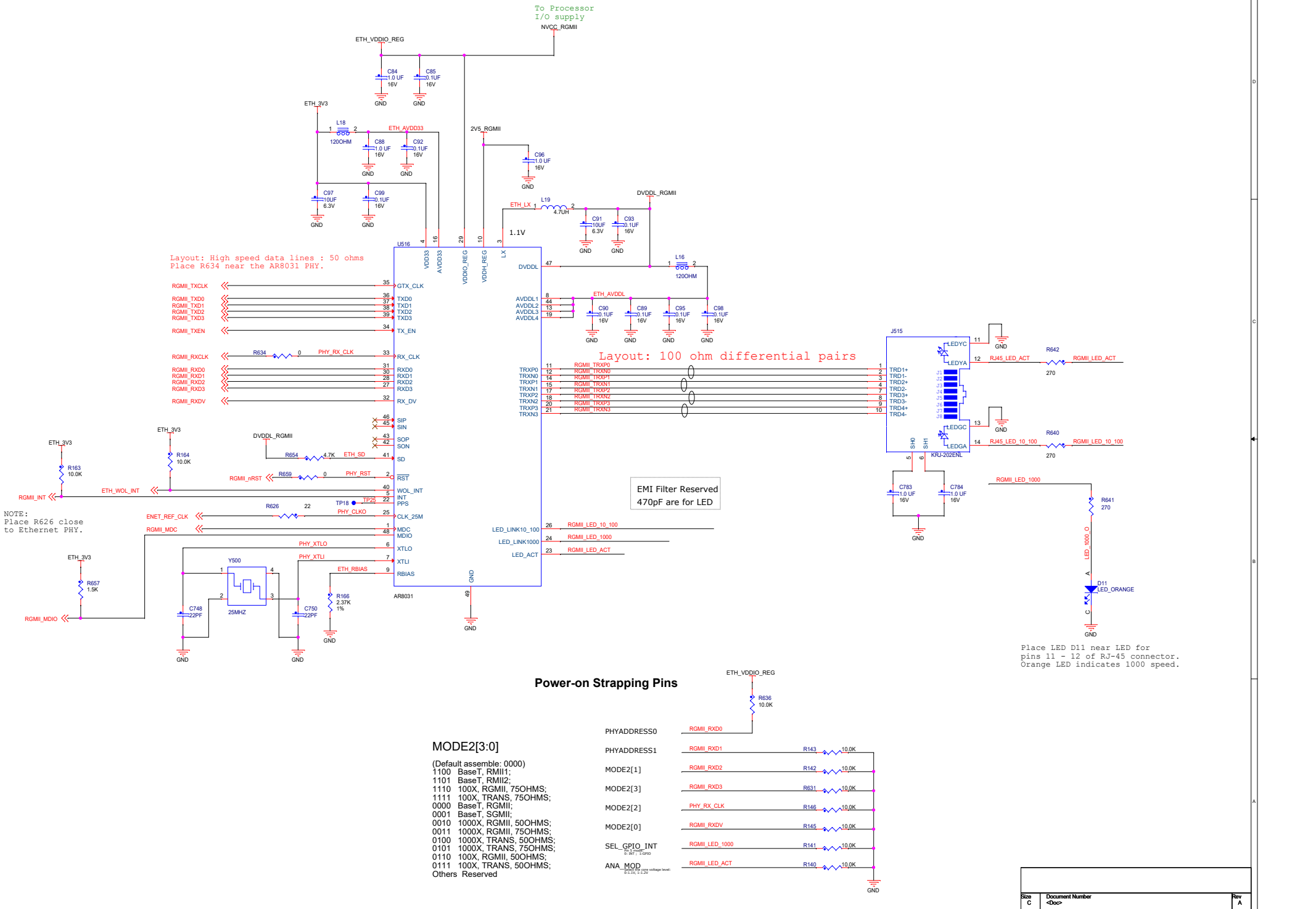
To Processor
I/O supply
NVCC_RGMII
ETH_VDDIO_REG
C84 1.0 UF 16V
C85 0.1UF 16V
ETH_3V3
L18 120OHM
ETH_AVDD33
C88 1.0 UF 16V
C92 0.1UF 16V
2V5_RGMII
C96 1.0 UF 16V
C97 10UF 6.3V
C99 0.1UF 16V
ETH_LX
L19 4.7UH
DVDDL_RGMII
C91 10UF 6.3V
C93 0.1UF 16V
1.1V
U516
VDD33
AVDD33
VDDIO_REG
VDDH_REG
LX
DVDDL
L16 120OHM
AVDDL1
AVDDL2
AVDDL3
AVDDL4
ETH_AVDDL
C90 0.1UF 16V
C89 0.1UF 16V
C95 0.1UF 16V
C98 0.1UF 16V
Layout: High speed data lines : 50 ohms
Place R634 near the AR8031 PHY.
RGMII_TXCLK
RGMII_TXD0
RGMII_TXD1
RGMII_TXD2
RGMII_TXD3
RGMII_TXEN
GTX_CLK
TXD0
TXD1
TXD2
TXD3
TX_EN
RGMII_RXCLK
R634 0
PHY_RX_CLK
RX_CLK
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
RGMII_RXDV
RXD0
RXD1
RXD2
RXD3
RX_DV
SIP
SIN
SOP
SON
SD
RST
WOL_INT
INT
PPS
CLK_25M
MDC
MDIO
XTLO
XTLI
RBIAS
AR8031
GND
Layout: 100 ohm differential pairs
TRXP0
TRXN0
TRXP1
TRXN1
TRXP2
TRXN2
TRXP3
TRXN3
RGMII_TRXP0
RGMII_TRXN0
RGMII_TRXP1
RGMII_TRXN1
RGMII_TRXP2
RGMII_TRXN2
RGMII_TRXP3
RGMII_TRXN3
J515
TRD1+
TRD1-
TRD2+
TRD2-
TRD3+
TRD3-
TRD4+
TRD4-
LEDYC
LEDYA
LEDGC
LEDGA
SH0
SH1
KRJ-202ENL
RJ45_LED_ACT
RJ45_LED_10_100
R642 270
R640 270
RGMII_LED_ACT
RGMII_LED_10_100
C783 1.0 UF 16V
C784 1.0 UF 16V
RGMII_LED_1000
R641 270
LED_1000_O
D11 LED_ORANGE
ETH_3V3
R163 10.0K
R164 10.0K
RGMII_INT
ETH_WOL_INT
DVDDL_RGMII
R654 4.7K
ETH_SD
RGMII_nRST
R659 0
PHY_RST
TP18
TP25
R626 22
PHY_CLKO
ENET_REF_CLK
RGMII_MDC
RGMII_MDIO
R657 1.5K
PHY_XTLO
PHY_XTLI
ETH_RBIAS
Y500
25MHZ
C748 22PF
C750 22PF
R166 2.37K 1%
LED_LINK10_100
LED_LINK1000
LED_ACT
EMI Filter Reserved
470pF are for LED
NOTE:
Place R626 close
to Ethernet PHY.
Place LED D11 near LED for
pins 11 - 12 of RJ-45 connector.
Orange LED indicates 1000 speed.
Power-on Strapping Pins
ETH_VDDIO_REG
R636 10.0K
PHYADDRESS0
PHYADDRESS1
MODE2[1]
MODE2[3]
MODE2[2]
MODE2[0]
SEL_GPIO_INT
ANA_MOD
RGMII_RXD0
RGMII_RXD1
RGMII_RXD2
RGMII_RXD3
PHY_RX_CLK
RGMII_RXDV
RGMII_LED_1000
RGMII_LED_ACT
R143 10.0K
R142 10.0K
R631 10.0K
R146 10.0K
R145 10.0K
R141 10.0K
R140 10.0K
MODE2[3:0]
(Default assemble: 0000)
1100 BaseT, RMII1;
1101 BaseT, RMII2;
1110 100X, RGMII, 75OHMS;
1111 100X, TRANS, 75OHMS;
0000 BaseT, RGMII;
0001 BaseT, SGMII;
0010 1000X, RGMII, 50OHMS;
0011 1000X, RGMII, 75OHMS;
0100 1000X, TRANS, 50OHMS;
0101 1000X, TRANS, 75OHMS;
0110 100X, RGMII, 50OHMS;
0111 100X, TRANS, 50OHMS;
Others Reserved
Size C
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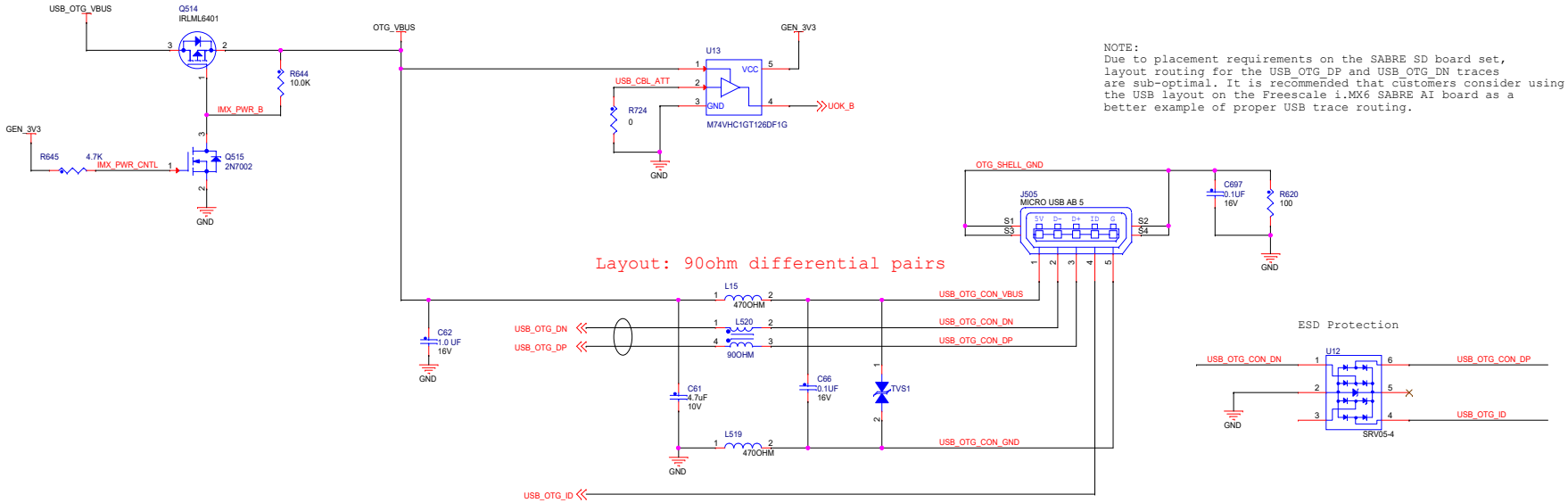

NOTEs:

1. R103 populated in A position to prevent USB_5V path to battery charge ICs when no batteries are attached. To enable charging batteries from USB, move resistor from Position A to Position B.

TRUTH TABLE

OTG VBUS INPUT TO BATTERY CHARGERS

USB_OTG _PWR_EN	OTG_PWR _ON	OTG_PWR _ON_B	OTG_VBUS _CHGR
LOW	HIGH	LOW	POWERED
HIGH	LOW	HIGH	NOT POWERED

NOTE:
On all three pad resistor options, resistors are to be initially populated on pads 1 - 2 (Option A). Users may move resistors from their default locations as needed.

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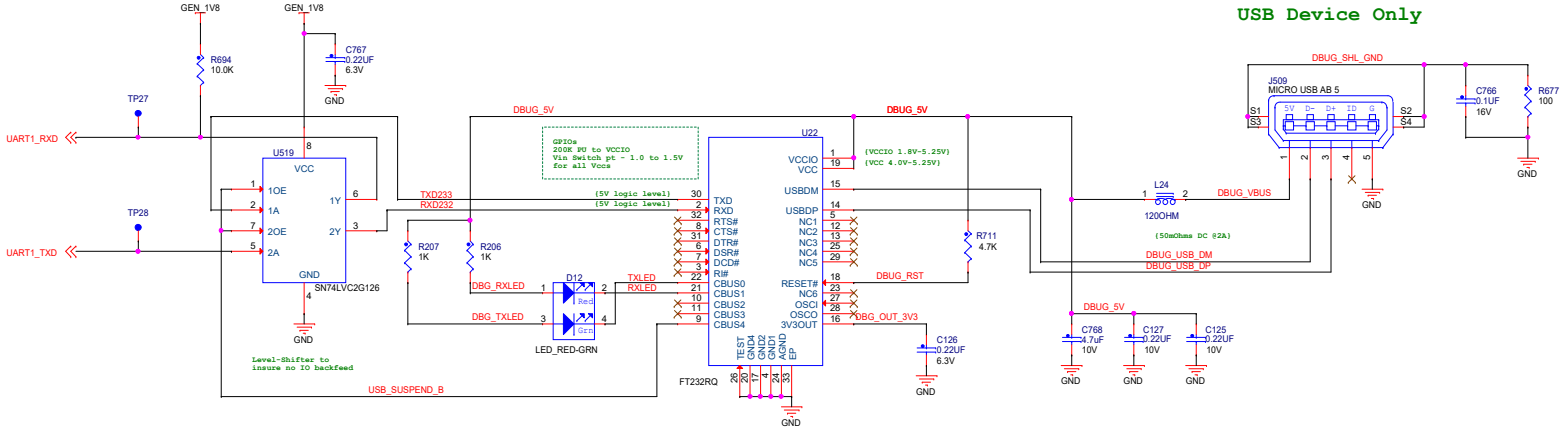
DEBUG UART TO USB CONVERSION

Library Revision - A



USB Device Only

Drivers located at:
http://www.ftdichip.com/Products/ICs/FT232R.htm

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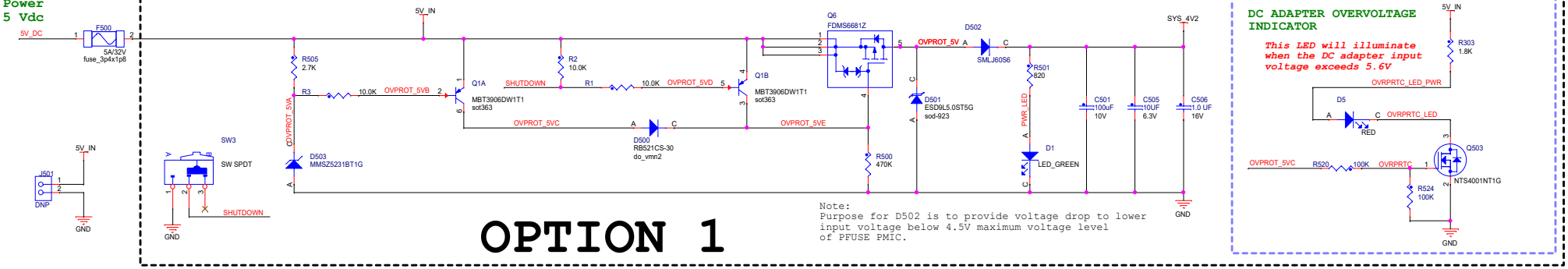
OVER VOLTAGE PROTECTION

External Power 5 Vdc



Note:
Purpose for D502 is to provide voltage drop to lower input voltage below 4.5V maximum voltage level of PFUSE PMIC.

OPTION 1

DC ADAPTER OVERVOLTAGE INDICATOR

This LED will illuminate when the DC adapter input voltage exceeds 5.6V

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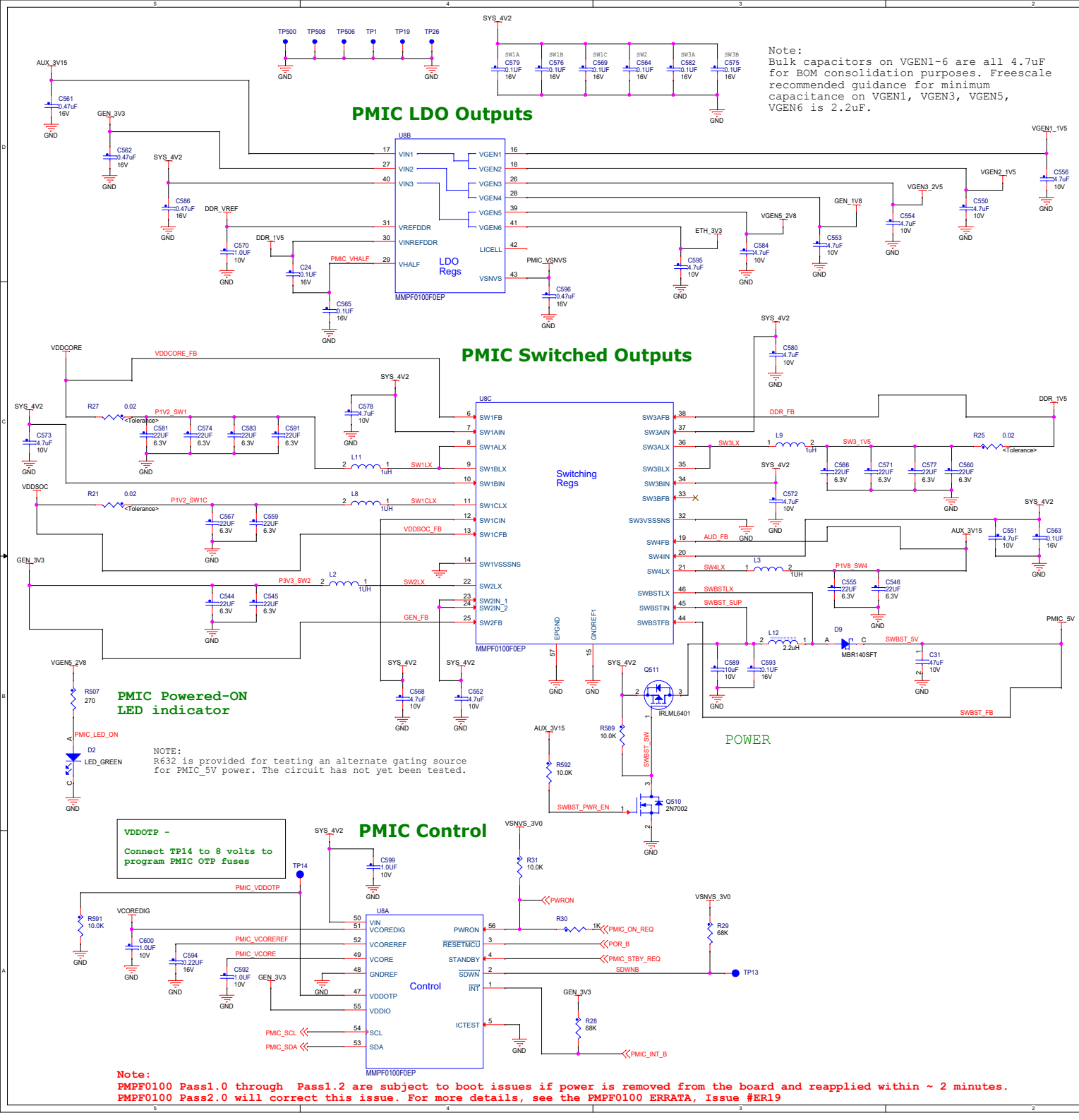

Typical Power Requirements

	Voltage	Power Up Sequence	Current Drawn (mA)	SYS 4V2 Current (mA)	NOTES
SW1A	1.375	1	2155	1001	
SW1B					
SW1C	1.375	2	1590	739	
SW2	3.3	5	653	728	
SW3A	1.5	3	1500	760	
SW3B					
SW4	3.15	6	200	213	
SWBST	5.0	13	300	507	
VGEN1	1.5	9	100	0	Supplied from SW4
VGEN2	1.5	10	250	0	Supplied from SW4
VGEN3	2.8	11	70	66	
VGEN4	1.8	12	310	189	
VGEN5	2.8	10	75	71	See Note on Page 20
VGEN6	3.3	8	160	178	
VSNVS	3.0	0	0.2	0	
VREFDDR	0.75	3	10	3	
Total System Current Requirements:			4454		

SYSTEM POWER RAILS

Voltge	Rail Name	Block	Generated By	Current Capability (mA)	NOTES
5.0	PMIC_5V	USB	PF0100 SWBST	600	
		LVDS1			
		HDMI			
	AUX_5V	SATA	MAX8815	1000	
		LVDS0			
		CAN			
3.3	GEN_3V3	EMMC	PF0100 SW2	2000	NVCC_LCD NVCC_EIM0/1/2 NVCC_GPIO NVCC_SD2/3 NVCC_NANDF NAND_JTAG
		SD3			
		NOR			
		SATA			
		LVDS			
		HDMI			
		MIPI			
		mPCIe			
		SENSORS			
	VGEN6_3V3	ETH	PF0100 VGEN6	200	NVCC_ENET
3.15	AUX_3V15	EXP HDR	PF0100 SW4	1000	Supplies: VGEN1 VGEN2
		TOUCH			
		GPS			
2.8	VDDHIGH_IN	IMX6	PF0100 VGEN5	100	
	VGEN3_2V5	CAMERA	PF0100 VGEN3	100	
2.5	GEN_2V5	SATA	IMX6 VDDHIGH_CAP	TBD	NVCC_MIPI
		HDMI			
		MIPI			
		mPCIe			
1.8	GEN_1V8	AUDIO	PF0100 VGEN4	350	NVCC_SD1 NVCC_CSI
		CAMERA			
		ACC			
1.5	VGEN2_1V5	CAMERA	PF0100VGEN2	250	
	VGEN1_1V5	GPS	PF0100 VGEN1	100	
		mPCIe			
	DDR_1V5	DDR	PF0100 SW3A/B	2500	
1.375	VDDCORE	ARMCORE	PF0100 SW1A/B	2500	
	VDDSOC	VDDSOC	PF0100 SW1C	1750	
0.75	VREFDDR	DDR	PF0100 VREFDDR	10	

Note:
To turn off board "AUTO ON" feature, depopulate R30 and R31, and populate U509. This feature has not yet been tested.

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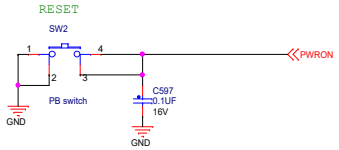
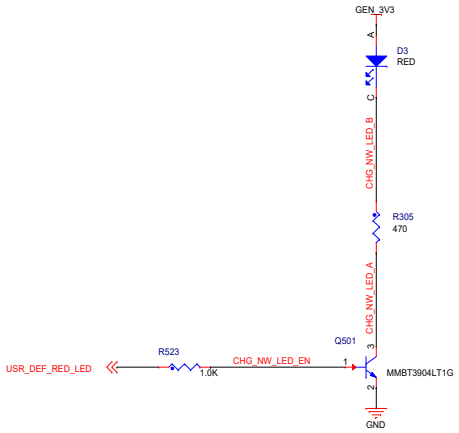
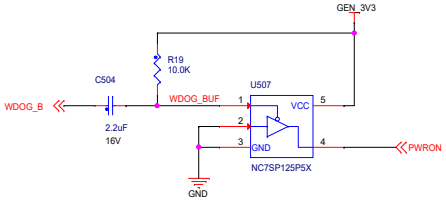
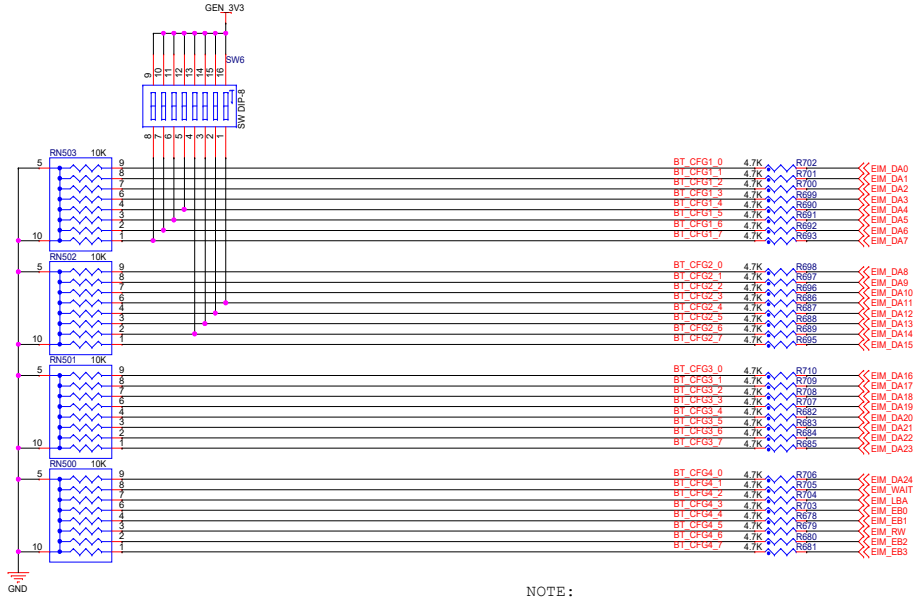


NOTE:
On Rev B4 and later designs, the RESET button is connected directly to the PWRON input of the PMIC. This will cause a complete board reset (Processor & PMIC) when the RESET button is pressed.





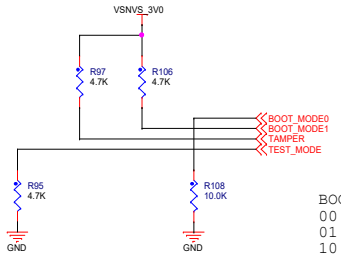
Boot Configuration Select



NOTE:
Place series resistors so as to minimize EIM portion of trace length. Two layout possibilites include:
1) As close to processor as possbile.
2) Close to other componets using EIM signals.

Boot Select Table

8	7	6	5	4	3	2	1
BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG2_6	BT_CFG2_5	BT_CFG2_4	BT_CFG2_3
011X = MMC/eMMC Boot				X0 = 1-bit X1 = 4-bit 10 = 8-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
010X = SD/eSD Boot				X0 = 1-bit X1 = 4-bit		01 = SD2 Boot 10 = SD3 Boot 11 = SD4 Boot	
0010 = SATA Boot				X	X	X	0



BOOT MODES:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

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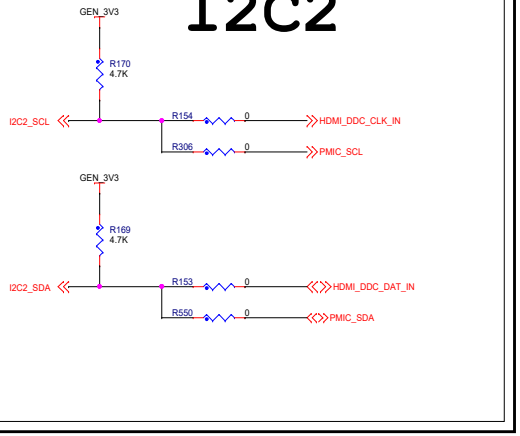
I2C2



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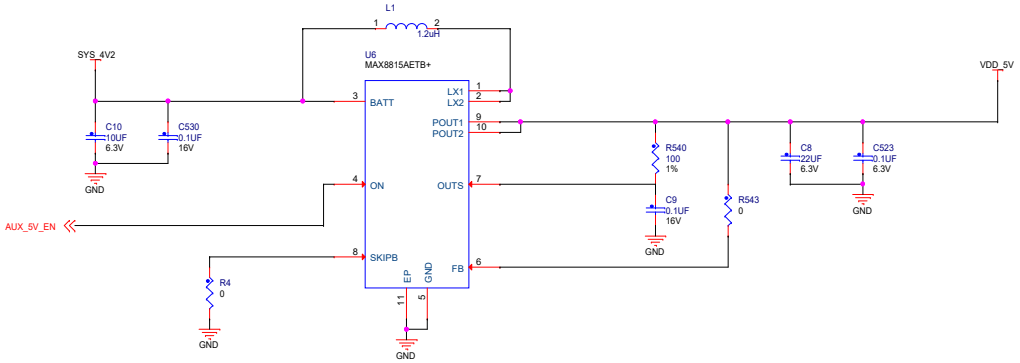
5.0V@1A DC2DC



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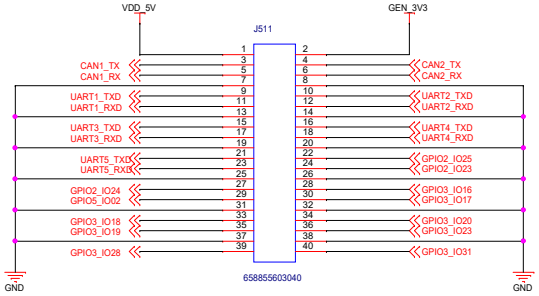

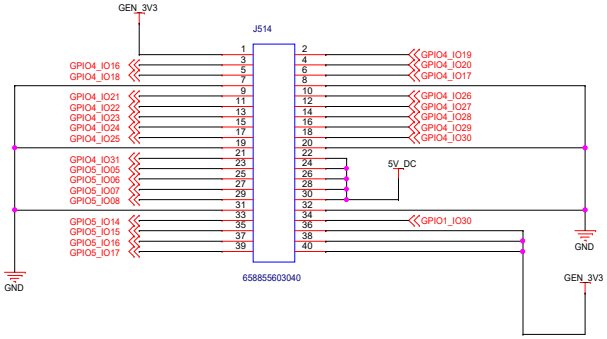

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