Chapter 1

Reversible Computing

In thus chapter we introduce basics of Reversible logic, Reversible gates and Reversible circuit.

1.1 Reversible Logic

A function is reversible if it is bijective. In other words in a reversible function the number of inputs must be equal to the number of outputs and there is a one-to-one mapping between its input and output vectors. A reversible gate realizes a reversible function. For example Table 1 represents a truth table of a particular reversible function with three inputs (i1, i2, i3) and three outputs (o1, o2, o3). Here the number of input variables and the number of output variables are the same. From the truth table, it can be seen that for any two input vectors, the corresponding output vectors are different. Similarly for any two output vectors the corresponding input vectors are different. A conventional 2-input AND gate (see the truth table in Table)is not considered to be reversible because it has two input variables but only output variable and for three different input vectors(00, 01, 10) output vector is the same(i.e., 0) which is not allowed in reversible logic. Other conventional logic gates such as OR, NAND, NOR, X-OR are also not reversible. The only exception is NOT gate which is reversible.

1.2 Reversible Gates

Reversible circuits are built from a set of reversible logic gates since conventional logic gates other than NOT gate are not applicable in reversible logic. A reversible logic gate is an n-input n-output logic device with one-to-one mapping so that the outputs can be determined from the inputs as well as

the inputs can be uniquely recovered from the outputs. Some of the basic logic gates are discussed below.

1.2.1 CNOT gate

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as: I (A, B); O(P= A, Q= A XOR B), I and O are input and output vectors respectively. Figure below shows a 2*2 CNOT gate and its symbol along with truth table.

Figure 1.1: A CNOT gate

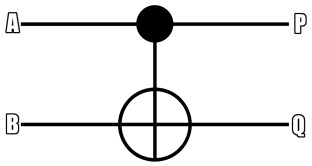


Table 1.1: Truth Table of CNOT Gate

Input		Output	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

1.2.2 TOFFOLI Gate

A 3*3 Toffoli gate along with truth table is shown in figure. The input vector is I (A, B, C) and the output vector is O(P, Q, R). The outputs are defined by P=A, Q=B, R=AB XOR C.

Figure 1.2: A TOFFOLI gate

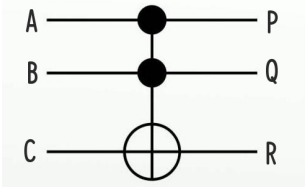


Table 1.2: Truth Table of Toffoli Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

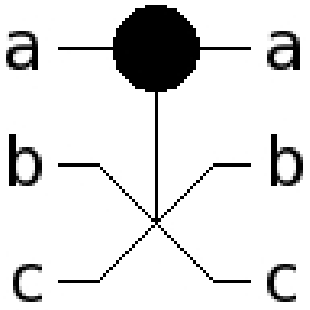
1.2.3 Fredkin Gate

Figure below shows a 3*3 Fredkin gate along with truth table. The input vector is I (a, b, c) and the output vector is O (a, b, c). The output is defined by a=a, b=a'b XOR ac and c=a'c XOR ac.

Table 1.3: Fredkin Gate Truth Table

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 1.3: A FREDKIN gate



1.2.4 Peres Gate

Fig shows a 3*3 Peres gate along with its truth table. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A XOR B and R=AB XOR C.

Figure 1.4: A PERES gate

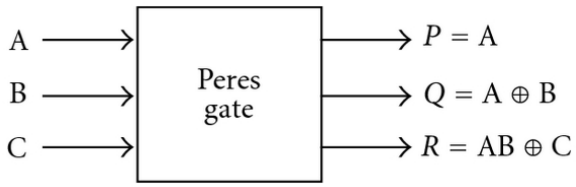


Figure 1.5: Peres gate equivalent

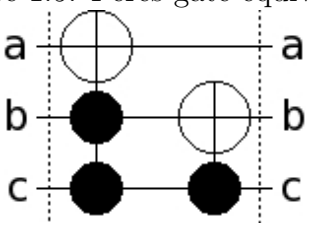


Table 1.4: Peres Gate Truth Table

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

1.3 Reversible Circuit

A reversible circuit consists of only reversible gates which are interconnected without any fan-out or feedback. The term fan-out refers to the maximum number of inputs that can be driven from one output of a gate. In a reversible circuit the fan-out of a gate is at most one. A reversible circuit is represented by network of wires that carry bit values to gate that perform elementary operations on the bits. The wires are referred to as bit lines. The input bits are written on the left side of the circuit and the output bits are written on the right side of the circuit. The circuit is acyclic i.e., it is linear and time in circuit propagates from left to right. At every time step each wire can enter at most one gate. If a reversible circuit is built using only Toffoli gates including NOT gates, CNOT gates and negative control Toffoli gates, it is known as a Toffoli circuit. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility

1.4 Conventional Circuit Vs Reversible Circuit

Reversible circuits unavoidably generate heat because of losses of information during the computation. In contrast to conventional gates reversible logic gates have same number of inputs and outputs. Unlike conventional circuits feedback and fan-out concept is not allowed in reversible circuits. Moreover, logic design of reversible circuit is quite different from that of conventional irreversible logic circuits. For realization of non-balanced Boolean functions by a reversible circuit it is necessary to apply constant signals to some inputs of the circuit whereas in conventional circuits with complex gates using constant signals is useful but not necessary.