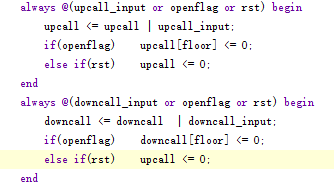
[Synth 8-327] inferring latch for variable 'height\_reg' ["C:/Users/jojo/Desktop/Elevator/StatusTransition.v":43]



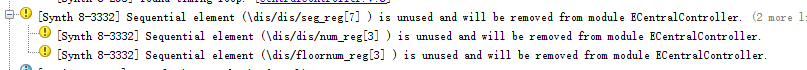
这种if… if else 分支判断 若掉了一个分支即掉了一种情况会出现这种warinning

这种赋值语句还可能造成muti driven

有关referenced signal should be on a sensitivity list

[When must a signal be inserted into the sensitivity list of a process](https://stackoverflow.com/questions/8991223/when-must-a-signal-be-inserted-into-the-sensitivity-list-of-a-process)

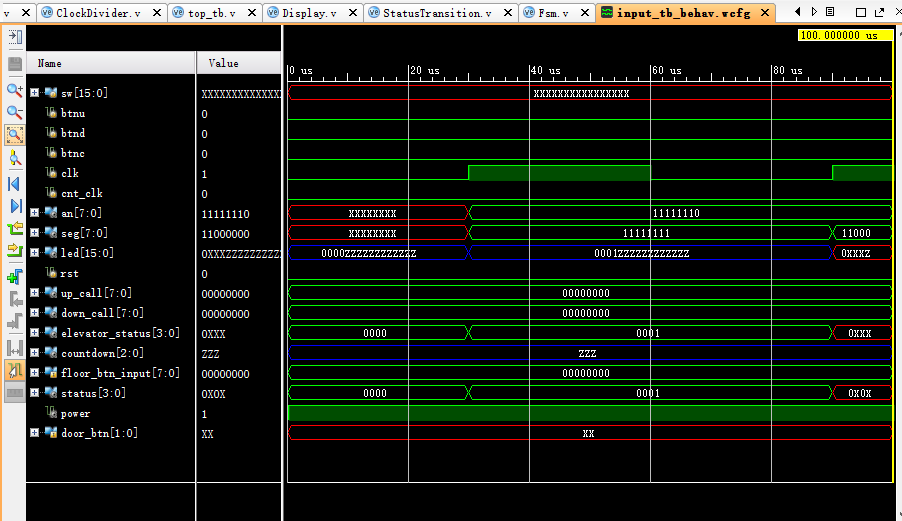
<https://stackoverflow.com/questions/8991223/when-must-a-signal-be-inserted-into-the-sensitivity-list-of-a-process>

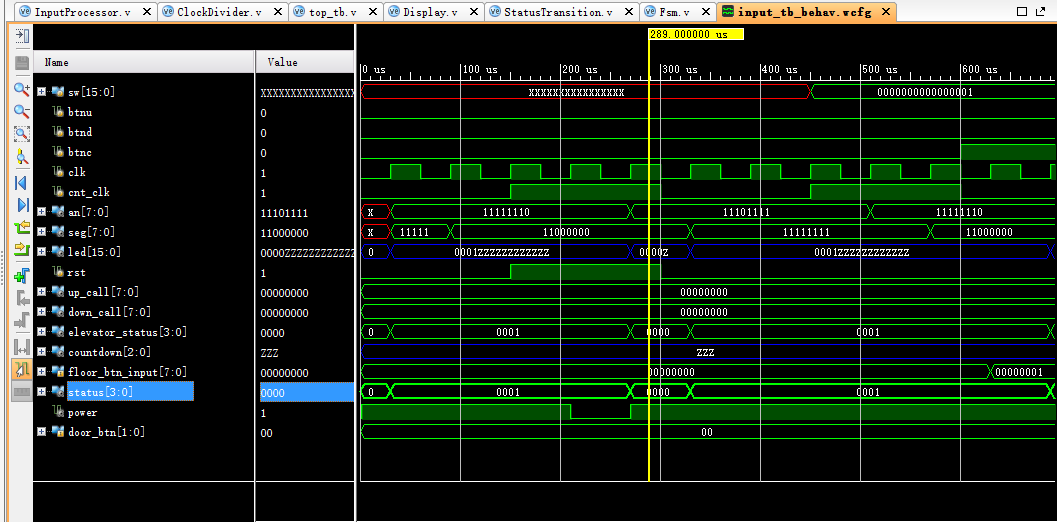


原因在于vivado发现了你的某一寄存器始终存储定值，于是决定其可以优化掉

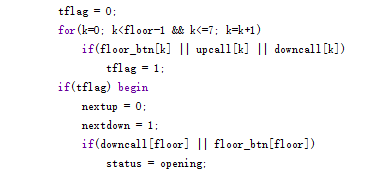
在后仿真的过程中发现状态机的status走一段之后就会到XXX状态，十分令人费解

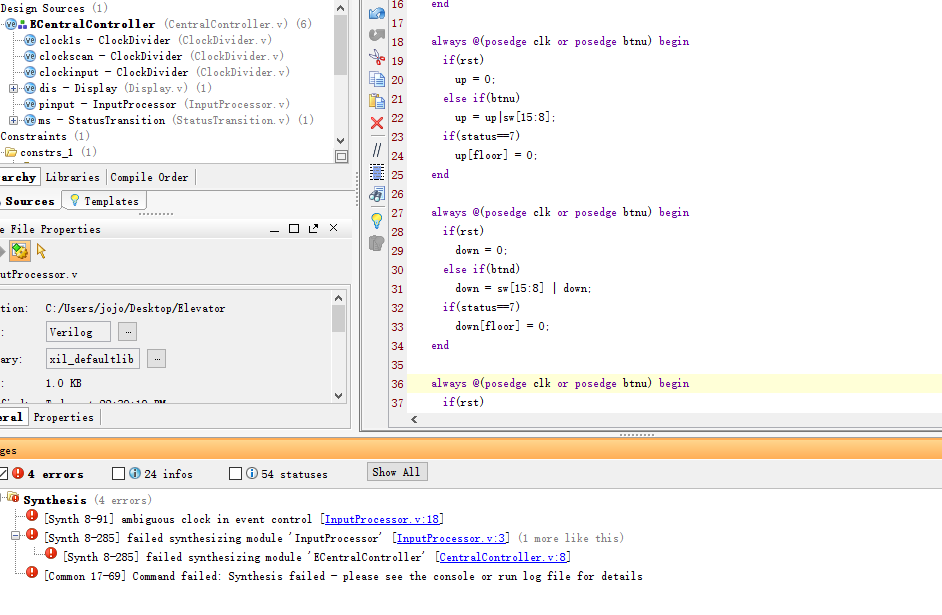
仔细分析之后觉得可能时决定状态转换的分支变量出现了不确定的XXX值，这样导致status值最终为XXX，如下俩图的情况





溢出惨案：





<https://forums.xilinx.com/t5/7-Series-FPGAs/Synth-8-91-ambiguous-clock-in-event-control/td-p/676245>

