

СОДЕРЖАНИЕ

Введение.....	3
1 Изучение работы шины AXI	4
1.1 Симуляция программы общего варианта.....	4
1.2 Симуляция программы индивидуального варианта.....	6
2 Сборка проекта.....	8
3 Запуск программного обеспечения на хост-системе	9
Заключение.....	10
Ответы на контрольные вопросы	11
Приложение А Содержимое файла host_example.cpp	14
Приложение Б Содержимое xclbin.info-файла	23
Приложение В Содержимое log-файла	28

ВВЕДЕНИЕ

Ускорителями вычислений принято называть специальные аппаратные устройства, способные выполнять ограниченный ряд задач с большей параллельностью и за меньшее время в сравнении с универсальными микропроцессорными ЭВМ . Как правило, ускоритель представляет собой структуру, включающую большое количество примитивных микропроцессорных устройств, объединенных шинами связей.

В настоящее время применение ускорителей вычислений охватывает ряд важных областей: финансовые вычисления, ускорение запросов к базам данных, машинное обучение, видео-аналитика. В ряде случаев удается достичь ускорения более чем в 90 раз по сравнению с универсальными ЭВМ, построенными на микропроцессорах Intel x86.

Цель работы: изучение архитектуры гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx. Для достижения данной цели необходимо выполнить следующие задачи:

- изучить основные сведения о платформе Xilinx Alveo U200;
- разработать RTL описание ускорителя вычислений по индивидуальному варианту;
- выполнить генерацию ядра ускорителя;
- выполнить синтез и сборку бинарного модуля ускорителя;
- разработать и отладить тестирующее программное обеспечение на серверной хост-платформе;
- провести тесты работы ускорителя вычислений.

Все задания выполняются в соответствии с вариантом №4.

1 Изучение работы шины AXI

В данном разделе приведены диаграммы, иллюстрирующие процесс рукопожатия и пакетного чтения.

1.1 Симуляция программы общего варианта

Каналы позволяют сформировать конвейерные транзакции чтения и записи. Последовательность событий транзакции чтения можно представить следующим образом: ARVALID -> ARREADY -> RVALID -> RREADY. На рисунке 1.1 приведена транзакция чтения данных вектора на шине AXI4 MM из DDR памяти.

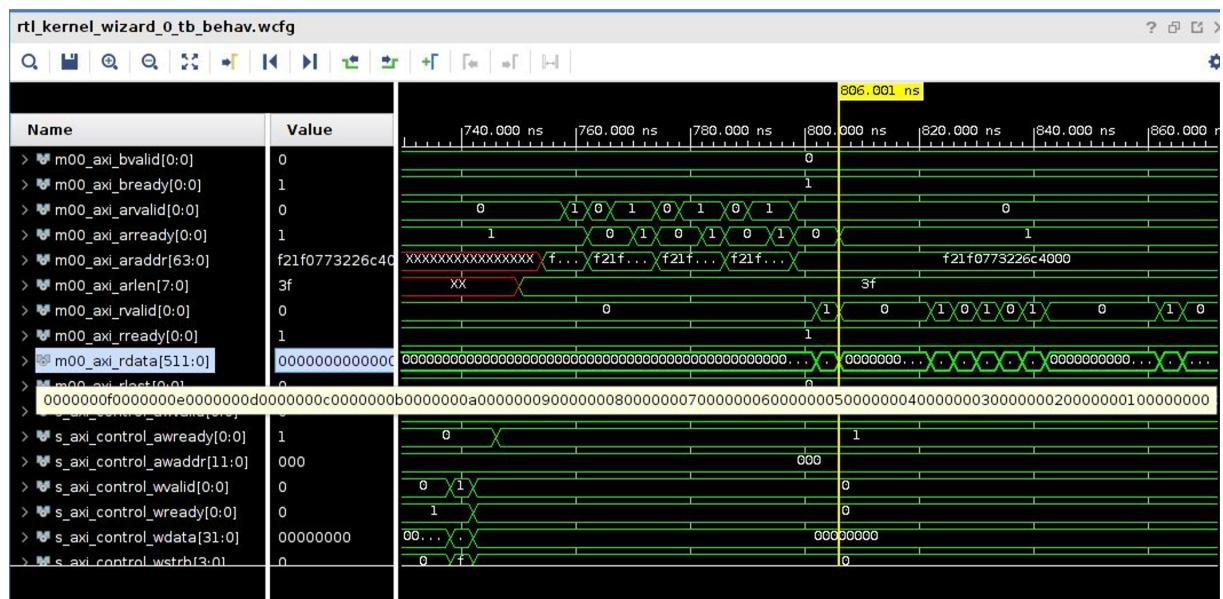


Рисунок 1.1 – Транзакция чтения данных вектора на шине AXI4 MM из DDR памяти

Последовательность событий транзакции записи: AWVALID → AWREADY → WVALID → WREADY → BVALID → BREADY. На рисунке 1.2 приведена транзакция записи результата инкремента данных на шине AXI4 MM.

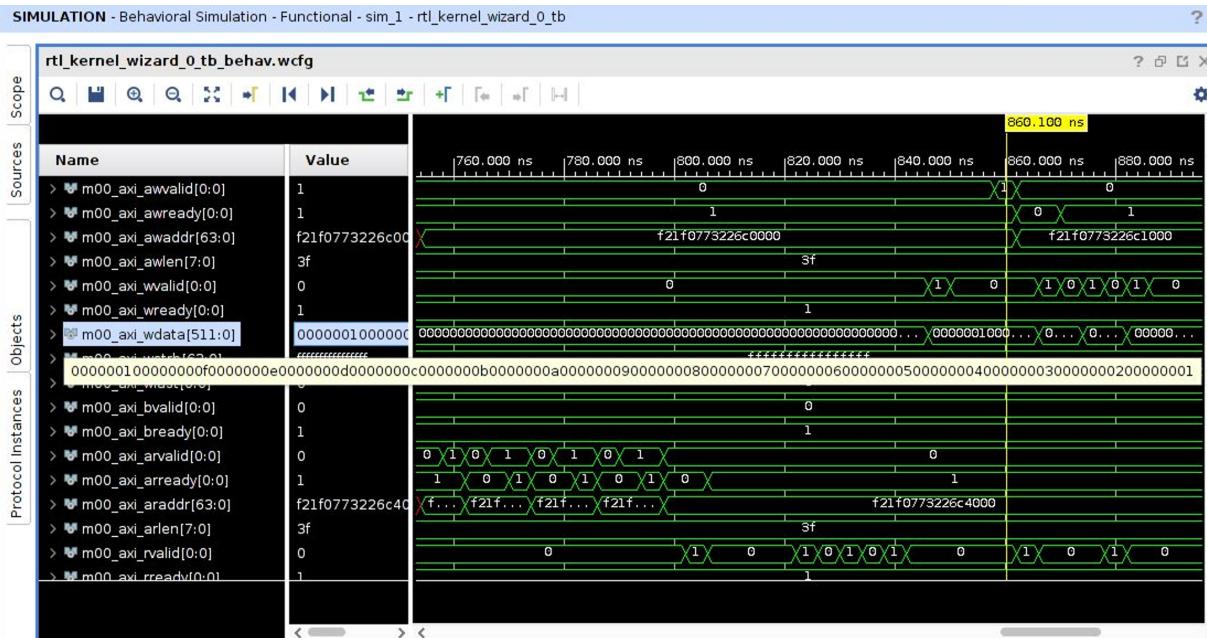


Рисунок 1.2 — Транзакция записи результата инкремента данных на шине AXI4 MM

На рисунке 1.3 приведен инкремент данных.

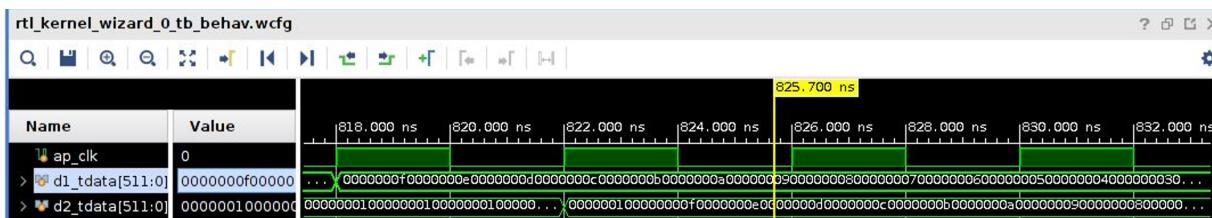


Рисунок 1.3 — Инкремент данных в модуле

1.2 Симуляция программы индивидуального варианта

Теперь изменим модуль так, чтобы ускоритель выполнял функцию из индивидуального задания. Сделанные изменения отражены в листинге B.1.

Листинг 1.1 — Модифицированная функция

```
1 always @(* posedge s_axis_aclk ) begin
2     for ( i=0; i<LP_NUM_LOOPS; i=i+1) begin
3         d2_tdata [ i *C_ADDER_BIT_WIDTH+:C_ADDER_BIT_WIDTH] <=
4             (d1_tdata [C_ADDER_BIT_WIDTH*i+:C_ADDER_BIT_WIDTH] > 61680 ?
5              d1_tdata [C_ADDER_BIT_WIDTH*i+:C_ADDER_BIT_WIDTH] : 61680) + 1;
6     end
7 end
```

На рисунке 1.4 приведена транзакция чтения данных вектора на шине AXI4 MM из DDR памяти.

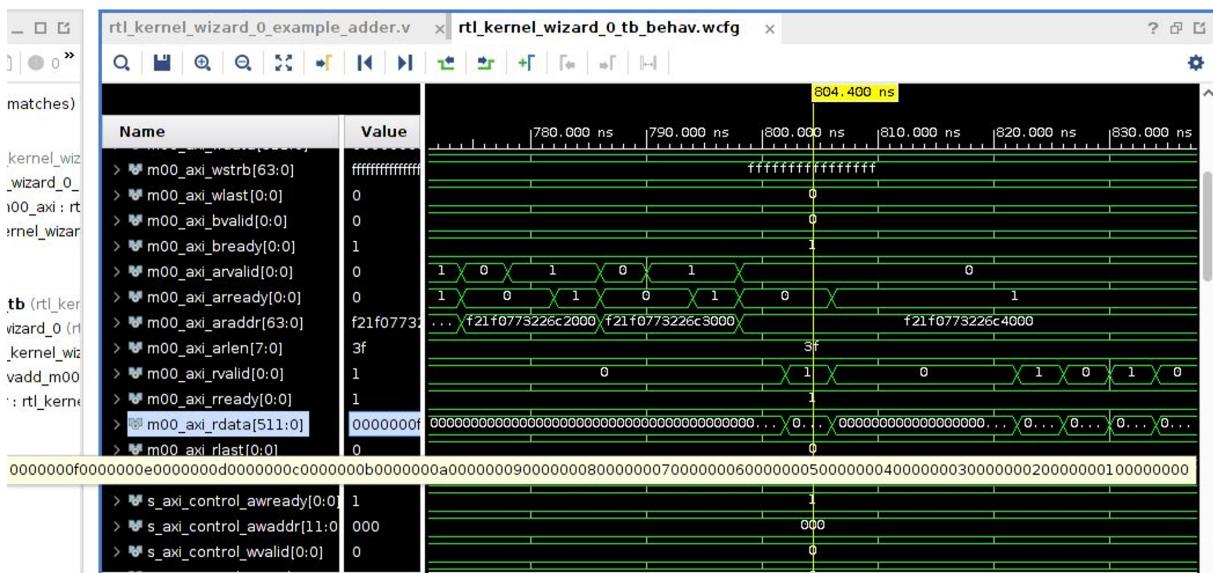


Рисунок 1.4 — Транзакция чтения данных вектора на шине AXI4 MM из DDR памяти

На рисунке 1.5 приведена транзакция записи результата инкремента данных на шине AXI4 MM.



Рисунок 1.5 – Транзакция записи результата инкремента данных нашине AXI4 MM

На рисунке 1.6 приведен инкремент данных.



Рисунок 1.6 – Инкремент данных в модуле

2 Сборка проекта

В листинге 2.1 приведено содержимое конфигурационного файла. В соответствии с вариантом требовалось использовать регионы SLR2, DDR[3].

Листинг 2.1 — Содержимое файла конфигурации.

```
1 [connectivity]
2 nk=rtl_kernel_wizard_0:1:vinc0
3
4 slr=vinc0:SLR2
5
6 sp=vinc0.m00_axi:DDR[3]
7 sp=vinc0.m00_axi:PLRAM[0]
8
9 [vivado]
10 prop=run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore
11 prop=run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore
12 prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true
13 prop=run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=AggressiveExplore
14 prop=run.impl_1.STEPS.ROUTE_DESIGN.ARGS.DIRECTIVE=Explore
```

Содержимое файлов v++*.log и *.xclbin.info. приведено в приложениях Б и В.

3 Запуск программного обеспечения на хост-системе

В листинге 3.1 приведена измененная части файла host_example.cpp. Всё содержимое файла приведено в приложении А.

Листинг 3.1 — Модуль host_example.cpp

```
1 // Check Results
2
3 for (cl_uint i = 0; i < number_of_words; i++) {
4     unsigned res = (h_data[i] > 61680 ? h_data[i] : 61680) + 1;
5     if (res != h_axi00_ptr0_output[i]) {
6         printf("ERROR in rtl_kernel_wizard_0::m00_axi - array index %d
7             (host addr 0x%03x) - input=%d (0x%0x), output=%d (0x%0x)\n",
8             i, i*4, h_data[i], h_data[i], h_axi00_ptr0_output[i],
9             h_axi00_ptr0_output[i]);
10        check_status = 1;
11    }
12    // printf("i=%d, input=%d, output=%d\n", i, h_axi00_ptr0_input[i],
13    // h_axi00_ptr0_output[i]);
14 }
```

Для отладки и проверки работоспособности была использована утилита xgdb. На рисунке 3.1 приведены результаты тестирования.

```
For help, type "help".
Type "apropos word" to search for commands related to "word"...
Reading symbols from rtl_kernel_wizard_0_host_example.exe...
(gdb) run
Starting program: /iu_home/lu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/rtl_kernel_wizard_0_host_example.exe vinc.xclbin
[Thread debugging using libthread_db enabled]
Using host libthread_db library "/lib/x86_64-linux-gnu/libthread_db.so.1".
[New Thread 0x7ffff5b2f700 (LWP 46875)]
INFO: Found 1 platforms
INFO: Selected platform 0 from Xilinx
INFO: Found 1 devices
CL_DEVICE_NAME xilinx_v200_xdma_201830_2
Selected xilinx_v200_xdma_201830_2 as the target device
INFO: loading xclbin vinc.xclbin
[New Thread 0x7ffff4f2d700 (LWP 46946)]
[New Thread 0x7ffffeff700 (LWP 46948)]
[New Thread 0x7ffffef7fe700 (LWP 46953)]
[New Thread 0x7ffffefffd700 (LWP 46956)]
[New Thread 0x7ffffefffc700 (LWP 46959)]
[New Thread 0x7ffffedfffb700 (LWP 46960)]
INFO: Test completed successfully.
[Thread 0x7ffff4f2d700 (LWP 46946) exited]
[Thread 0x7ffff5b2f700 (LWP 46875) exited]
[Thread 0x7ffffefffd700 (LWP 46956) exited]
[Thread 0x7ffffefffb700 (LWP 46960) exited]
[Thread 0x7ffffefffc700 (LWP 46959) exited]
[Thread 0x7ffffeff7fe700 (LWP 46953) exited]
[Thread 0x7ffffeff700 (LWP 46948) exited]
[Inferior 1 (process 46806) exited normally]
(gdb) []
```

Рисунок 3.1 — Результаты тестирования

ЗАКЛЮЧЕНИЕ

В ходе данной работы были изучены архитектура гетерогенных вычислительных систем и технологии разработки ускорителей вычислений на базе ПЛИС фирмы Xilinx. Была выполнена генерация ядра ускорителя с последующими синтезом, сборкой и тестированием бинарного модуля ускорителя.

ОТВЕТЫ НА КОНТРОЛЬНЫЕ ВОПРОСЫ

1. Преимущества и недостатки XDMA и QDMA платформ

Недостатки использовани XDMA:

1. Большая латентность и меньшая пропускная способность за счет того, что данные сначала должны быть перемещены в память ускорителя.

Преимущества использования QDMA:

1. Предоставляет прямое потоковое соединение с низкой задержкой и большой пропускной способностью между хостом и ядрами;
2. Позволяет передавать поток данных непосредственно в логику FPGA параллельно с их обработкой.

2. Последовательность действий, необходимых для инициализации ускорителя со стороны хост-системы

1. С помощью вызова `clGetPlatformIDs` хост получает все платформы.
2. С помощью вызова `clGetPlatformInfo` хост получает имя платформы и затем выбирает платформу Xilinx.
3. С помощью вызова `clGetDeviceIDs` хост получает ID устройства.
4. С помощью вызова `clGetDeviceInfo` хост получает информацию об устройстве.
5. С помощью вызова `clCreateContext` создается контекст для переменных.
6. С помощью вызова `clCreateCommandQueue` создается команда для устройства-ускорителя.

3. Процедура запуска задания на исполнения в ускорительном ядре VINC

1. С помощью вызова `load_file_to_memory` данные, бинарный поток (данные из *.xclbin), копируются из ОЗУ в локальную память ускорителя посредством DMA.
2. По итогу выполнения `clCreateProgramWithBinary`, `clBuildProgram` и `clCreateKernel` создается исполняемый файл (уже в памяти устройства-ускорителя).
3. С помощью `clCreateBuffer` и `clEnqueueWriteBuffer` данные, подлежащие обработке, копируются из ОЗУ в локальную память ускорителя посредством DMA (с помощью второй команды осуществляется передача указателей на начало буферов исходных operandов).
4. С помощью двух вызовов `clSetKernelArg` указываются параметры (в данном случае это `d_scalar00` и `d_axi00_ptr0`).
5. С помощью команды `clEnqueueNDRangeKernel` запускается исполнение ядра (программы на ускорителе).
6. С помощью команды `clEnqueueReadBuffer` выполняется чтение готовых данных.

4. Процесс линковки на основании содержимого log-файла

Процесс сборки состоит из шести этапов.

1. Анализ конфигурационного файла, анализ профиля устройства, поиск необходимых аппаратных компонентов, интерфейсов;
2. FPGA линковка синтезированных ядер с платформой;
3. FPGA оптимизация логики (минимизация логики (булевой) для оптимизации площади, минимизации задержек);
4. FPGA logic placement (Преобразование булевых уравнений в схему логики ПЛИС. Выбор конкретного места для каждого логического блока в ПЛИС);
5. FPGA разводка (создание соединений между логическими блоками);

6. FPGA генерирование файла с программной информацией для отправки его на ПЛИС (*.xclbin файл);

ПРИЛОЖЕНИЕ А

СОДЕРЖИМОЕ ФАЙЛА HOST_EXAMPLE.CPP

Листинг А.1 — Содержимое файла host_example.cpp

```
1 // This is a generated file. Use and modify at your own risk.  
2 //  
3 ///////////////////////////////////////////////////////////////////  
4 /*****  
5 Vendor: Xilinx  
6 Associated Filename: main.c  
7 #Purpose: This example shows a basic vector add +1 (constant) by  
     manipulating  
8 #           memory inplace.  
9 *****/  
10  
11 #include <fcntl.h>  
12 #include <stdio.h>  
13 #include <iostream>  
14 #include <stdlib.h>  
15 #include <string.h>  
16 #include <math.h>  
17 #ifdef _WINDOWS  
18 #include <io.h>  
19 #else  
20 #include <unistd.h>  
21 #include <sys/time.h>  
22 #endif  
23 #include <assert.h>  
24 #include <stdbool.h>  
25 #include <sys/types.h>  
26 #include <sys/stat.h>  
27 #include <CL/opencl.h>  
28 #include <CL/cl_ext.h>  
29 #include "xclhal2.h"  
30  
31 //  
32 ///////////////////////////////////////////////////////////////////  
33 #define NUM_WORKGROUPS (1)  
34 #define WORKGROUP_SIZE (256)
```

```

35 #define MAX_LENGTH 8192
36 #define MEM_ALIGNMENT 4096
37 #if defined(VITIS_PLATFORM) && !defined(TARGET_DEVICE)
38 #define STR_VALUE(arg)      #arg
39 #define GET_STRING(name)  STR_VALUE(name)
40 #define TARGET_DEVICE GET_STRING(VITIS_PLATFORM)
41 #endif
42
43 ///////////////////////////////////////////////////////////////////
44
45 cl_uint load_file_to_memory(const char *filename, char **result)
46 {
47     cl_uint size = 0;
48     FILE *f = fopen(filename, "rb");
49     if (f == NULL) {
50         *result = NULL;
51         return -1; // -1 means file opening fail
52     }
53     fseek(f, 0, SEEK_END);
54     size = ftell(f);
55     fseek(f, 0, SEEK_SET);
56     *result = (char *)malloc(size+1);
57     if (size != fread(*result, sizeof(char), size, f)) {
58         free(*result);
59         return -2; // -2 means file reading fail
60     }
61     fclose(f);
62     (*result)[size] = 0;
63     return size;
64 }
65
66 int main(int argc, char** argv)
67 {
68
69     cl_int err;                                // error code returned from api
70     calls
71     cl_uint check_status = 0;
72     const cl_uint number_of_words = 4096; // 16KB of data
73
74     cl_platform_id platform_id;                // platform id
75     cl_device_id device_id;                   // compute device id
76     cl_context context;                      // compute context
77     cl_command_queue commands;               // compute command queue

```

```

78 cl_program program; // compute programs
79 cl_kernel kernel; // compute kernel
80
81 cl_uint* h_data; // host memory for
82 // input vector
82 char cl_platform_vendor[1001];
83 char target_device_name[1001] = TARGET_DEVICE;
84
85 cl_uint* h_axi00_ptr0_output = (cl_uint*)aligned_alloc(MEM_ALIGNMENT,
86 MAX_LENGTH * sizeof(cl_uint*)); // host memory for output vector
86 cl_mem d_axi00_ptr0; // device memory used for
87 // a vector
88
88 if (argc != 2) {
89     printf("Usage: %s xclbin\n", argv[0]);
90     return EXIT_FAILURE;
91 }
92
93 // Fill our data sets with pattern
94 h_data = (cl_uint*)aligned_alloc(MEM_ALIGNMENT,MAX_LENGTH * sizeof(
95 cl_uint*));
95 for (cl_uint i = 0; i < MAX_LENGTH; i++) {
96     h_data[i] = i;
97     h_axi00_ptr0_output[i] = 0;
98
99 }
100
101 // Get all platforms and then select Xilinx platform
102 cl_platform_id platforms[16]; // platform id
103 cl_uint platform_count;
104 cl_uint platform_found = 0;
105 err = clGetPlatformIDs(16, platforms, &platform_count);
106 if (err != CL_SUCCESS) {
107     printf("ERROR: Failed to find an OpenCL platform!\n");
108     printf("ERROR: Test failed\n");
109     return EXIT_FAILURE;
110 }
111 printf("INFO: Found %d platforms\n", platform_count);
112
113 // Find Xilinx Platform
114 for (cl_uint iplat=0; iplat<platform_count; iplat++) {
115     err = clGetPlatformInfo(platforms[iplat], CL_PLATFORM_VENDOR, 1000,
116     (void *)cl_platform_vendor, NULL);
117     if (err != CL_SUCCESS) {
118         printf("ERROR: clGetPlatformInfo(CL_PLATFORM_VENDOR) failed!\n"
119             );

```

```

118     printf("ERROR: Test failed\n");
119     return EXIT_FAILURE;
120 }
121 if (strcmp(cl_platform_vendor, "Xilinx") == 0) {
122     printf("INFO: Selected platform %d from %s\n", iplat,
123           cl_platform_vendor);
124     platform_id = platforms[iplat];
125     platform_found = 1;
126 }
127 if (!platform_found) {
128     printf("ERROR: Platform Xilinx not found. Exit.\n");
129     return EXIT_FAILURE;
130 }
131
132 // Get Accelerator compute device
133 cl_uint num_devices;
134 cl_uint device_found = 0;
135 cl_device_id devices[16]; // compute device id
136 char cl_device_name[1001];
137 err = clGetDeviceIDs(platform_id, CL_DEVICE_TYPE_ACCELERATOR, 16,
138                      devices, &num_devices);
139 printf("INFO: Found %d devices\n", num_devices);
140 if (err != CL_SUCCESS) {
141     printf("ERROR: Failed to create a device group!\n");
142     printf("ERROR: Test failed\n");
143     return -1;
144 }
145
146 //iterate all devices to select the target device.
147 for (cl_uint i=0; i<num_devices; i++) {
148     err = clGetDeviceInfo(devices[i], CL_DEVICE_NAME, 1024,
149                           cl_device_name, 0);
150     if (err != CL_SUCCESS) {
151         printf("ERROR: Failed to get device name for device %d!\n", i);
152         printf("ERROR: Test failed\n");
153         return EXIT_FAILURE;
154     }
155     printf("CL_DEVICE_NAME %s\n", cl_device_name);
156     if (strcmp(cl_device_name, target_device_name) == 0) {
157         device_id = devices[i];
158         device_found = 1;
159         printf("Selected %s as the target device\n", cl_device_name);
160     }

```

```

161 if (!device_found) {
162     printf("ERROR: Target device %s not found. Exit.\n",
163            target_device_name);
164     return EXIT_FAILURE;
165 }
166 // Create a compute context
167 //
168 context = clCreateContext(0, 1, &device_id, NULL, NULL, &err);
169 if (!context) {
170     printf("ERROR: Failed to create a compute context!\n");
171     printf("ERROR: Test failed\n");
172     return EXIT_FAILURE;
173 }
174 //
175 // Create a command commands
176 commands = clCreateCommandQueue(context, device_id,
177                                 CL_QUEUE_PROFILING_ENABLE | CL_QUEUE_OUT_OF_ORDER_EXEC_MODE_ENABLE,
178                                 &err);
179 if (!commands) {
180     printf("ERROR: Failed to create a command commands!\n");
181     printf("ERROR: code %i\n", err);
182     printf("ERROR: Test failed\n");
183     return EXIT_FAILURE;
184 }
185 cl_int status;
186 //
187 // Create Program Objects
188 // Load binary from disk
189 unsigned char *kernelbinary;
190 char *xclbin = argv[1];
191 //
192 // xclbin
193 //
194 printf("INFO: loading xclbin %s\n", xclbin);
195 cl_uint n_i0 = load_file_to_memory(xclbin, (char **) &kernelbinary);
196 if (n_i0 < 0) {
197     printf("ERROR: failed to load kernel from xclbin: %s\n", xclbin);
198     printf("ERROR: Test failed\n");
199     return EXIT_FAILURE;

```

```

200    }
201
202    size_t n0 = n_i0;
203
204    // Create the compute program from offline
205    program = clCreateProgramWithBinary(context, 1, &device_id, &n0,
206                                         (const unsigned char **) &
207                                         kernelbinary, &status, &err);
208
209    free(kernelbinary);
210
211    if ((!program) || (err != CL_SUCCESS)) {
212        printf("ERROR: Failed to create compute program from binary %d!\n",
213               err);
214        printf("ERROR: Test failed\n");
215        return EXIT_FAILURE;
216    }
217
218    // Build the program executable
219    //
220    err = clBuildProgram(program, 0, NULL, NULL, NULL, NULL);
221    if (err != CL_SUCCESS) {
222        size_t len;
223        char buffer[2048];
224
225        printf("ERROR: Failed to build program executable!\n");
226        clGetProgramBuildInfo(program, device_id, CL_PROGRAM_BUILD_LOG,
227                               sizeof(buffer), buffer, &len);
228        printf("%s\n", buffer);
229        printf("ERROR: Test failed\n");
230        return EXIT_FAILURE;
231    }
232
233    // Create the compute kernel in the program we wish to run
234    //
235    kernel = clCreateKernel(program, "rtl_kernel_wizard_0", &err);
236    if (!kernel || err != CL_SUCCESS) {
237        printf("ERROR: Failed to create compute kernel!\n");
238        printf("ERROR: Test failed\n");
239        return EXIT_FAILURE;
240    }
241
242    // Create structs to define memory bank mapping
243    cl_mem_ext_ptr_t mem_ext;
244    mem_ext.obj = NULL;
245    mem_ext.param = kernel;

```

```

243
244
245     mem_ext.flags = 1;
246     d_axi00_ptr0 = clCreateBuffer(context, CL_MEM_READ_WRITE |
247                                     CL_MEM_EXT_PTR_XILINX, sizeof(cl_uint) * number_of_words, &mem_ext,
248                                     &err);
249     if (err != CL_SUCCESS) {
250         std::cout << "Return code for clCreateBuffer flags=" << mem_ext.flags
251             << ":" << err << std::endl;
252     }
253
254     if (!(d_axi00_ptr0)) {
255         printf("ERROR: Failed to allocate device memory!\n");
256         printf("ERROR: Test failed\n");
257         return EXIT_FAILURE;
258     }
259
260     err = clEnqueueWriteBuffer(commands, d_axi00_ptr0, CL_TRUE, 0, sizeof(
261                                     cl_uint) * number_of_words, h_data, 0, NULL, NULL);
262     if (err != CL_SUCCESS) {
263         printf("ERROR: Failed to write to source array h_data: d_axi00_ptr0
264             : %d!\n", err);
265         printf("ERROR: Test failed\n");
266         return EXIT_FAILURE;
267     }
268
269     // Set the arguments to our compute kernel
270     // cl_uint vector_length = MAX_LENGTH;
271     err = 0;
272     cl_uint d_scalar00 = 0;
273     err |= clSetKernelArg(kernel, 0, sizeof(cl_uint), &d_scalar00); // Not
274     // used in example RTL logic.
275     err |= clSetKernelArg(kernel, 1, sizeof(cl_mem), &d_axi00_ptr0);
276
277     if (err != CL_SUCCESS) {
278         printf("ERROR: Failed to set kernel arguments! %d\n", err);
279         printf("ERROR: Test failed\n");
280         return EXIT_FAILURE;
281     }
282
283     size_t global[1];
284     size_t local[1];
285     // Execute the kernel over the entire range of our 1d input data set

```

```

283 // using the maximum number of work group items for this device
284
285 global[0] = 1;
286 local[0] = 1;
287 err = clEnqueueNDRangeKernel(commands, kernel, 1, NULL, (size_t*)&
288     global, (size_t*)&local, 0, NULL, NULL);
289 if (err) {
290     printf("ERROR: Failed to execute kernel! %d\n", err);
291     printf("ERROR: Test failed\n");
292     return EXIT_FAILURE;
293 }
294
295
296
297 // Read back the results from the device to verify the output
298 //
299 cl_event readevent;
300
301 err = 0;
302 err |= clEnqueueReadBuffer( commands, d_axi00_ptr0, CL_TRUE, 0, sizeof(
303     cl_uint) * number_of_words, h_axi00_ptr0_output, 0, NULL, &readevent
304 );
305
306
307 if (err != CL_SUCCESS) {
308     printf("ERROR: Failed to read output array! %d\n", err);
309     printf("ERROR: Test failed\n");
310     return EXIT_FAILURE;
311 }
312
313 for (cl_uint i = 0; i < number_of_words; i++) {
314     unsigned res = (h_data[i] > 61680 ? h_data[i] : 61680) + 1;
315     if (res != h_axi00_ptr0_output[i]) {
316         printf("ERROR in rtl_kernel_wizard_0::m00_axi - array index %d
317             (host addr 0x%03x) - input=%d (0x%0x), output=%d (0x%0x)\n", i
318             , i * 4, h_data[i], h_data[i], h_axi00_ptr0_output[i],
319             h_axi00_ptr0_output[i]);
320         check_status = 1;
321     }
322     // printf("i=%d, input=%d, output=%d\n", i, h_axi00_ptr0_input[i],
323     // h_axi00_ptr0_output[i]);
324 }
325

```

```
322 //  
323 //  
  
324 // Shutdown and cleanup  
325 //  
  
326 clReleaseMemObject( d_axi00_ptr0 );  
327 free( h_axi00_ptr0_output );  
328  
329  
330  
331 free( h_data );  
332 clReleaseProgram( program );  
333 clReleaseKernel( kernel );  
334 clReleaseCommandQueue( commands );  
335 clReleaseContext( context );  
336  
337 if (check_status) {  
338     printf( "ERROR: Test failed\n" );  
339     return EXIT_FAILURE;  
340 } else {  
341     printf( "INFO: Test completed successfully.\n" );  
342     return EXIT_SUCCESS;  
343 }  
344  
345  
346 } // end of main
```

ПРИЛОЖЕНИЕ Б

СОДЕРЖИМОЕ XCLBIN.INFO-ФАЙЛА

Листинг Б.1 — Содержимое vinc.xclbin.info файла.

```
1  
2 XRT Build Version: 2.8.743 (2020.2)  
3     Build Date: 2020-11-16 00:19:11  
4         Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9  
5  
6 xclbin Information  
7  
8     Generated by:           v++ (2020.2) on 2020-11-18-05:13:29  
9     Version:                2.8.743  
10    Kernels:                 rtl_kernel_wizard_0  
11    Signature:  
12    Content:                 Bitstream  
13    UUID (xclbin):          2ad77cd8-9519-4568-938e-8d376acc3ea2  
14    Sections:                DEBUG_IP_LAYOUT, BITSTREAM, MEM_TOPOLOGY,  
15                                IP_LAYOUT,  
16                                CONNECTIVITY, CLOCK_FREQ_TOPOLOGY,  
17                                BUILD_METADATA,  
18                                EMBEDDED_METADATA, SYSTEM_METADATA,  
19                                GROUP_CONNECTIVITY, GROUP_TOPOLOGY  
20  
21 Hardware Platform (Shell) Information  
22  
23     Vendor:                 xilinx  
24     Board:                  u200  
25     Name:                   xdma  
26     Version:                201830.2  
27     Generated Version:      Vivado 2018.3 (SW Build: 2568420)  
28     Created:                Tue Jun 25 06:55:20 2019  
29     FPGA Device:            xcu200  
30     Board Vendor:          xilinx.com  
31     Board Name:             xilinx.com:au200:1.0  
32     Board Part:             xilinx.com:au200:part0:1.0  
33     Platform VBNV:          xilinx_u200_xdma_201830_2  
34     Static UUID:            c102e7af-b2b8-4381-992b-9a00cc3863eb  
35     Feature ROM TimeStamp: 1561465320  
36 Clocks
```

```
37 Name: DATA_CLK
38 Index: 0
39 Type: DATA
40 Frequency: 300 MHz
41
42 Name: KERNEL_CLK
43 Index: 1
44 Type: KERNEL
45 Frequency: 500 MHz
46
47 Memory Configuration
48
49 Name: bank0
50 Index: 0
51 Type: MEM_DDR4
52 Base Address: 0x4000000000
53 Address Size: 0x4000000000
54 Bank Used: No
55
56 Name: bank1
57 Index: 1
58 Type: MEM_DDR4
59 Base Address: 0x5000000000
60 Address Size: 0x4000000000
61 Bank Used: No
62
63 Name: bank2
64 Index: 2
65 Type: MEM_DDR4
66 Base Address: 0x6000000000
67 Address Size: 0x4000000000
68 Bank Used: No
69
70 Name: bank3
71 Index: 3
72 Type: MEM_DDR4
73 Base Address: 0x7000000000
74 Address Size: 0x4000000000
75 Bank Used: Yes
76
77 Name: PLRAM[0]
78 Index: 4
79 Type: MEM_DRAM
80 Base Address: 0x3000000000
81 Address Size: 0x20000
82 Bank Used: No
```

```

83
84     Name:          PLRAM[1]
85     Index:         5
86     Type:          MEM_DRAM
87     Base Address: 0x3000200000
88     Address Size: 0x20000
89     Bank Used:   No
90
91
92     Name:          PLRAM[2]
93     Index:         6
94     Type:          MEM_DRAM
95     Base Address: 0x3000400000
96     Address Size: 0x20000
97     Bank Used:   No
98
99
100    Kernel: rtl_kernel_wizard_0
101
102    Definition
103
104    Ports
105
106    Port:          s_axi_control
107    Mode:          slave
108    Range (bytes): 0x1000
109    Data Width:   32 bits
110    Port Type:    addressable
111
112    Port:          m00_axi
113    Mode:          master
114    Range (bytes): 0xFFFFFFFFFFFFFF
115    Data Width:   512 bits
116    Port Type:    addressable
117
118
119    Instance:      vinc0
120    Base Address: 0x1e00000
121
122    Argument:      scalar00
123    Register Offset: 0x010
124    Port:          s_axi_control
125    Memory:        <not applicable>
126
127    Argument:      axi00_ptr0

```

```

128 Register Offset: 0x018
129 Port: m00_axi
130 Memory: bank3 (MEM_DDR4)
131
132 Generated By
133
134 Command: v++
135 Version: 2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)
136 Command Line: v++ --config /iu_home/iu7179/workspace/Alveo_lab1_kernels
    /vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/myconf.conf --
    connectivity.nk rtl_kernel_wizard_0:1:vinc0 --connectivity.slr vinc0:SLR2
    --connectivity.sp vinc0.m00_axi:DDR[3] --connectivity.sp vinc0.
    m00_axi:PLRAM[0] --input_files /iu_home/iu7179/workspace/
    Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/
    rtl_kernel_wizard_0.xo --link --optimize 0 --output vinc.xclbin --
    platform xilinx_u200_xdma_201830_2 --report_level 0 --target hw --
    vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=Explore --
    vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.DIRECTIVE=Explore --
    vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED=true --vivado
    .prop run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.DIRECTIVE=
    AggressiveExplore --vivado.prop run.impl_1.STEPS.ROUTE_DESIGN.ARGS.
    DIRECTIVE=Explore
137 Options: --config /iu_home/iu7179/workspace/Alveo_lab1_kernels/
    vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/myconf.conf
    --connectivity.nk rtl_kernel_wizard_0:1:vinc0
    --connectivity.slr vinc0:SLR2
    --connectivity.sp vinc0.m00_axi:DDR[3]
    --connectivity.sp vinc0.m00_axi:PLRAM[0]
    --input_files /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/rtl_kernel_wizard_0.xo
    --link
    --optimize 0
    --output vinc.xclbin
    --platform xilinx_u200_xdma_201830_2
    --report_level 0
    --target hw
    --vivado.prop run.impl_1.STEPS.OPT_DESIGN.ARGS.DIRECTIVE=
        Explore
    --vivado.prop run.impl_1.STEPS.PLACE_DESIGN.ARGS.
        DIRECTIVE=Explore
    --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.IS_ENABLED
        =true
    --vivado.prop run.impl_1.STEPS.PHYS_OPT_DESIGN.ARGS.
        DIRECTIVE=AggressiveExplore

```

```
153      —vivado.prop.run.impl_1.STEPS.ROUTE_DESIGN.ARGS.  
154          DIRECTIVE=Explore  
155 User Added Key Value Pairs  
156 _____  
157     <empty>  
158 _____
```

ПРИЛОЖЕНИЕ В

СОДЕРЖИМОЕ LOG-ФАЙЛА

Листинг В.1 – СОДЕРЖИМОЕ LOG-ФАЙЛА.

```
1 INFO: [v++ 60-1306] Additional information associated with this v++ link  
can be found at:  
2 Reports: /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/  
/rtl_kernel_wizard_0_ex/exports/_x/reports/link  
3 Log files: /iu_home/iu7179/workspace/Alveo_lab1_kernels/  
vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/logs/link  
4 INFO: [v++ 60-1548] Creating build summary session with primary output /  
iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/  
rtl_kernel_wizard_0_ex/exports/vinc.xclbin.link_summary, at Sat Dec 11  
11:52:07 2021  
5 INFO: [v++ 60-1316] Initiating connection to rulecheck server, at Sat Dec  
11 11:52:07 2021  
6 INFO: [v++ 60-1315] Creating rulecheck session with output '/iu_home/iu7179/  
/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/  
exports/_x/reports/link/v++_link_vinc_guidance.html', at Sat Dec 11  
11:52:26 2021  
7 INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/  
xilinx_u200_xdma_201830_2/xilinx_u200_xdma_201830_2.xpfm  
8 INFO: [v++ 60-1578] This platform contains Device Support Archive '/opt/  
xilinx/platforms/xilinx_u200_xdma_201830_2/hw/xilinx_u200_xdma_201830_2.  
dsa'  
9 INFO: [v++ 74-74] Compiler Version string: 2020.2  
10 INFO: [v++ 60-1302] Platform 'xilinx_u200_xdma_201830_2.xpfm' has been  
explicitly enabled for this release.  
11 INFO: [v++ 60-629] Linking for hardware target  
12 INFO: [v++ 60-423] Target device: xilinx_u200_xdma_201830_2  
13 INFO: [v++ 60-1332] Run 'run_link' status: Not started  
14 INFO: [v++ 60-1443] [11:53:22] Run run_link: Step system_link: Started  
15 INFO: [v++ 60-1453] Command Line: system_link —xo /iu_home/iu7179/  
workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/  
exports/rtl_kernel_wizard_0.xo —config /iu_home/iu7179/workspace/  
Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/  
link/int/syslinkConfig.ini —xpfm /opt/xilinx/platforms/  
xilinx_u200_xdma_201830_2/xilinx_u200_xdma_201830_2.xpfm —target hw —  
output_dir /iu_home/iu7179/workspace/Alveo_lab1_kernels/  
vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int —temp_dir  
/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/  
rtl_kernel_wizard_0_ex/exports/_x/link/sys_link  
16 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/  
Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/  
link/run_link
```

```

17 INFO: [SYSTEM_LINK 60-1316] Initiating connection to rulecheck server , at
      Sat Dec 11 11:53:37 2021
18 INFO: [SYSTEM_LINK 82-70] Extracting xo v3 file /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/
      rtl_kernel_wizard_0.xo
19 INFO: [SYSTEM_LINK 82-53] Creating IP database /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
      link/sys_link/_sysl/.cdb/xd_ip_db.xml
20 INFO: [SYSTEM_LINK 82-38] [11:53:39] build_xd_ip_db started: /data/Xilinx/
      Vitis/2020.2/bin/build_xd_ip_db -ip_search 0 -sds-pf /iu_home/iu7179/
      workspace/Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/
      exports/_x/link/sys_link/xilinx_u200_xdma_201830_2.hpfm -clkid 0 -ip /
      iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado rtl_kernel/
      rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/iprepo/
      mycompany_com_kernel rtl_kernel_wizard_0_1_0,rtl_kernel_wizard_0 -o /
      iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado rtl_kernel/
      rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
21 INFO: [SYSTEM_LINK 82-37] [11:54:08] build_xd_ip_db finished successfully
22 Time (s): cpu = 00:00:30 ; elapsed = 00:00:29 . Memory (MB): peak =
      1557.895 ; gain = 0.000 ; free physical = 51564 ; free virtual = 232990
23 INFO: [SYSTEM_LINK 82-51] Create system connectivity graph
24 INFO: [SYSTEM_LINK 82-102] Applying explicit connections to the system
      connectivity graph: /iu_home/iu7179/workspace/Alveo_lab1_kernels/
      vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/
      cfgraph/cfgen_cfgraph.xml
25 INFO: [SYSTEM_LINK 82-38] [11:54:08] cfgen started: /data/Xilinx/Vitis
      /2020.2/bin/cfgen -nk rtl_kernel_wizard_0:1:vinc0 -slr vinc0:SLR2 -sp
      vinc0.m00_axi:DDR[3] -sp vinc0.m00_axi:PLRAM[0] -dmclkid 0 -r /iu_home/
      iu7179/workspace/Alveo_lab1_kernels/vivado rtl_kernel/
      rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
      -o /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado rtl_kernel/
      rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/cfgraph/cfgen_cfgraph.
      xml
26 INFO: [CFGGEN 83-0] Kernel Specs:
27 INFO: [CFGGEN 83-0] kernel: rtl_kernel_wizard_0 , num: 1 {vinc0}
28 INFO: [CFGGEN 83-0] Port Specs:
29 INFO: [CFGGEN 83-0] kernel: vinc0 , k_port: m00_axi , sptag: DDR[3]
30 INFO: [CFGGEN 83-0] kernel: vinc0 , k_port: m00_axi , sptag: PLRAM[0]
31 INFO: [CFGGEN 83-0] SLR Specs:
32 INFO: [CFGGEN 83-0] instance: vinc0 , SLR: SLR2
33 INFO: [CFGGEN 83-2228] Creating mapping for argument vinc0.axi00_ptr0 to DDR
      [3] for directive vinc0.m00_axi:DDR[3]
34 INFO: [SYSTEM_LINK 82-37] [11:54:30] cfgen finished successfully
35 Time (s): cpu = 00:00:21 ; elapsed = 00:00:22 . Memory (MB): peak =
      1557.895 ; gain = 0.000 ; free physical = 47722 ; free virtual = 229156
36 INFO: [SYSTEM_LINK 82-52] Create top-level block diagram

```

```

37 INFO: [SYSTEM_LINK 82-38] [11:54:30] cf2bd started: /data/Xilinx/Vitis
        /2020.2/bin(cf2bd --linux --trace-buffer 1024 --input_file /iu_home/
        iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/cfggraph/cfggen_cfggraph.
        xml --ip_db /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/_sysl
        /.cdb/xd_ip_db.xml --cf_name dr --working_dir /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/sys_link/_sysl/.xsd --temp_dir /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/sys_link --output_dir /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int --target_bd
        pfm_dynamic.bd
38 INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /
        iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/cfggraph/cfggen_cfggraph.
        xml -r /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/_sysl/.cdb/xd_ip_db.xml
        -o dr.xml
39 INFO: [CF2BD 82-28] cf2xd finished successfully
40 INFO: [CF2BD 82-31] Launching cf_xsds: cf_xsds -disable-address-gen -bd
        pfm_dynamic.bd -dn dr -dp /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/sys_link/_sysl
        /.xsd
41 INFO: [CF2BD 82-28] cf_xsds finished successfully
42 INFO: [SYSTEM_LINK 82-37] [11:54:43] cf2bd finished successfully
43 Time (s): cpu = 00:00:11 ; elapsed = 00:00:13 . Memory (MB): peak =
        1557.895 ; gain = 0.000 ; free physical = 47497 ; free virtual = 228947
44 INFO: [v++ 60-1441] [11:54:44] Run run_link: Step system_link: Completed
45 Time (s): cpu = 00:01:18 ; elapsed = 00:01:22 . Memory (MB): peak =
        1576.969 ; gain = 0.000 ; free physical = 47563 ; free virtual = 229009
46 INFO: [v++ 60-1443] [11:54:44] Run run_link: Step cf2sw: Started
47 INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/int/sdsl.dat -rtd /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/cf2sw.rtd -
        nofilter /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/cf2sw_full.rtd -xclbin /
        iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/xclbin_orig.xml -o /iu_home/
        iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/xclbin_orig.1.xml
48 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/run_link
49 INFO: [v++ 60-1441] [11:54:57] Run run_link: Step cf2sw: Completed

```

```

50 Time (s): cpu = 00:00:13 ; elapsed = 00:00:14 . Memory (MB): peak =
      1576.969 ; gain = 0.000 ; free physical = 46909 ; free virtual = 228364
51 INFO: [v++ 60-1443] [11:54:57] Run run_link: Step rtd2_system_diagram:
      Started
52 INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram
53 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
      link/run_link
54 INFO: [v++ 60-1441] [11:55:06] Run run_link: Step rtd2_system_diagram:
      Completed
55 Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:09 . Memory (MB): peak =
      1576.969 ; gain = 0.000 ; free physical = 44422 ; free virtual = 225881
56 INFO: [v++ 60-1443] [11:55:06] Run run_link: Step vpl: Started
57 INFO: [v++ 60-1453] Command Line: vpl -t hw -f xilinx_u200_xdma_201830_2 --
      remote_ip_cache /iu_home/iu7179/workspace/Alveo_lab1_kernels/
      vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/.ipcache --output_dir /
      iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado rtl_kernel/
      rtl_kernel_wizard_0_ex/exports/_x/link/int --log_dir /iu_home/iu7179/
      workspace/Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/
      exports/_x/logs/link --report_dir /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
      reports/link --config /iu_home/iu7179/workspace/Alveo_lab1_kernels/
      vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/vplConfig.
      ini -k /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado rtl_kernel/
      rtl_kernel_wizard_0_ex/exports/_x/link/int/kernel_info.dat --
      webtalk_flag Vitis --temp_dir /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
      link --no-info --iprepo /iu_home/iu7179/workspace/Alveo_lab1_kernels/
      vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/xo/ip_repo/
      mycompany_com_kernel rtl_kernel_wizard_0_1_0 --messageDb /iu_home/iu7179/
      workspace/Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/
      exports/_x/link/run_link/vpl.pb /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
      link/int/dr.bd.tcl
58 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
      Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
      link/run_link
59
60 ***** vpl v2020.2 (64-bit)
61 **** SW Build (by xbuild) on 2020-11-18-05:13:29
62 ** Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.
63
64 INFO: [VPL 60-839] Read in kernel information from file '/iu_home/iu7179/
      workspace/Alveo_lab1_kernels/vivado rtl_kernel/rtl_kernel_wizard_0_ex/
      exports/_x/link/int/kernel_info.dat'.
65 INFO: [VPL 74-74] Compiler Version string: 2020.2

```

```
66 INFO: [VPL 60-423] Target device: xilinx_u200_xdma_201830_2
67 INFO: [VPL 60-1032] Extracting hardware platform to /iu_home/iu7179/
    workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/
    exports/_x/link/vivado/vpl/.local/hw_platform
68 WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not exist.
69 [11:59:47] Run vpl: Step create_project: Started
70 Creating Vivado project.
71 [12:00:13] Run vpl: Step create_project: Completed
72 [12:00:13] Run vpl: Step create_bd: Started
73 [12:01:46] Run vpl: Step create_bd: RUNNING...
74 [12:03:19] Run vpl: Step create_bd: RUNNING...
75 [12:04:51] Run vpl: Step create_bd: RUNNING...
76 [12:06:41] Run vpl: Step create_bd: RUNNING...
77 [12:08:21] Run vpl: Step create_bd: RUNNING...
78 [12:09:26] Run vpl: Step create_bd: Completed
79 [12:09:26] Run vpl: Step update_bd: Started
80 [12:09:30] Run vpl: Step update_bd: Completed
81 [12:09:30] Run vpl: Step generate_target: Started
82 [12:11:07] Run vpl: Step generate_target: RUNNING...
83 [12:12:41] Run vpl: Step generate_target: RUNNING...
84 [12:14:11] Run vpl: Step generate_target: RUNNING...
85 [12:15:46] Run vpl: Step generate_target: RUNNING...
86 [12:17:15] Run vpl: Step generate_target: RUNNING...
87 [12:18:53] Run vpl: Step generate_target: RUNNING...
88 [12:20:22] Run vpl: Step generate_target: RUNNING...
89 [12:22:07] Run vpl: Step generate_target: RUNNING...
90 [12:22:09] Run vpl: Step generate_target: Completed
91 [12:22:09] Run vpl: Step config_hw_runs: Started
92 [12:23:50] Run vpl: Step config_hw_runs: RUNNING...
93 [12:24:06] Run vpl: Step config_hw_runs: Completed
94 [12:24:06] Run vpl: Step synth: Started
95 [12:26:25] Block-level synthesis in progress, 0 of 66 jobs complete, 3 jobs
    running.
96 [12:27:02] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
    running.
97 [12:27:40] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
    running.
98 [12:28:17] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
    running.
99 [12:29:00] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
    running.
100 [12:29:39] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
    running.
101 [12:30:18] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
    running.
```

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102 [12:30:55] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
103 [12:31:36] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
104 [12:32:14] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
105 [12:32:53] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
106 [12:33:30] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
107 [12:34:11] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
108 [12:34:48] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs
     running.
109 [12:35:29] Block-level synthesis in progress, 6 of 66 jobs complete, 2 jobs
     running.
110 [12:36:07] Block-level synthesis in progress, 7 of 66 jobs complete, 1 job
     running.
111 [12:36:48] Block-level synthesis in progress, 7 of 66 jobs complete, 4 jobs
     running.
112 [12:37:27] Block-level synthesis in progress, 7 of 66 jobs complete, 8 jobs
     running.
113 [12:38:06] Block-level synthesis in progress, 9 of 66 jobs complete, 6 jobs
     running.
114 [12:38:43] Block-level synthesis in progress, 10 of 66 jobs complete, 5
     jobs running.
115 [12:39:24] Block-level synthesis in progress, 10 of 66 jobs complete, 7
     jobs running.
116 [12:40:00] Block-level synthesis in progress, 11 of 66 jobs complete, 7
     jobs running.
117 [12:40:38] Block-level synthesis in progress, 12 of 66 jobs complete, 6
     jobs running.
118 [12:41:17] Block-level synthesis in progress, 12 of 66 jobs complete, 6
     jobs running.
119 [12:41:58] Block-level synthesis in progress, 12 of 66 jobs complete, 8
     jobs running.
120 [12:42:35] Block-level synthesis in progress, 13 of 66 jobs complete, 7
     jobs running.
121 [12:43:18] Block-level synthesis in progress, 13 of 66 jobs complete, 7
     jobs running.
122 [12:43:57] Block-level synthesis in progress, 13 of 66 jobs complete, 7
     jobs running.
123 [12:44:34] Block-level synthesis in progress, 13 of 66 jobs complete, 8
     jobs running.
124 [12:45:13] Block-level synthesis in progress, 16 of 66 jobs complete, 5
     jobs running.
```

125 [12:45:52] Block-level synthesis in progress, 17 of 66 jobs complete, 4
jobs running.
126 [12:46:31] Block-level synthesis in progress, 18 of 66 jobs complete, 6
jobs running.
127 [12:47:07] Block-level synthesis in progress, 18 of 66 jobs complete, 7
jobs running.
128 [12:47:45] Block-level synthesis in progress, 19 of 66 jobs complete, 7
jobs running.
129 [12:48:21] Block-level synthesis in progress, 19 of 66 jobs complete, 7
jobs running.
130 [12:48:59] Block-level synthesis in progress, 21 of 66 jobs complete, 6
jobs running.
131 [12:49:37] Block-level synthesis in progress, 21 of 66 jobs complete, 6
jobs running.
132 [12:50:16] Block-level synthesis in progress, 21 of 66 jobs complete, 8
jobs running.
133 [12:50:53] Block-level synthesis in progress, 22 of 66 jobs complete, 7
jobs running.
134 [12:51:34] Block-level synthesis in progress, 22 of 66 jobs complete, 7
jobs running.
135 [12:52:10] Block-level synthesis in progress, 22 of 66 jobs complete, 8
jobs running.
136 [12:52:48] Block-level synthesis in progress, 22 of 66 jobs complete, 8
jobs running.
137 [12:53:23] Block-level synthesis in progress, 22 of 66 jobs complete, 8
jobs running.
138 [12:54:03] Block-level synthesis in progress, 24 of 66 jobs complete, 6
jobs running.
139 [12:54:39] Block-level synthesis in progress, 25 of 66 jobs complete, 5
jobs running.
140 [12:55:19] Block-level synthesis in progress, 25 of 66 jobs complete, 7
jobs running.
141 [12:55:55] Block-level synthesis in progress, 25 of 66 jobs complete, 8
jobs running.
142 [12:56:35] Block-level synthesis in progress, 27 of 66 jobs complete, 6
jobs running.
143 [12:57:12] Block-level synthesis in progress, 27 of 66 jobs complete, 6
jobs running.
144 [12:57:51] Block-level synthesis in progress, 29 of 66 jobs complete, 6
jobs running.
145 [12:58:26] Block-level synthesis in progress, 29 of 66 jobs complete, 6
jobs running.
146 [12:59:15] Block-level synthesis in progress, 29 of 66 jobs complete, 8
jobs running.
147 [12:59:52] Block-level synthesis in progress, 30 of 66 jobs complete, 7
jobs running.

148 [13:00:54] Block-level synthesis in progress, 31 of 66 jobs complete, 6
jobs running.
149 [13:01:39] Block-level synthesis in progress, 31 of 66 jobs complete, 8
jobs running.
150 [13:02:15] Block-level synthesis in progress, 32 of 66 jobs complete, 7
jobs running.
151 [13:02:55] Block-level synthesis in progress, 32 of 66 jobs complete, 7
jobs running.
152 [13:03:33] Block-level synthesis in progress, 33 of 66 jobs complete, 7
jobs running.
153 [13:04:13] Block-level synthesis in progress, 33 of 66 jobs complete, 7
jobs running.
154 [13:04:50] Block-level synthesis in progress, 33 of 66 jobs complete, 8
jobs running.
155 [13:05:31] Block-level synthesis in progress, 33 of 66 jobs complete, 8
jobs running.
156 [13:06:10] Block-level synthesis in progress, 34 of 66 jobs complete, 7
jobs running.
157 [13:06:52] Block-level synthesis in progress, 36 of 66 jobs complete, 5
jobs running.
158 [13:07:31] Block-level synthesis in progress, 36 of 66 jobs complete, 6
jobs running.
159 [13:08:13] Block-level synthesis in progress, 36 of 66 jobs complete, 8
jobs running.
160 [13:08:48] Block-level synthesis in progress, 36 of 66 jobs complete, 8
jobs running.
161 [13:09:27] Block-level synthesis in progress, 37 of 66 jobs complete, 7
jobs running.
162 [13:10:06] Block-level synthesis in progress, 38 of 66 jobs complete, 6
jobs running.
163 [13:10:50] Block-level synthesis in progress, 39 of 66 jobs complete, 6
jobs running.
164 [13:11:26] Block-level synthesis in progress, 39 of 66 jobs complete, 7
jobs running.
165 [13:12:06] Block-level synthesis in progress, 39 of 66 jobs complete, 8
jobs running.
166 [13:12:44] Block-level synthesis in progress, 40 of 66 jobs complete, 7
jobs running.
167 [13:13:24] Block-level synthesis in progress, 40 of 66 jobs complete, 7
jobs running.
168 [13:14:00] Block-level synthesis in progress, 40 of 66 jobs complete, 8
jobs running.
169 [13:14:42] Block-level synthesis in progress, 40 of 66 jobs complete, 8
jobs running.
170 [13:15:19] Block-level synthesis in progress, 40 of 66 jobs complete, 8
jobs running.

171 [13:16:01] Block-level synthesis in progress , 41 of 66 jobs complete , 7
jobs running .

172 [13:16:40] Block-level synthesis in progress , 41 of 66 jobs complete , 7
jobs running .

173 [13:17:20] Block-level synthesis in progress , 41 of 66 jobs complete , 8
jobs running .

174 [13:17:55] Block-level synthesis in progress , 42 of 66 jobs complete , 7
jobs running .

175 [13:18:36] Block-level synthesis in progress , 42 of 66 jobs complete , 7
jobs running .

176 [13:19:15] Block-level synthesis in progress , 43 of 66 jobs complete , 7
jobs running .

177 [13:19:54] Block-level synthesis in progress , 43 of 66 jobs complete , 7
jobs running .

178 [13:20:30] Block-level synthesis in progress , 44 of 66 jobs complete , 7
jobs running .

179 [13:21:12] Block-level synthesis in progress , 45 of 66 jobs complete , 6
jobs running .

180 [13:21:49] Block-level synthesis in progress , 46 of 66 jobs complete , 7
jobs running .

181 [13:22:28] Block-level synthesis in progress , 46 of 66 jobs complete , 7
jobs running .

182 [13:23:05] Block-level synthesis in progress , 46 of 66 jobs complete , 8
jobs running .

183 [13:23:45] Block-level synthesis in progress , 46 of 66 jobs complete , 8
jobs running .

184 [13:24:22] Block-level synthesis in progress , 46 of 66 jobs complete , 8
jobs running .

185 [13:25:03] Block-level synthesis in progress , 48 of 66 jobs complete , 6
jobs running .

186 [13:25:40] Block-level synthesis in progress , 48 of 66 jobs complete , 6
jobs running .

187 [13:26:19] Block-level synthesis in progress , 49 of 66 jobs complete , 7
jobs running .

188 [13:26:55] Block-level synthesis in progress , 50 of 66 jobs complete , 6
jobs running .

189 [13:27:34] Block-level synthesis in progress , 51 of 66 jobs complete , 7
jobs running .

190 [13:28:10] Block-level synthesis in progress , 51 of 66 jobs complete , 7
jobs running .

191 [13:28:51] Block-level synthesis in progress , 53 of 66 jobs complete , 6
jobs running .

192 [13:29:27] Block-level synthesis in progress , 55 of 66 jobs complete , 5
jobs running .

193 [13:30:08] Block-level synthesis in progress , 57 of 66 jobs complete , 6
jobs running .

194 [13:30:47] Block-level synthesis in progress , 58 of 66 jobs complete , 5
jobs running .

195 [13:31:28] Block-level synthesis in progress , 59 of 66 jobs complete , 6
jobs running .

196 [13:32:05] Block-level synthesis in progress , 59 of 66 jobs complete , 6
jobs running .

197 [13:32:53] Block-level synthesis in progress , 59 of 66 jobs complete , 6
jobs running .

198 [13:33:29] Block-level synthesis in progress , 60 of 66 jobs complete , 5
jobs running .

199 [13:34:11] Block-level synthesis in progress , 60 of 66 jobs complete , 5
jobs running .

200 [13:34:48] Block-level synthesis in progress , 61 of 66 jobs complete , 4
jobs running .

201 [13:35:29] Block-level synthesis in progress , 61 of 66 jobs complete , 4
jobs running .

202 [13:36:05] Block-level synthesis in progress , 61 of 66 jobs complete , 4
jobs running .

203 [13:36:50] Block-level synthesis in progress , 61 of 66 jobs complete , 4
jobs running .

204 [13:37:30] Block-level synthesis in progress , 62 of 66 jobs complete , 3
jobs running .

205 [13:38:15] Block-level synthesis in progress , 63 of 66 jobs complete , 2
jobs running .

206 [13:38:54] Block-level synthesis in progress , 63 of 66 jobs complete , 2
jobs running .

207 [13:39:40] Block-level synthesis in progress , 63 of 66 jobs complete , 2
jobs running .

208 [13:40:17] Block-level synthesis in progress , 63 of 66 jobs complete , 2
jobs running .

209 [13:41:01] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

210 [13:41:38] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

211 [13:42:24] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

212 [13:43:02] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

213 [13:43:46] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

214 [13:44:24] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

215 [13:45:07] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

216 [13:45:44] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

```
217 [13:46:28] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
218 [13:47:05] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
219 [13:47:48] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
220 [13:48:24] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
221 [13:49:05] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
222 [13:49:44] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
223 [13:50:27] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
224 [13:51:05] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
225 [13:51:50] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
226 [13:52:27] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
227 [13:53:12] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
228 [13:53:48] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
229 [13:54:33] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
230 [13:55:09] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
231 [13:55:58] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
232 [13:56:38] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
233 [13:57:23] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
234 [13:58:01] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
235 [13:58:50] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
236 [13:59:28] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
237 [14:00:15] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
238 [14:00:55] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
239 [14:01:43] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job
      running.
```

240 [14:02:23] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

241 [14:03:11] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

242 [14:03:50] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

243 [14:04:36] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

244 [14:05:14] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

245 [14:06:05] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

246 [14:06:43] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

247 [14:07:29] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

248 [14:08:07] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

249 [14:08:53] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

250 [14:09:34] Block-level synthesis in progress , 64 of 66 jobs complete , 1 job
running .

251 [14:10:21] Block-level synthesis in progress , 65 of 66 jobs complete , 0
jobs running .

252 [14:10:59] Block-level synthesis in progress , 65 of 66 jobs complete , 0
jobs running .

253 [14:11:46] Block-level synthesis in progress , 65 of 66 jobs complete , 0
jobs running .

254 [14:12:23] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

255 [14:13:09] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

256 [14:13:48] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

257 [14:14:31] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

258 [14:15:13] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

259 [14:16:01] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

260 [14:16:41] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

261 [14:17:27] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

262 [14:18:07] Block-level synthesis in progress , 65 of 66 jobs complete , 1 job
running .

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263 [14:18:55] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
264 [14:19:33] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
265 [14:20:20] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
266 [14:20:59] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
267 [14:21:45] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
268 [14:22:23] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
269 [14:23:09] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
270 [14:23:49] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
271 [14:24:36] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
272 [14:25:15] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job
      running.
273 [14:26:01] Block-level synthesis in progress, 66 of 66 jobs complete, 0
      jobs running.
274 [14:26:40] Block-level synthesis in progress, 66 of 66 jobs complete, 0
      jobs running.
275 [14:27:28] Top-level synthesis in progress.
276 [14:28:07] Top-level synthesis in progress.
277 [14:28:55] Top-level synthesis in progress.
278 [14:29:35] Top-level synthesis in progress.
279 [14:30:23] Top-level synthesis in progress.
280 [14:31:03] Top-level synthesis in progress.
281 [14:31:47] Top-level synthesis in progress.
282 [14:32:25] Top-level synthesis in progress.
283 [14:33:12] Top-level synthesis in progress.
284 [14:33:51] Top-level synthesis in progress.
285 [14:34:40] Top-level synthesis in progress.
286 [14:35:19] Top-level synthesis in progress.
287 [14:36:02] Top-level synthesis in progress.
288 [14:36:39] Top-level synthesis in progress.
289 [14:37:27] Top-level synthesis in progress.
290 [14:38:07] Top-level synthesis in progress.
291 [14:38:52] Top-level synthesis in progress.
292 [14:39:31] Top-level synthesis in progress.
293 [14:40:41] Run vpl: Step synth: Completed
294 [14:40:41] Run vpl: Step impl: Started
295 [15:50:36] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to
      platform). Elapsed time: 03h 55m 18s
```

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296
297 [15:50:36] Starting logic optimization..
298 [15:56:23] Phase 1 Generate And Synthesize MIG Cores
299 [16:31:20] Phase 2 Generate And Synthesize Debug Cores
300 [16:56:14] Phase 3 Retarget
301 [16:59:14] Phase 4 Constant propagation
302 [17:00:44] Phase 5 Sweep
303 [17:07:17] Phase 6 BUFG optimization
304 [17:09:39] Phase 7 Shift Register Optimization
305 [17:10:20] Phase 8 Post Processing Netlist
306 [17:25:27] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time:
               01h 34m 51s
307
308 [17:25:27] Starting logic placement..
309 [17:30:56] Phase 1 Placer Initialization
310 [17:30:56] Phase 1.1 Placer Initialization Netlist Sorting
311 [17:46:31] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device
312 [17:56:53] Phase 1.3 Build Placer Netlist Model
313 [18:10:39] Phase 1.4 Constrain Clocks/Macros
314 [18:12:08] Phase 2 Global Placement
315 [18:12:08] Phase 2.1 Floorplanning
316 [18:16:29] Phase 2.1.1 Partition Driven Placement
317 [18:16:29] Phase 2.1.1.1 PBP: Partition Driven Placement
318 [18:18:48] Phase 2.1.1.2 PBP: Clock Region Placement
319 [18:23:09] Phase 2.1.1.3 PBP: Compute Congestion
320 [18:23:51] Phase 2.1.1.4 PBP: UpdateTiming
321 [18:26:09] Phase 2.1.1.5 PBP: Add part constraints
322 [18:26:52] Phase 2.2 Update Timing before SLR Path Opt
323 [18:27:39] Phase 2.3 Global Placement Core
324 [19:04:28] Phase 2.3.1 Physical Synthesis In Placer
325 [19:18:31] Phase 3 Detail Placement
326 [19:18:31] Phase 3.1 Commit Multi Column Macros
327 [19:18:31] Phase 3.2 Commit Most Macros & LUTRAMs
328 [19:25:15] Phase 3.3 Small Shape DP
329 [19:25:15] Phase 3.3.1 Small Shape Clustering
330 [19:27:28] Phase 3.3.2 Flow Legalize Slice Clusters
331 [19:28:18] Phase 3.3.3 Slice Area Swap
332 [19:34:15] Phase 3.4 Place Remaining
333 [19:34:54] Phase 3.5 Re-assign LUT pins
334 [19:36:19] Phase 3.6 Pipeline Register Optimization
335 [19:37:06] Phase 3.7 Fast Optimization
336 [19:41:27] Phase 4 Post Placement Optimization and Clean-Up
337 [19:41:27] Phase 4.1 Post Commit Optimization
338 [19:51:52] Phase 4.1.1 Post Placement Optimization
339 [19:52:33] Phase 4.1.1.1 BUFG Insertion
340 [19:52:33] Phase 1 Physical Synthesis Initialization

```

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341 [19:54:54] Phase 4.1.1.2 BUFG Replication
342 [19:58:44] Phase 4.1.1.3 Replication
343 [20:05:24] Phase 4.2 Post Placement Cleanup
344 [20:06:05] Phase 4.3 Placer Reporting
345 [20:06:05] Phase 4.3.1 Print Estimated Congestion
346 [20:08:20] Phase 4.4 Final Placement Cleanup
347 [21:22:38] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 03
               h 57m 11s
348
349 [21:22:38] Starting logic routing..
350 [21:29:11] Phase 1 Build RT Design
351 [21:41:11] Phase 2 Router Initialization
352 [21:41:11] Phase 2.1 Fix Topology Constraints
353 [21:41:51] Phase 2.2 Pre Route Cleanup
354 [21:42:43] Phase 2.3 Global Clock Net Routing
355 [21:44:51] Phase 2.4 Update Timing
356 [21:58:45] Phase 2.5 Update Timing for Bus Skew
357 [21:58:45] Phase 2.5.1 Update Timing
358 [22:03:49] Phase 3 Initial Routing
359 [22:03:49] Phase 3.1 Global Routing
360 [22:09:50] Phase 4 Rip-up And Reroute
361 [22:09:50] Phase 4.1 Global Iteration 0
362 [22:44:51] Phase 4.2 Global Iteration 1
363 [22:49:47] Phase 4.3 Global Iteration 2
364 [22:54:02] Phase 5 Delay and Skew Optimization
365 [22:54:02] Phase 5.1 Delay CleanUp
366 [22:54:02] Phase 5.1.1 Update Timing
367 [23:00:28] Phase 5.2 Clock Skew Optimization
368 [23:01:14] Phase 6 Post Hold Fix
369 [23:01:14] Phase 6.1 Hold Fix Iter
370 [23:01:14] Phase 6.1.1 Update Timing
371 [23:06:19] Phase 7 Route finalize
372 [23:06:19] Phase 8 Verifying routed nets
373 [23:07:42] Phase 9 Depositing Routes
374 [23:12:07] Phase 10 Route finalize
375 [23:12:07] Phase 11 Post Router Timing
376 [23:18:36] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 01h 55m 58
               s
377
378 [23:18:36] Starting bitstream generation..
379 [01:11:05] Creating bitmap...
380 [02:02:33] Writing bitstream ./pfm_top_i_dynamic_region_my_rm_partial.bit
               ...
381 [02:02:33] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed
               time: 02h 43m 56s
382 [02:08:08] Run vpl: Step impl: Completed

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383 [02:08:23] Run vpl: FINISHED. Run Status: impl Complete!
384 INFO: [v++ 60-1441] [02:08:56] Run run_link: Step vpl: Completed
385 Time (s): cpu = 00:57:47 ; elapsed = 14:13:49 . Memory (MB): peak =
    1576.969 ; gain = 0.000 ; free physical = 53967 ; free virtual = 197097
386 INFO: [v++ 60-1443] [02:08:56] Run run_link: Step rtdgen: Started
387 INFO: [v++ 60-1453] Command Line: rtdgen
388 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
    Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
    link/run_link
389 INFO: [v++ 60-991] clock name 'clkwiz_kernel_clk_out1' (clock ID '0') is
    being mapped to clock name 'DATA_CLK' in the xclbin
390 INFO: [v++ 60-991] clock name 'clkwiz_kernel2_clk_out1' (clock ID '1') is
    being mapped to clock name 'KERNEL_CLK' in the xclbin
391 INFO: [v++ 60-1230] The compiler selected the following frequencies for the
    runtime controllable kernel clock(s) and scalable system clock(s):
    Kernel (DATA) clock: clkwiz_kernel_clk_out1 = 300, Kernel (KERNEL) clock
    : clkwiz_kernel2_clk_out1 = 500
392 INFO: [v++ 60-1453] Command Line: cf2sw -a /iu_home/iu7179/workspace/
    Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
    link/int/address_map.xml -sdsl /iu_home/iu7179/workspace/
    Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
    link/int/sdsl.dat -xclbin /iu_home/iu7179/workspace/Alveo_lab1_kernels/
    vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/xclbin_orig.
    xml -rtd /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
    /rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc.rtd -o /iu_home/iu7179/
    workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/
    exports/_x/link/int/vinc.xml
393 INFO: [v++ 60-1652] Cf2sw returned exit code: 0
394 INFO: [v++ 60-2311] HPISystemDiagram::writeSystemDiagramAfterRunningVivado ,
    rtdInputFilePath: /iu_home/iu7179/workspace/Alveo_lab1_kernels/
    vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc.rtd
395 INFO: [v++ 60-2312] HPISystemDiagram::writeSystemDiagramAfterRunningVivado ,
    systemDiagramOutputFilePath: /iu_home/iu7179/workspace/
    Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
    link/int/systemDiagramModelSlrBaseAddress.json
396 INFO: [v++ 60-1618] Launching
397 INFO: [v++ 60-1441] [02:09:08] Run run_link: Step rtdgen: Completed
398 Time (s): cpu = 00:00:11 ; elapsed = 00:00:12 . Memory (MB): peak =
    1576.969 ; gain = 0.000 ; free physical = 53806 ; free virtual = 196937
399 INFO: [v++ 60-1443] [02:09:08] Run run_link: Step xclbinutil: Started
400 INFO: [v++ 60-1453] Command Line: xclbinutil --add-section DEBUG_IP_LAYOUT:
    JSON:/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
    rtl_kernel_wizard_0_ex/exports/_x/link/int/debug_ip_layout.rtd --add-
    section BITSTREAM:RAW:/iu_home/iu7179/workspace/Alveo_lab1_kernels/
    vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/partial.bit
    --force --target hw --key-value SYS:dfx_enable:true --add-section :JSON

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: /iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc.rtd --append-section :
JSON:/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
rtl_kernel_wizard_0_ex/exports/_x/link/int/appendSection.rtd --add-
section CLOCK_FREQ_TOPOLOGY:JSON:/iu_home/iu7179/workspace/
Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
link/int/vinc_xml.rtd --add-section BUILD_METADATA:JSON:/iu_home/iu7179/
workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/
exports/_x/link/int/vinc_build.rtd --add-section EMBEDDED_METADATA:RAW:/
iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc.xml --add-section
SYSTEM_METADATA:RAW:/iu_home/iu7179/workspace/Alveo_lab1_kernels/
vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/link/int/
systemDiagramModelSlrBaseAddress.json --output /iu_home/iu7179/workspace
/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/
vinc.xclbin

401 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
    Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/run_link

402 XRT Build Version: 2.8.743 (2020.2)
403     Build Date: 2020-11-16 00:19:11
404     Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9
405 Creating a default 'in-memory' xclbin image.

406
407 Section: 'DEBUG_IP_LAYOUT'(9) was successfully added.
408 Size   : 440 bytes
409 Format : JSON
410 File   : '/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
    rtl_kernel_wizard_0_ex/exports/_x/link/int/debug_ip_layout.rtd'

411
412 Section: 'BITSTREAM'(0) was successfully added.
413 Size   : 42563630 bytes
414 Format : RAW
415 File   : '/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
    rtl_kernel_wizard_0_ex/exports/_x/link/int/partial.bit'

416
417 Section: 'MEM_TOPOLOGY'(6) was successfully added.
418 Format : JSON
419 File   : 'mem_topology'

420
421 Section: 'IP_LAYOUT'(8) was successfully added.
422 Format : JSON
423 File   : 'ip_layout'

424
425 Section: 'CONNECTIVITY'(7) was successfully added.
426 Format : JSON

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427 File    : 'connectivity'
428
429 Section: 'CLOCK_FREQ_TOPOLOGY'(11) was successfully added.
430 Size    : 274 bytes
431 Format  : JSON
432 File    : '/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc_xml.rtd'
433
434 Section: 'BUILD_METADATA'(14) was successfully added.
435 Size    : 3138 bytes
436 Format  : JSON
437 File    : '/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc_build.rtd'
438
439 Section: 'EMBEDDED_METADATA'(2) was successfully added.
440 Size    : 2759 bytes
441 Format  : RAW
442 File    : '/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/vinc.xml'
443
444 Section: 'SYSTEM_METADATA'(22) was successfully added.
445 Size    : 5802 bytes
446 Format  : RAW
447 File    : '/iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/_x/link/int/
        systemDiagramModelSlrBaseAddress.json'
448
449 Section: 'IP_LAYOUT'(8) was successfully appended to .
450 Format  : JSON
451 File    : 'ip_layout'
452 Successfully wrote (42586187 bytes) to the output file: /iu_home/iu7179/
        workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/
        exports/vinc.xclbin
453 Leaving xclbinutil.
454 INFO: [v++ 60-1441] [02:09:11] Run run_link: Step xclbinutil: Completed
455 Time (s): cpu = 00:00:00.47 ; elapsed = 00:00:03 . Memory (MB): peak =
        1576.969 ; gain = 0.000 ; free physical = 53632 ; free virtual = 196885
456 INFO: [v++ 60-1443] [02:09:11] Run run_link: Step xclbinutilinfo: Started
457 INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /
        iu_home/iu7179/workspace/Alveo_lab1_kernels/vivado_rtl_kernel/
        rtl_kernel_wizard_0_ex/exports/vinc.xclbin.info --input /iu_home/iu7179/
        workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/
        exports/vinc.xclbin
458 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/run_link

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459 INFO: [v++ 60-1441] [02:09:14] Run run_link: Step xclbinutilinfo: Completed
460 Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak =
        1576.969 ; gain = 0.000 ; free physical = 53700 ; free virtual = 196953
461 INFO: [v++ 60-1443] [02:09:14] Run run_link: Step generate_sc_driver:
        Started
462 INFO: [v++ 60-1453] Command Line:
463 INFO: [v++ 60-1454] Run Directory: /iu_home/iu7179/workspace/
        Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/
        link/run_link
464 INFO: [v++ 60-1441] [02:09:14] Run run_link: Step generate_sc_driver:
        Completed
465 Time (s): cpu = 00:00:00.01 ; elapsed = 00:00:00.05 . Memory (MB): peak =
        1576.969 ; gain = 0.000 ; free physical = 53718 ; free virtual = 196970
466 INFO: [v++ 60-244] Generating system estimate report...
467 INFO: [v++ 60-1092] Generated system estimate report: /iu_home/iu7179/
        workspace/Alveo_lab1_kernels/vivado_rtl_kernel/rtl_kernel_wizard_0_ex/
        exports/_x/reports/link/system_estimate_vinc.txt
468 INFO: [v++ 60-586] Created /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/vinc.ltx
469 INFO: [v++ 60-586] Created vinc.xclbin
470 INFO: [v++ 60-1307] Run completed. Additional information can be found in:
471     Guidance: /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/reports/link/v++
        _link_vinc_guidance.html
472     Timing Report: /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/reports/link/imp
        /impl_1_xilinx_u200_xdma_201830_2_bb_locked_timing_summary_routed.
        rpt
473     Vivado Log: /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/logs/link/vivado
        .log
474     Steps Log File: /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/_x/logs/link/link.
        steps.log
475
476 INFO: [v++ 60-2343] Use the vitis_analyzer tool to visualize and navigate
        the relevant reports. Run the following command.
477     vitis_analyzer /iu_home/iu7179/workspace/Alveo_lab1_kernels/
        vivado_rtl_kernel/rtl_kernel_wizard_0_ex/exports/vinc.xclbin .
        link_summary
478 INFO: [v++ 60-791] Total elapsed time: 14h 18m 23s
479 INFO: [v++ 60-1653] Closing dispatch client.

```