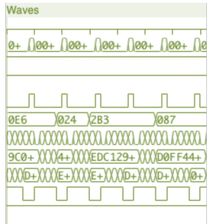
VIVADO

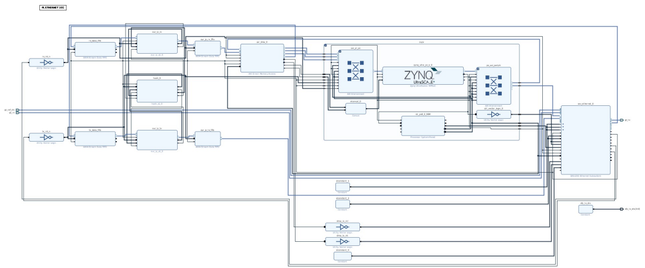
PetaLinux

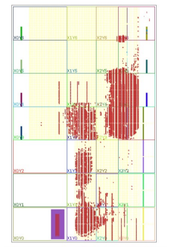
AMD XILINX

XILINX VITIS

Verilog + Verilator: Develop & Simulate → **Vivado: PL Block Design** → **Vivado: Synthesis** → **PetaLinux : Image** → **Vitis: Cross Compile** → **C: Traffic Generator**







Zynq UltraScale+ MPSoC ZCU102