VIVADO

Verilog + Verilator: Develop & Simulate

Vivado: PL Block Design

Vivado: Synthesis

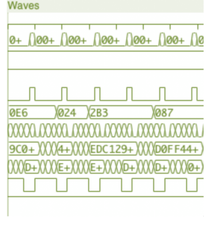
PetaLinux: Image

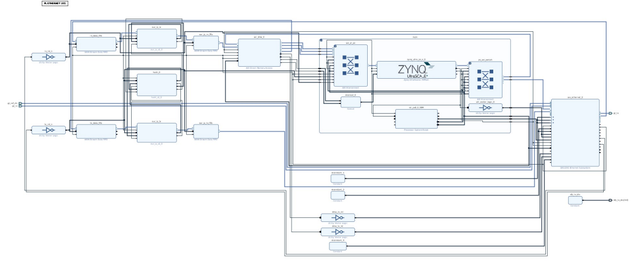
AMD XILINX

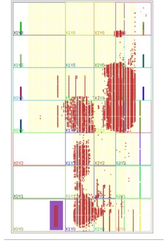
XILINX VITIS

Vitis: Cross Compile

C: Traffic Generator







Zynq UltraScale+ MPSoC ZCU102