

Lab 08: D Latch and D FlipFlop Analysis

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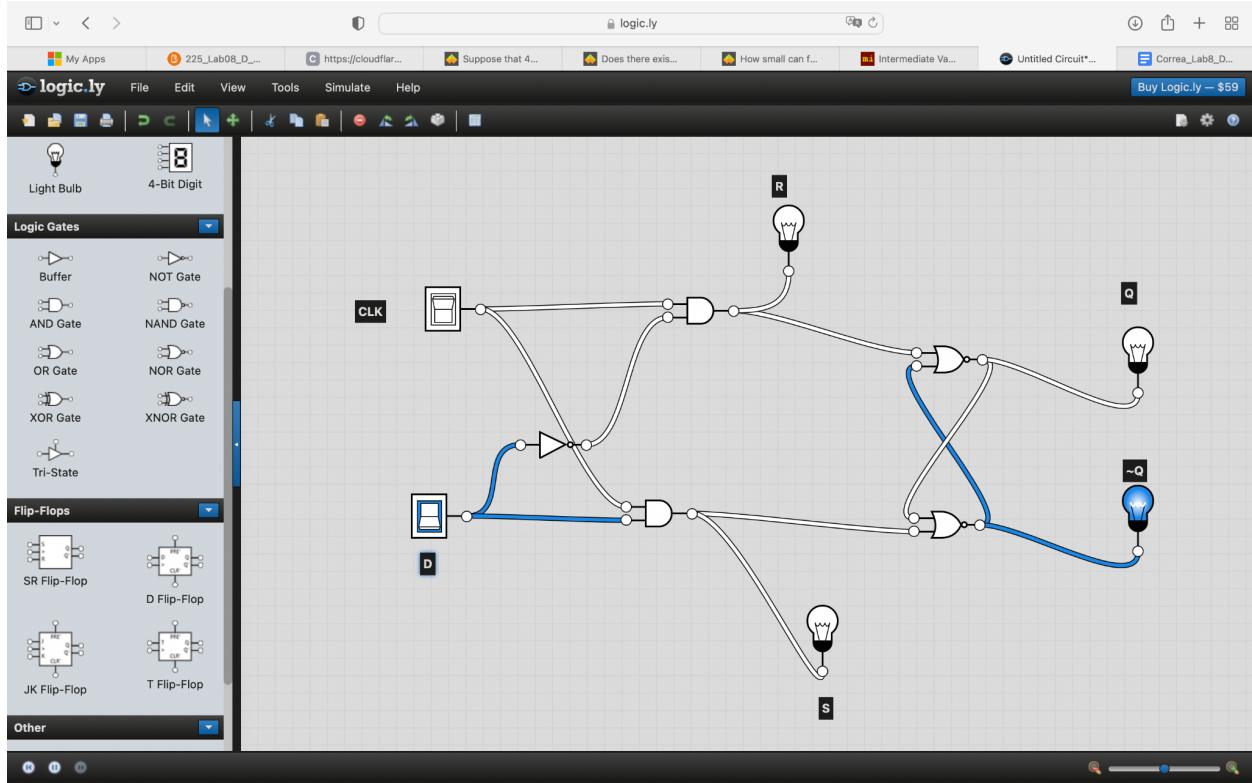
1. D-Latch

Table

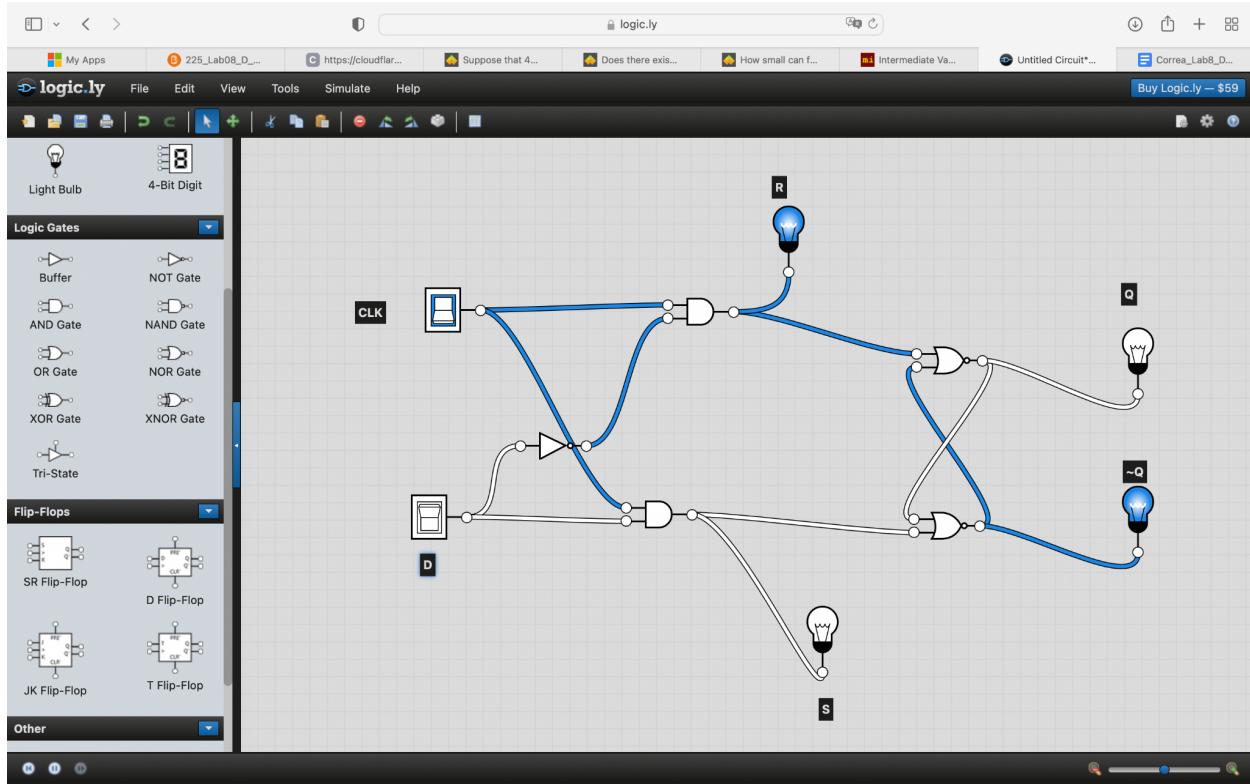
Steps	Clock	D	S	R	Q	$\sim Q$	Case
Step - 1	0	1	0	0	Qprev	$\sim Q$ Prev	Opaque
Step - 2	1	0	0	1	0	1	Transparent
Step - 3	1	1	1	0	1	0	Transparent
Step - 4	0	0	0	0	Qprev	$\sim Q$ prev	Opaque

Scenarios for D-Latch:

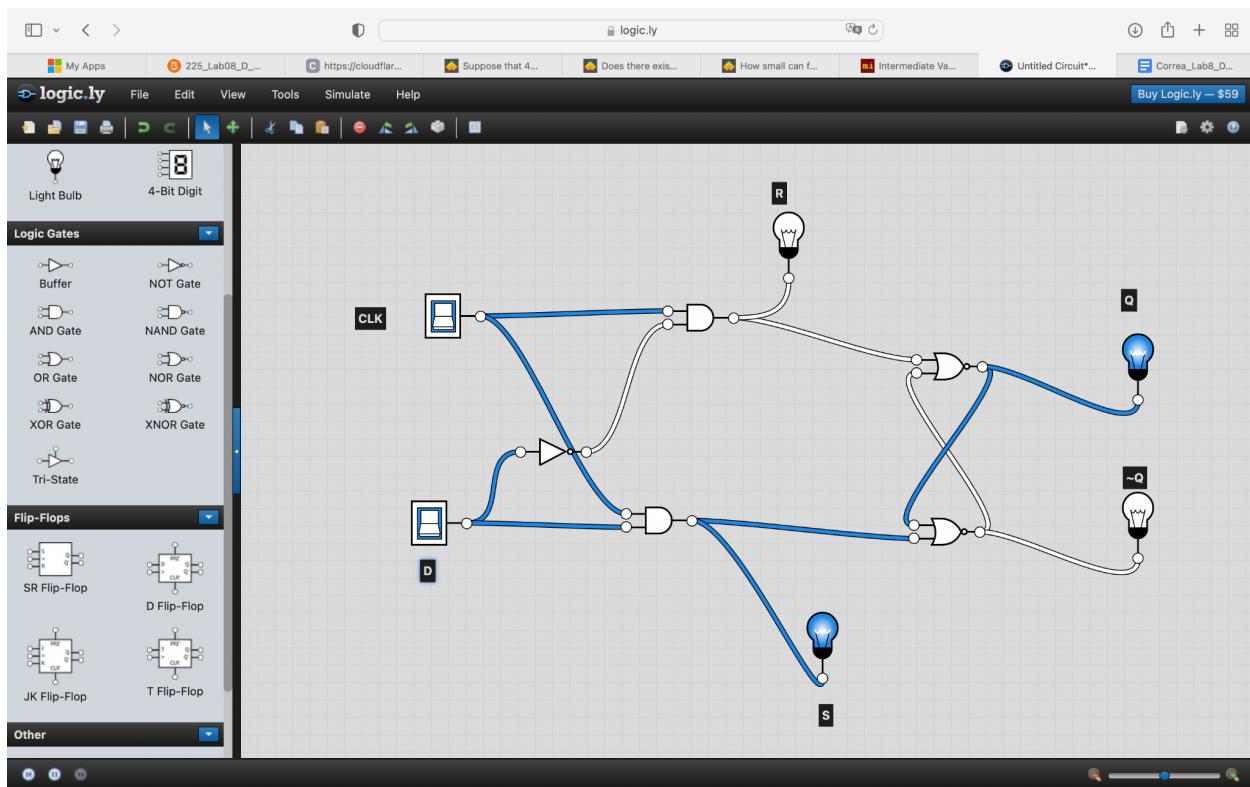
CLK = 0, D = 1, S = 0, R = 0, Q = Q_{prev}, ~Q = ~Q_{prev}



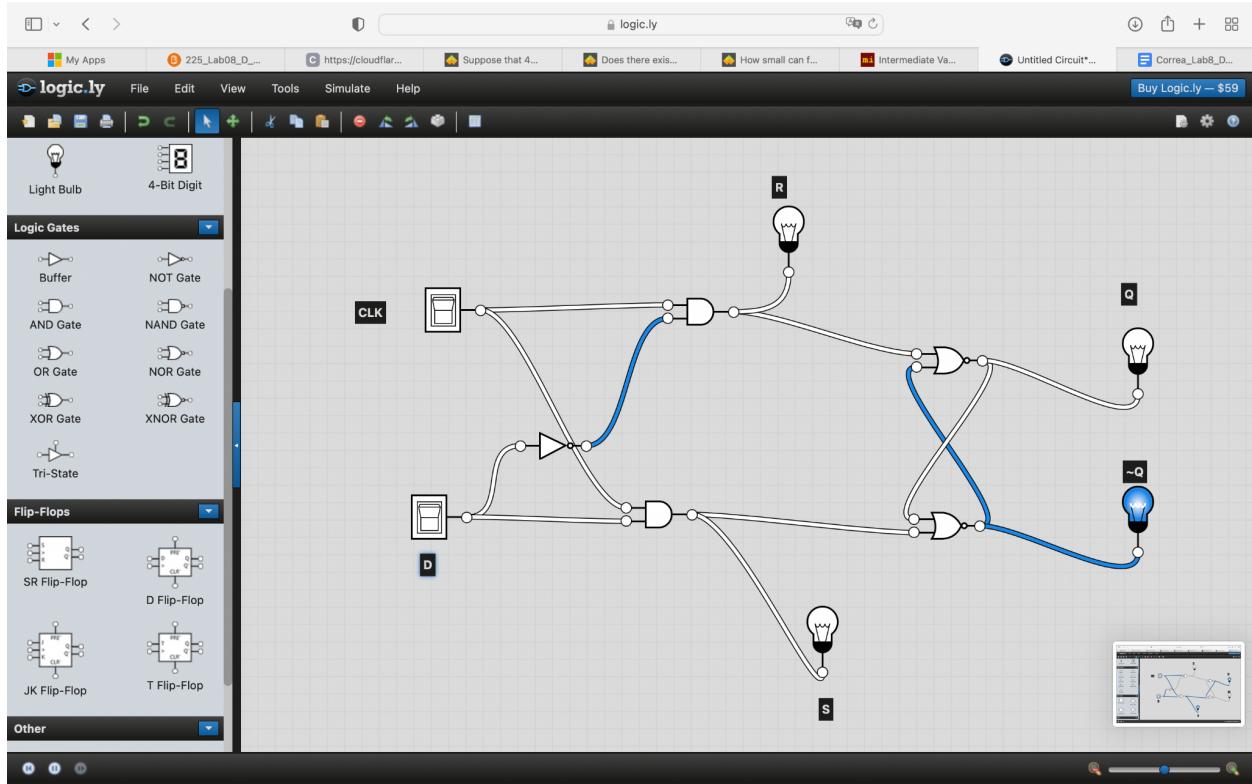
$CLK = 1, D = 0, S = 0, R = 1, Q = 0, \sim Q = 1$



$CLK = 1, D = 1, S = 1, R = 0, Q = 1, \sim Q = 0$



CLK = 0, D = 0, S = 0, R = 0, Q = Qprev, $\sim Q = \sim Q_{prev}$



2. D-FlipFlop

Description: When the D input on the FlipFlop is High D and Q are the same regardless of the CLK. If the D input goes from High to Low D changes while Q stays the same until the next clock rising edge (when clock goes from 0 to 1). When the D input goes from Low to High only D changes while Q stays the same until the next clock rising edge (when clock goes from 0 to 1).