Lab 05: Algebraic Simplification

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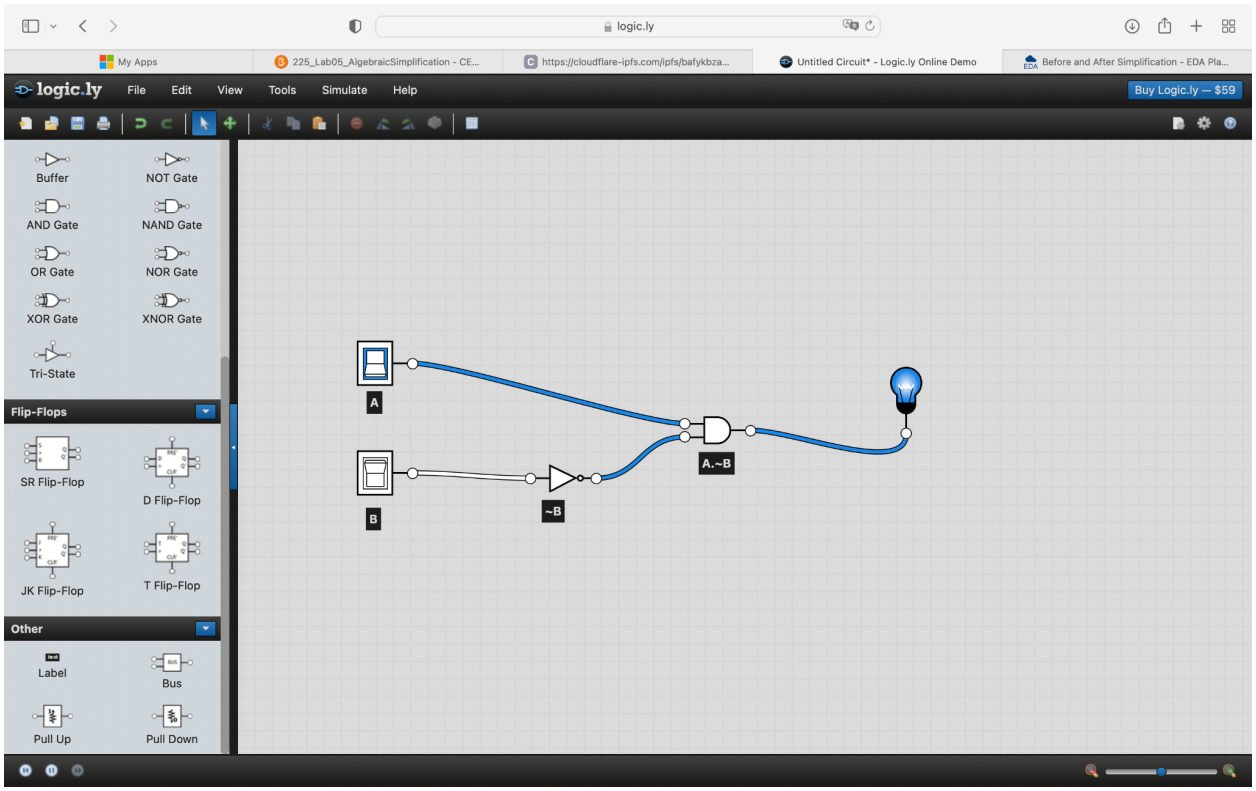
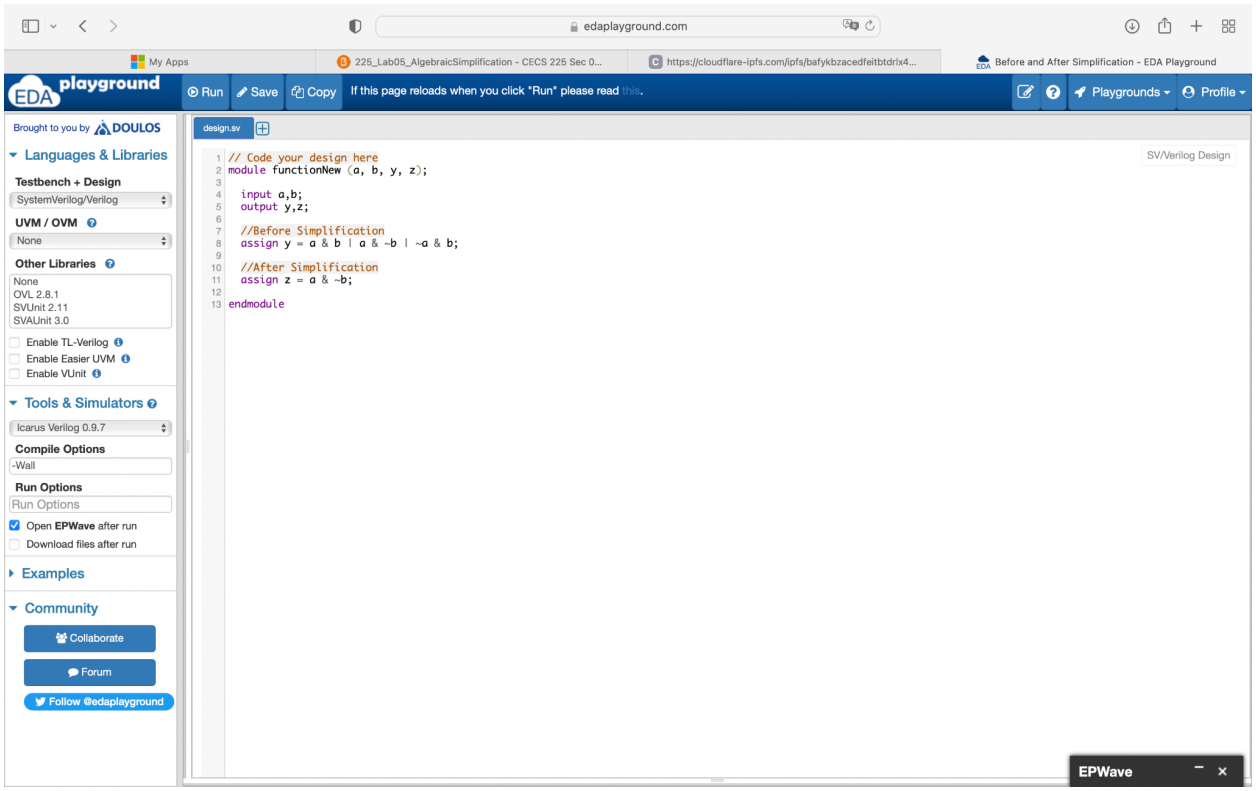
Schematic of Simplified Function:

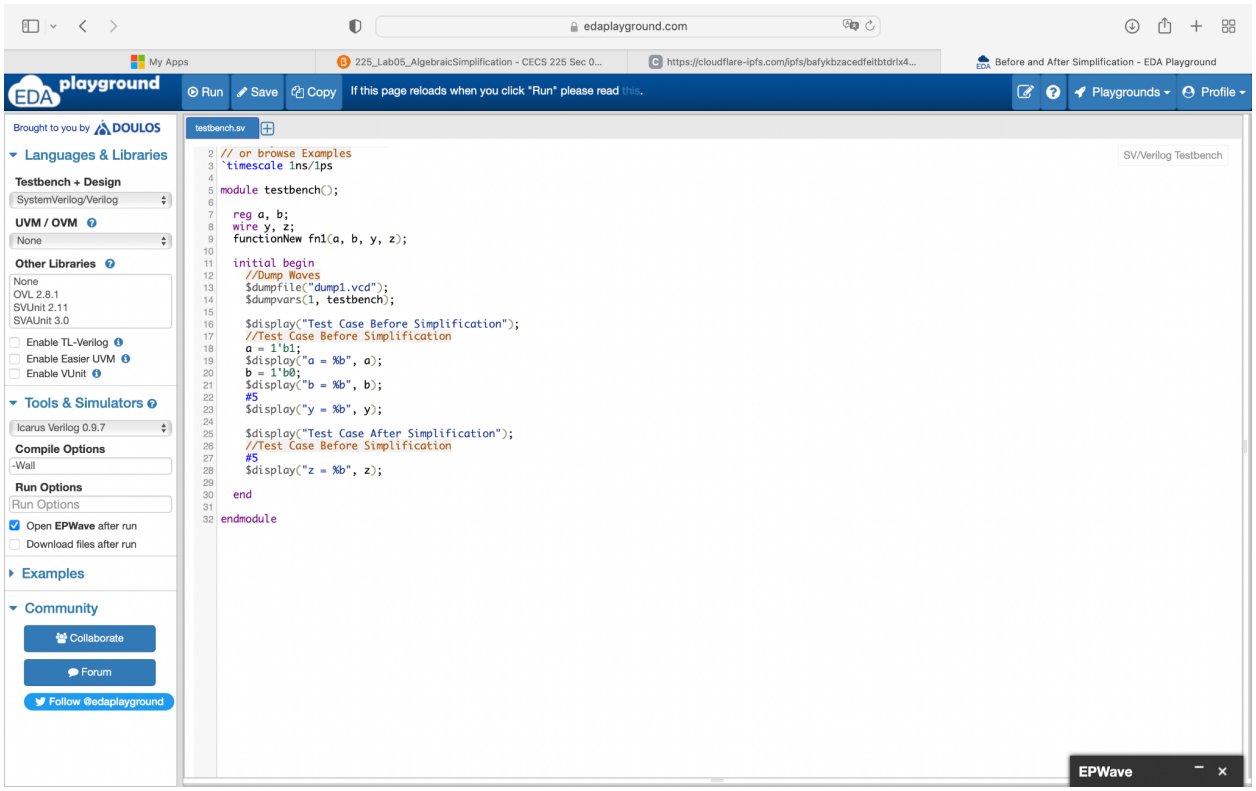


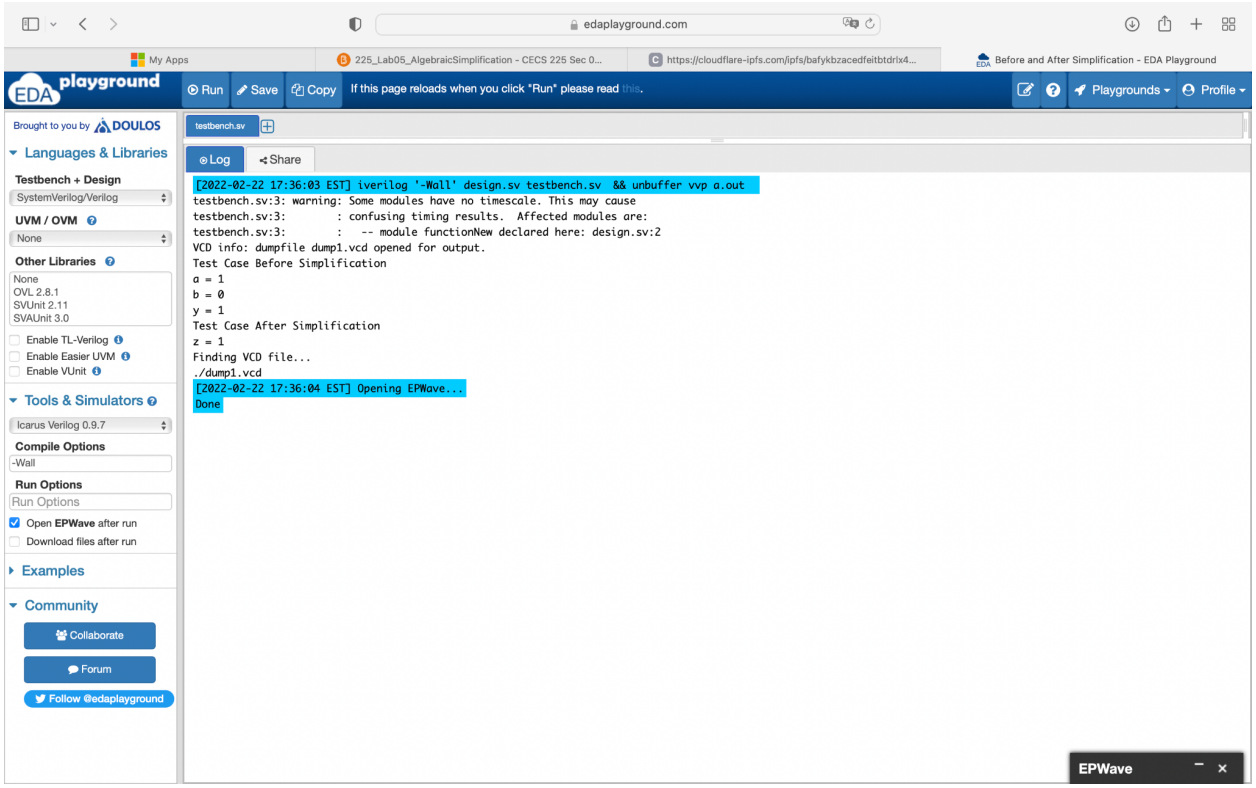
Truth Table of Simplified Function:

A	B	Z
0	0	0
0	1	0
1	0	1
1	1	0

Verilog Code for Simplified and UnSimplified Function:



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Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
SVAUnit 3.0
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Icarus Verilog 0.9.7
Compile Options
-Wall
Run Options
Run Options
Open EPWave after run
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Examples
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testbench.sv
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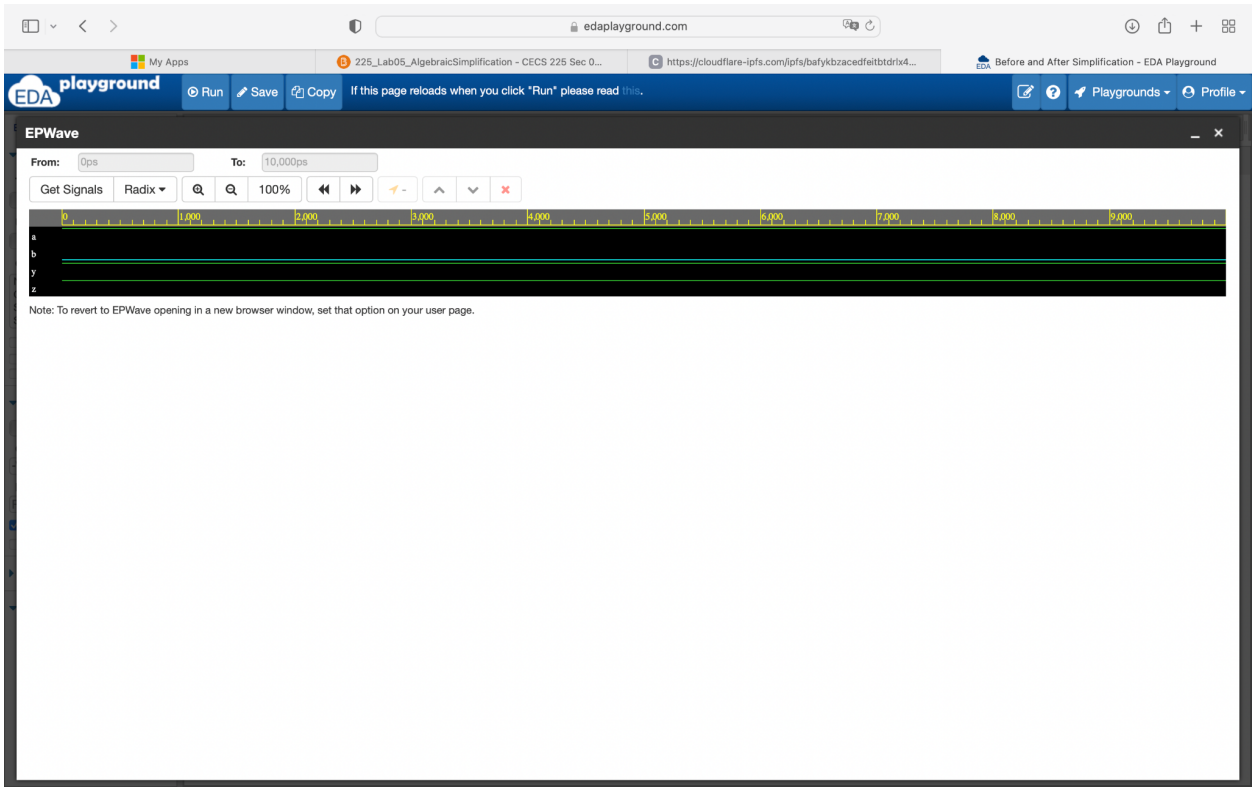
[2022-02-22 17:36:03 EST] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3: : confusing timing results. Affected modules are:
testbench.sv:3: : -- module functionNew declared here: design.sv:2
VCD info: dumpfile dump1.vcd opened for output.
Test Case Before Simplification
a = 1
b = 0
y = 1
Test Case After Simplification
z = 1
Finding VCD file...
./dump1.vcd
[2022-02-22 17:36:04 EST] Opening EPWave...
Done
EPWave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