Lab 06: K Map Simplification

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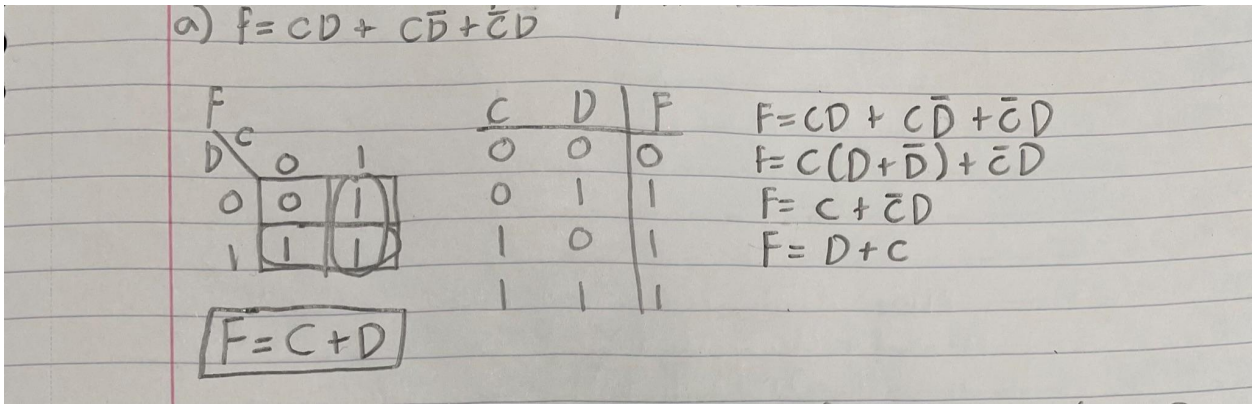
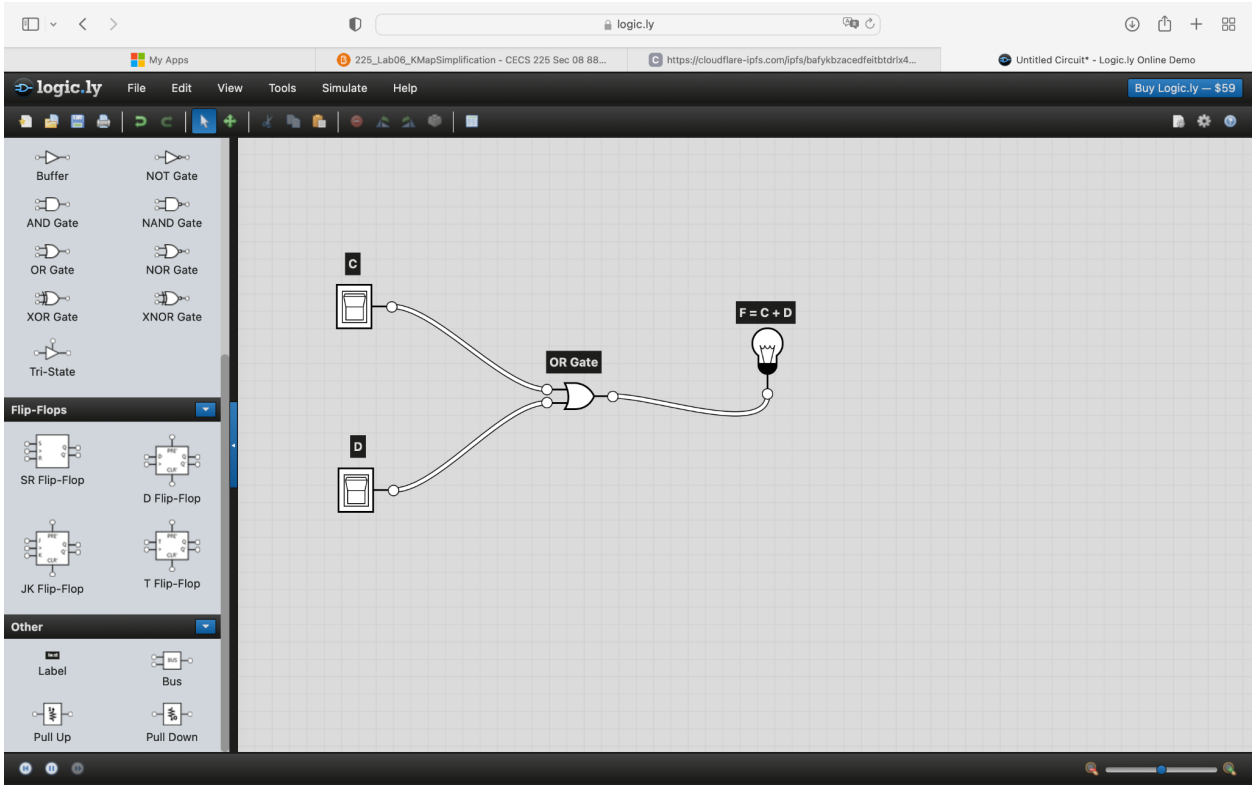
For Assignment Question 1(a):

Algebraic and K-Map Simplification for 1(a)

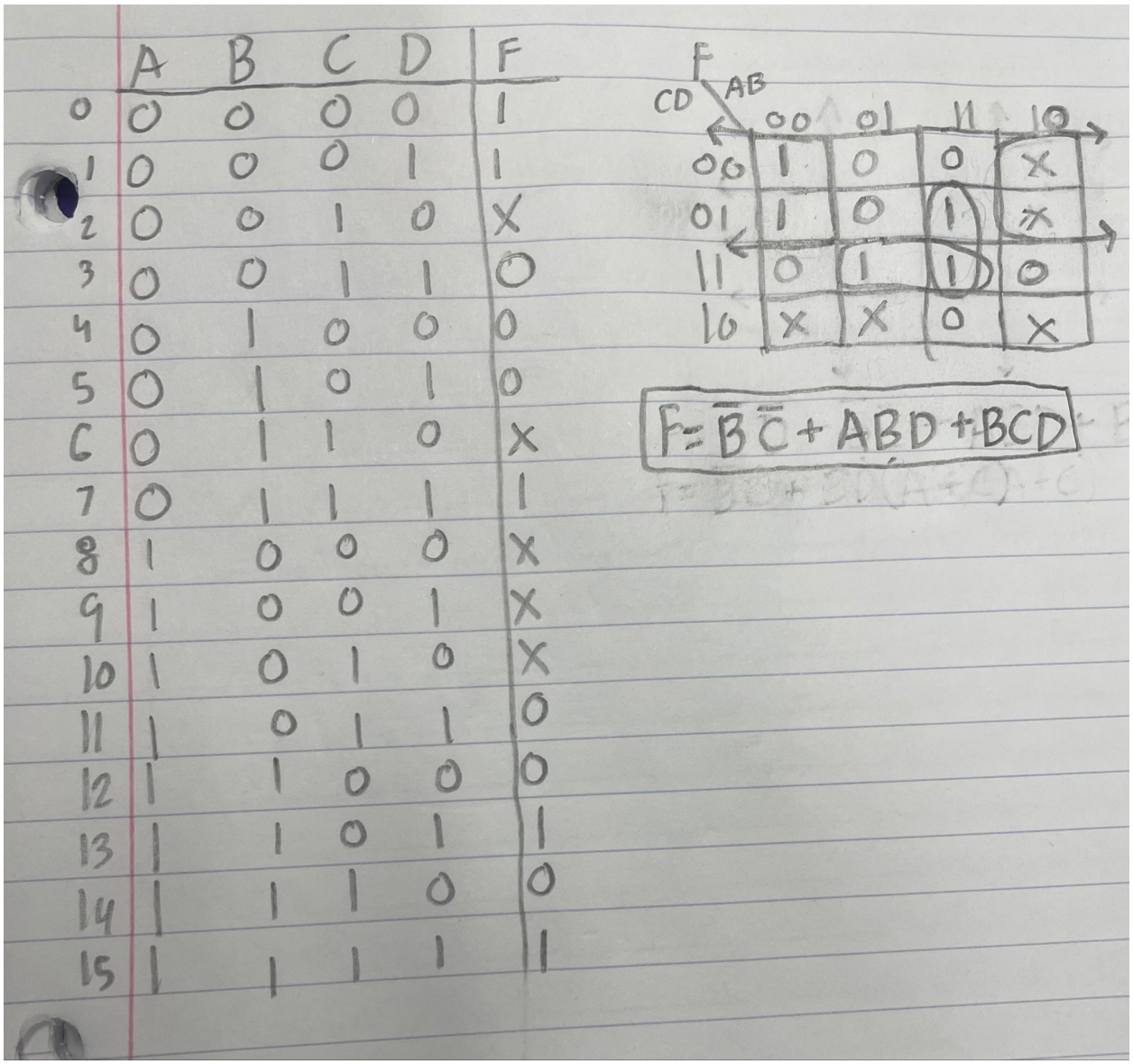


Schematic for 1(a)



For Assignment Question 1(b):

K-Map Simplification for 1(b)



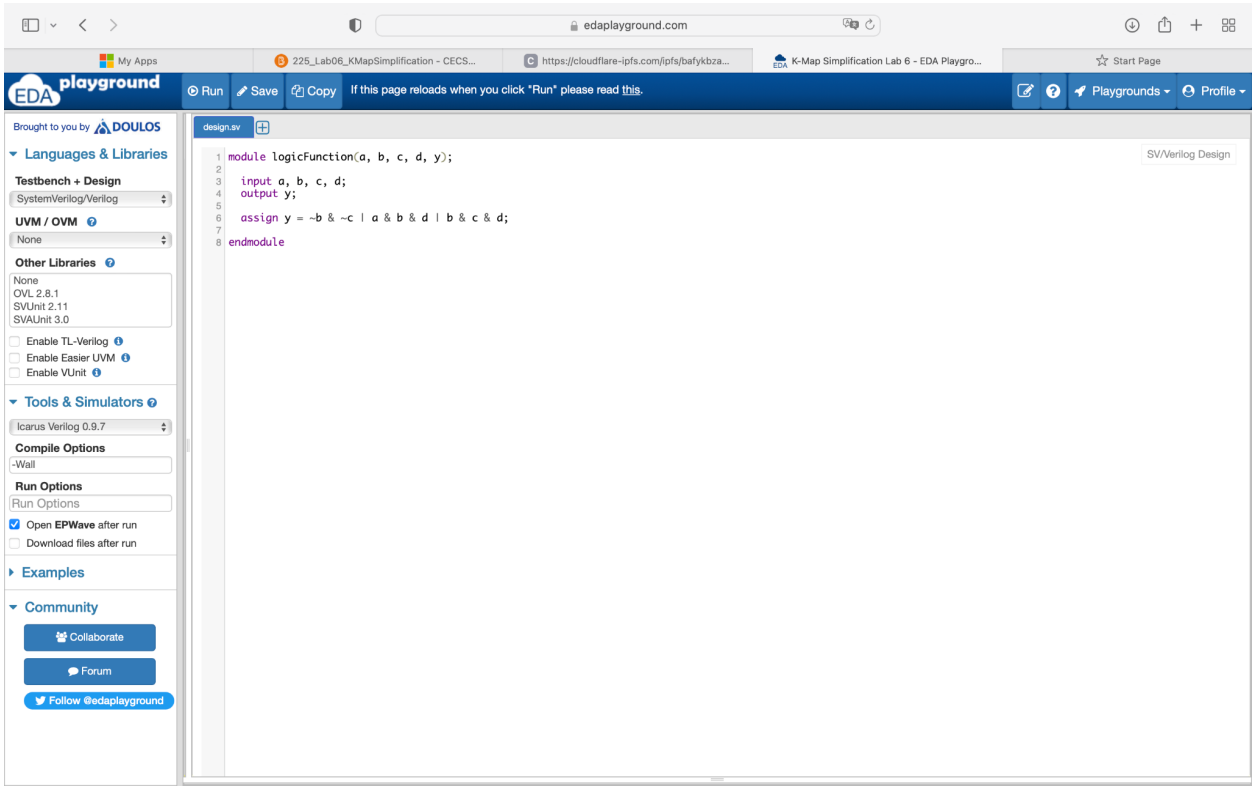
	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	X
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	X
7	0	1	1	1	1
8	1	0	0	0	X
9	1	0	0	1	X
10	1	0	1	0	X
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

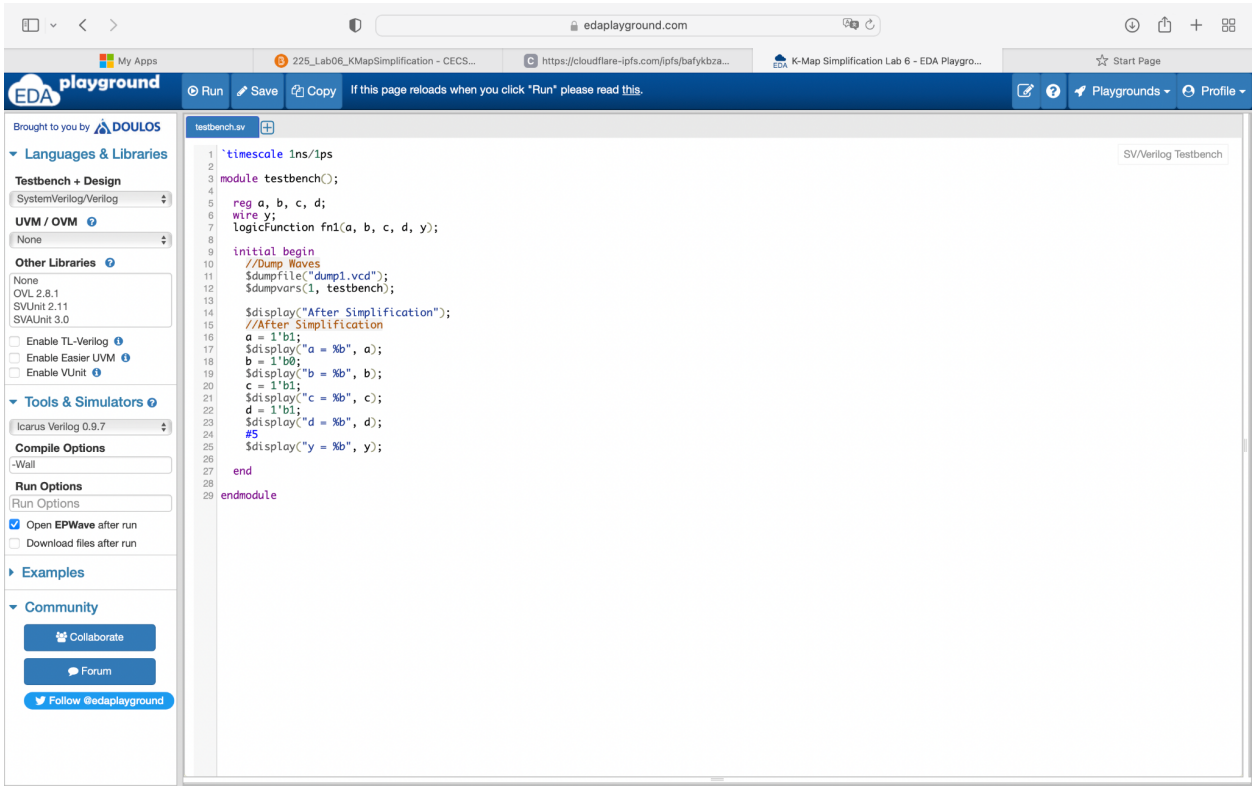
F

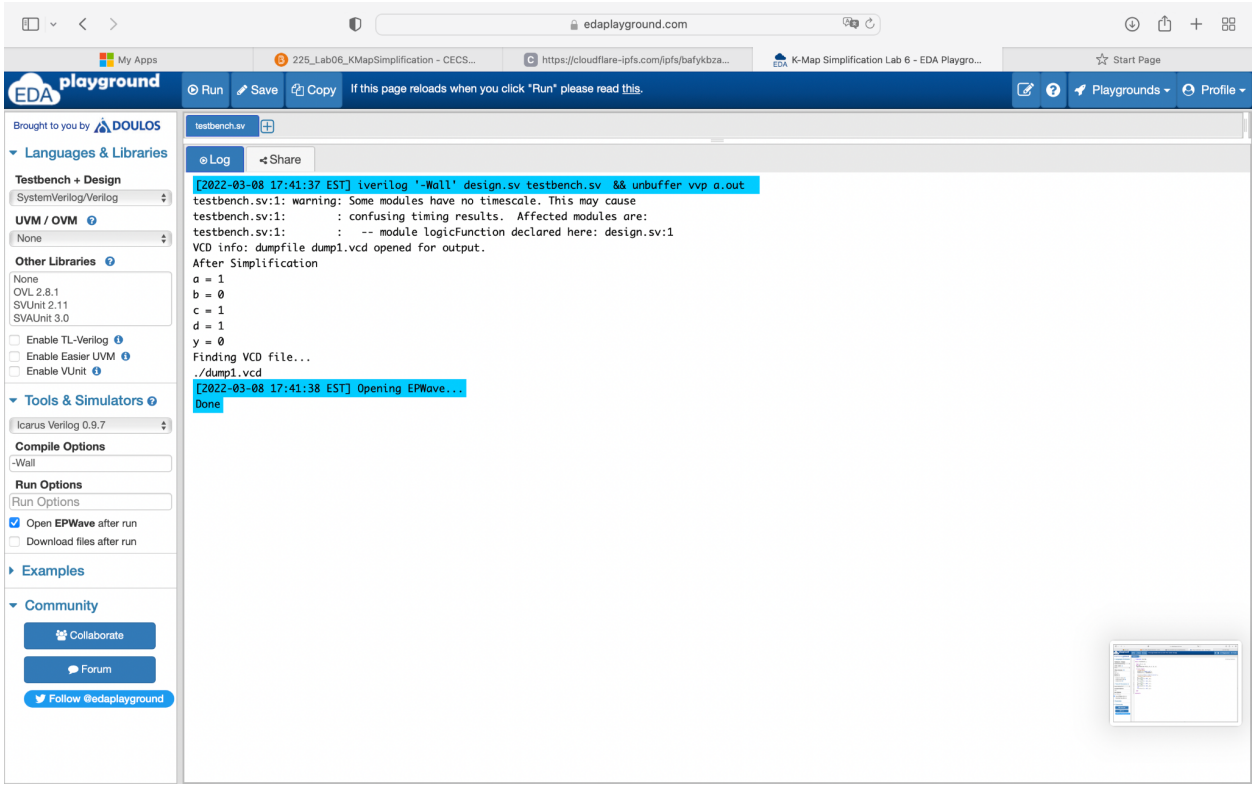
CD \ AB	00	01	11	10
00	1	0	0	X
01	1	0	1	X
11	0	1	1	0
10	X	X	0	X

$F = \bar{B}\bar{C} + ABD + BCD$

Verilog Code for Question 1(b)






edaplayground.com
My Apps
225_Lab06_KMapSimplification - CECS...
https://cloudflare-ipfs.com/ipfs/bafykbza...
K-Map Simplification Lab 6 - EDA Playgro...
Start Page
EDA playground
Run
Save
Copy
If this page reloads when you click "Run" please read this.
Playgrounds
Profile
Brought to you by DOULOS
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
SVAUnit 3.0
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Icarus Verilog 0.9.7
Compile Options
-Wall
Run Options
Run Options
Open EPWave after run
Download files after run
Examples
Community
Collaborate
Forum
Follow @edaplayground
testbench.sv
Log
Share
[2022-03-08 17:41:37 EST] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:1: warning: Some modules have no timescale. This may cause
testbench.sv:1: : confusing timing results. Affected modules are:
testbench.sv:1: : -- module logicFunction declared here: design.sv:1
VCD info: dumpfile dump1.vcd opened for output.
After Simplification
a = 1
b = 0
c = 1
d = 1
y = 0
Finding VCD file...
./dump1.vcd
[2022-03-08 17:41:38 EST] Opening EPWave...
Done