

Lab 07: SR Latch Using NOR and NAND Gates

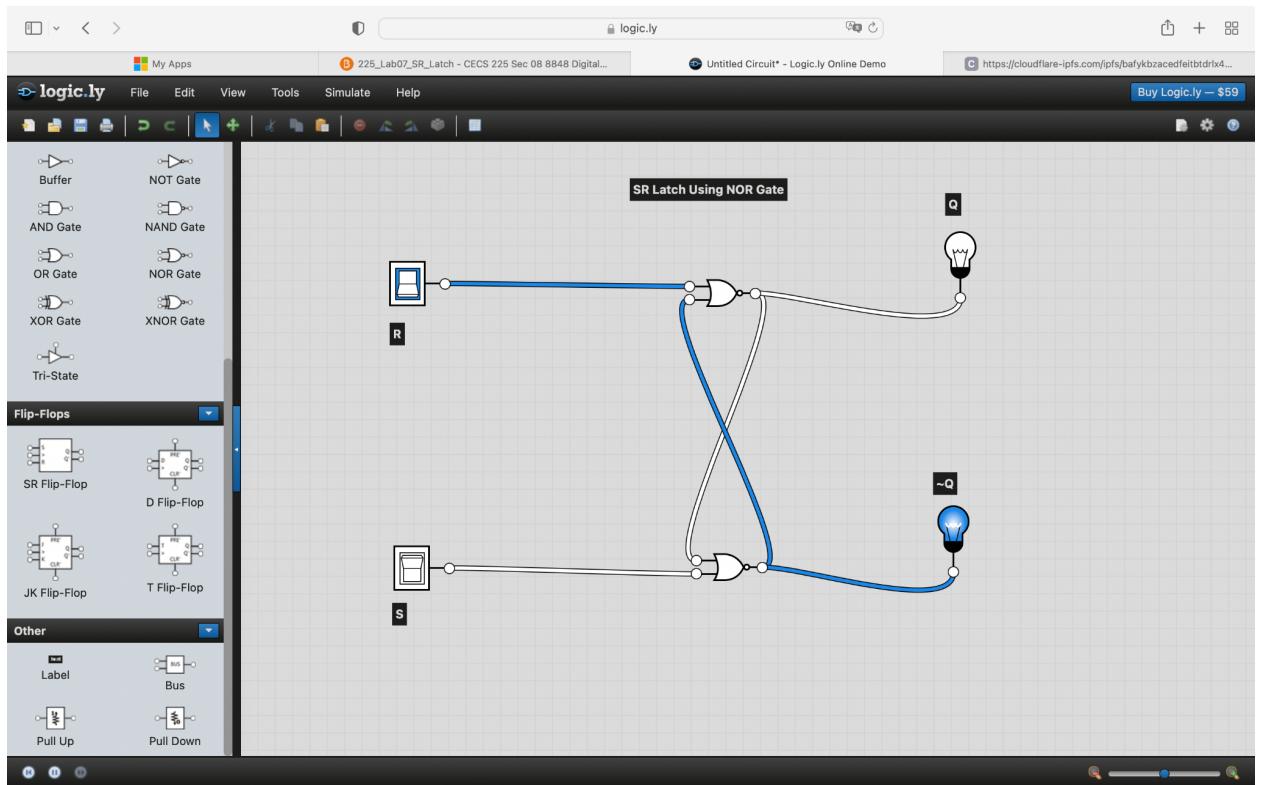
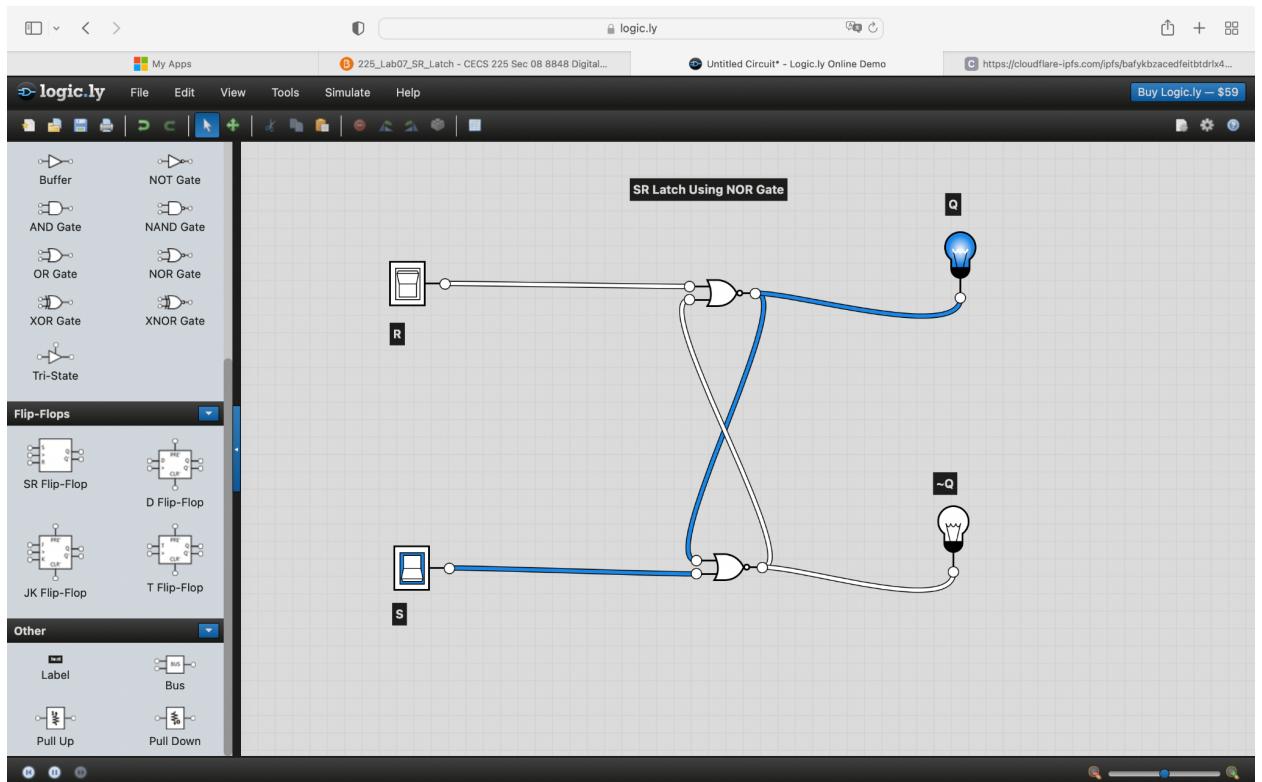
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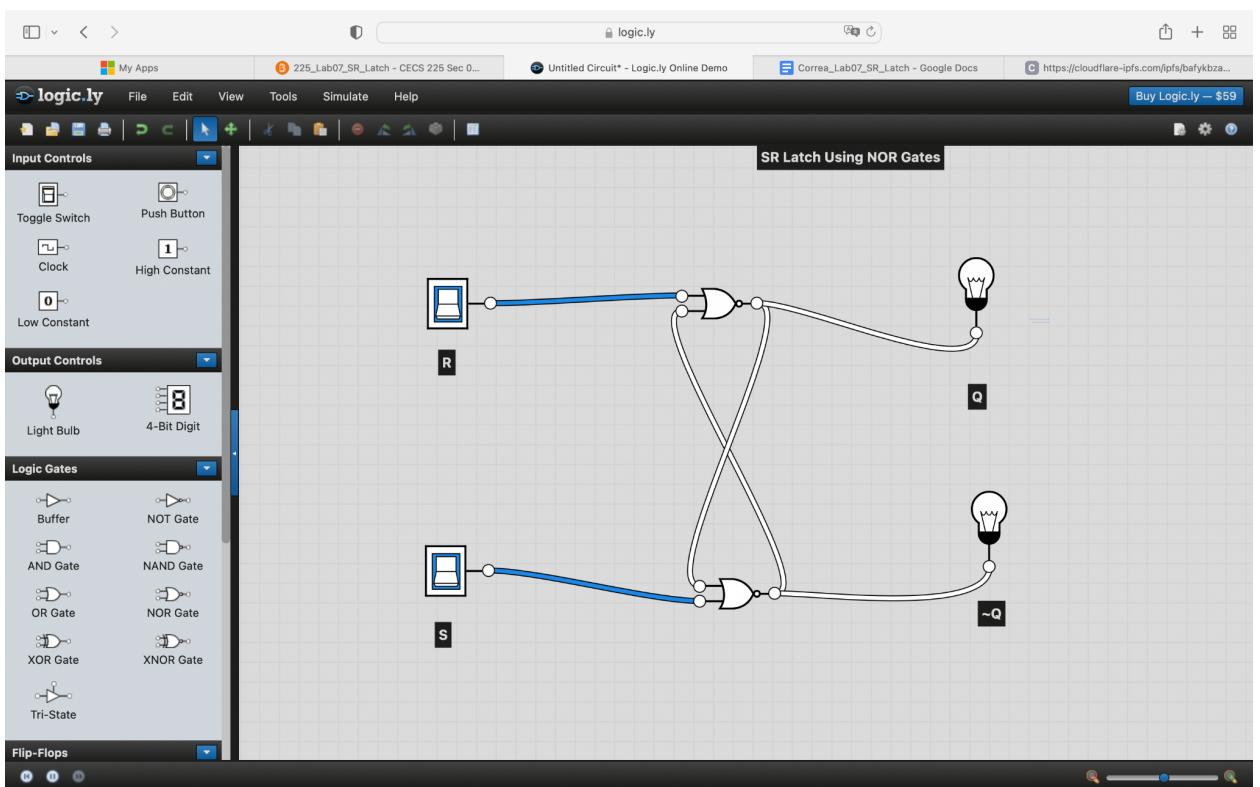
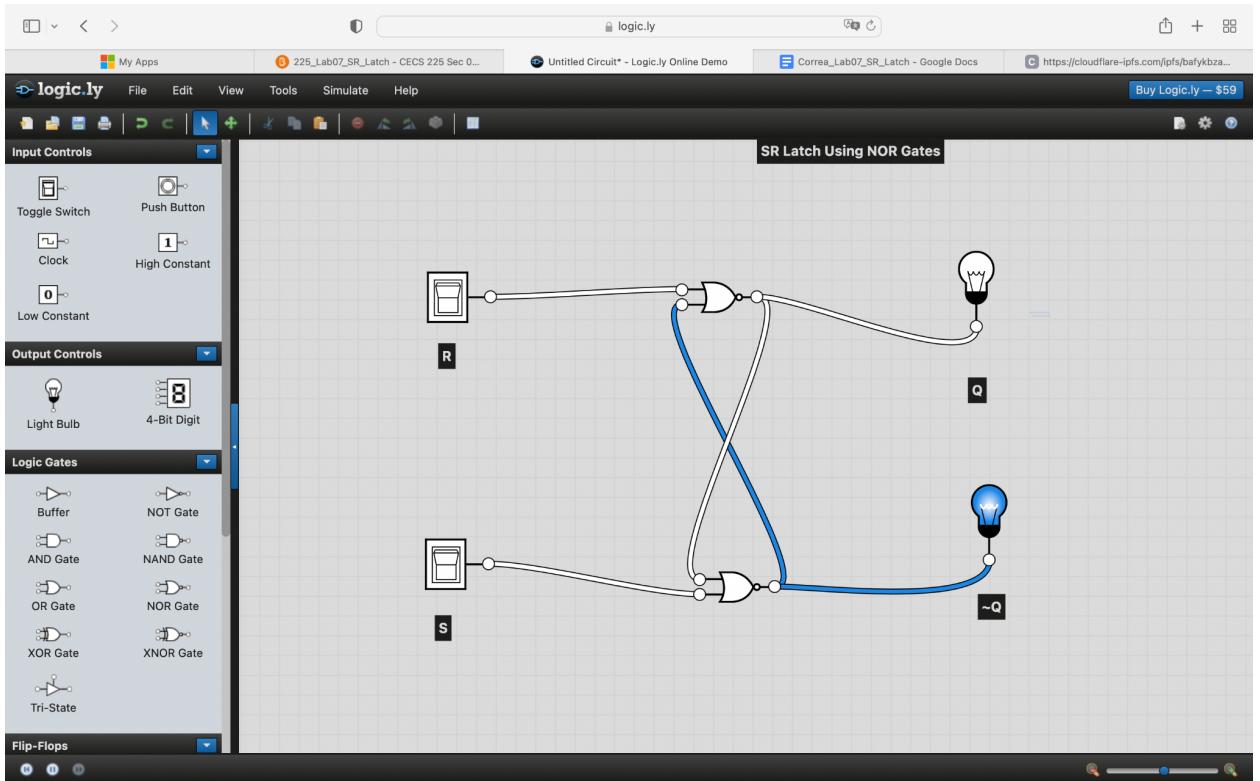
1. NOR Gate

Truth Table

STEPS	S	R	Q	$\sim Q$	Description
Step 1	1	0	1	0	Set Q = 1
Step 2	0	1	0	1	Reset Q = 0
Step 3	0	0	0	1	Memory
Step 4	1	1	0	0	Invalid

Schematics In Order of NOR Gates





2. NAND Gate

Truth Table

Steps	S	R	Q	$\sim Q$	Description
Step 1	1	0	1	0	Set Q = 1
Step 2	0	1	0	1	Reset Q = 0
Step 3	1	1	0	1	Memory
Step 4	0	0	1	1	Invalid

Schematics In order of NAND Gates

