

## Lab 09: Half Adder

CECS 225

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## Section 1: Half Adder Verilog Module Source Code

The screenshot shows the EDA Playground interface with the Half Adder Verilog module source code loaded in the 'design.av' file. The code is as follows:

```
1 module HalfAdder (A, B, Cout, S);
2   input A, B;
3   output Cout, S;
4
5   assign Cout = A & B;
6   assign S = A ^ B;
7
8 endmodule
9
```

The left sidebar shows the 'Languages & Libraries' section with 'SystemVerilog/Verilog' selected. The 'Tools & Simulators' section shows 'Icarus Verilog 0.9.7' selected. The 'Run' button is visible at the top of the editor.

## Section 2: Half Adder Verilog Test Code

The screenshot shows the EDA Playground interface with the Half Adder Verilog test code loaded in the 'testbench.av' file. The code is as follows:

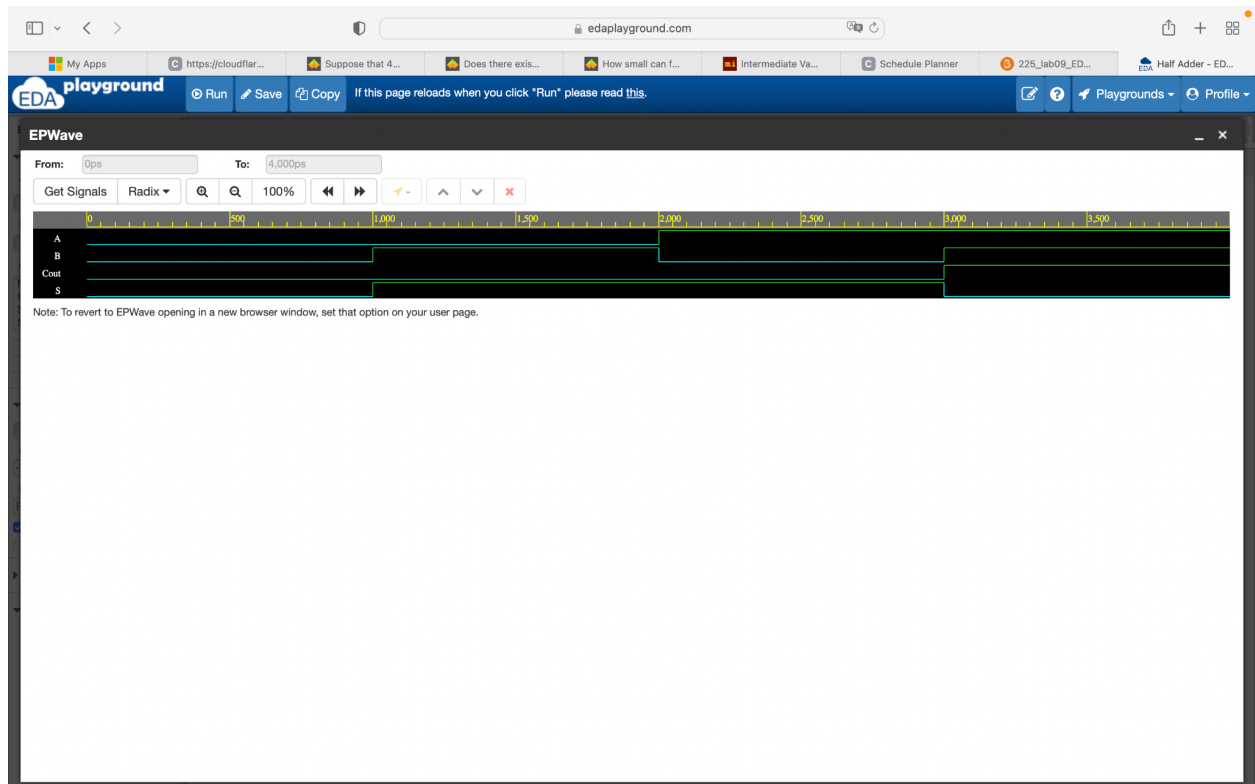
```
1 `timescale 1ns/1ps
2 module testbench();
3   reg A, B;
4   wire Cout, S;
5   HalfAdder HA1(A, B, Cout, S);
6
7   initial begin
8     $dumpfile("dump.vcd");
9     $dumpvars(1, testbench);
10
11     $display("Test Case 0");
12     A = 1'b0; B = 1'b0;
13     $display("A = %b", A, "B = %b", B);
14     #1
15     $display("Cout = %b", Cout, "S = %b", S);
16
17     $display("Test Case 1");
18     A = 1'b0; B = 1'b1;
19     $display("A = %b", A, "B = %b", B);
20     #1
21     $display("Cout = %b", Cout, "S = %b", S);
22
23     $display("Test Case 2");
24     A = 1'b1; B = 1'b0;
25     $display("A = %b", A, "B = %b", B);
26     #1
27     $display("Cout = %b", Cout, "S = %b", S);
28
29     $display("Test Case 3");
30     A = 1'b1; B = 1'b1;
31     $display("A = %b", A, "B = %b", B);
32     #1
33     $display("Cout = %b", Cout, "S = %b", S);
34
35   end
36 endmodule
37
```

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### Section 3: Half Adder Simulation Screenshot showing correct results

The screenshot shows the EDA Playground web interface. The left sidebar contains navigation options: Languages & Libraries, Tools & Simulators, and Community. The main area displays the testbench code for a Half Adder simulation. The code includes a Verilog testbench that defines inputs A and B, and outputs Cout and S. It sets up a simulation with a 10ns timescale and a dumpfile named dump.vcd. The simulation is run using Icarus Verilog 0.9.7. The log output shows the simulation results for four test cases, all of which are correct.

```
testbench.vv
[2022-04-12 21:10:44 UTC] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:1: warning: Some modules have no timescale. This may cause
testbench.sv:1:      : confusing timing results. Affected modules are:
testbench.sv:1:      : -- module HalfAdder declared here: design.sv:1
VCD info: dumpfile dump.vcd opened for output.
Test Case 0
A = 0 B = 0
Cout = 0 S = 0
Test Case 1
A = 0 B = 1
Cout = 0 S = 1
Test Case 2
A = 1 B = 0
Cout = 0 S = 1
Test Case 3
A = 1 B = 1
Cout = 1 S = 0
Finding VCD file...
./dump.vcd
[2022-04-12 21:10:45 UTC] Opening EPWave...
Done
```



#### **Section 4: Short Description Observation**

From what I can see we are adding two binary digits using logic gates. When the number of 1 inputs is odd the S goes to 1, and when all the inputs are 1 the Cout goes to 1. This logic helps replicate the adding of binary digits we learned in Chapter 1.