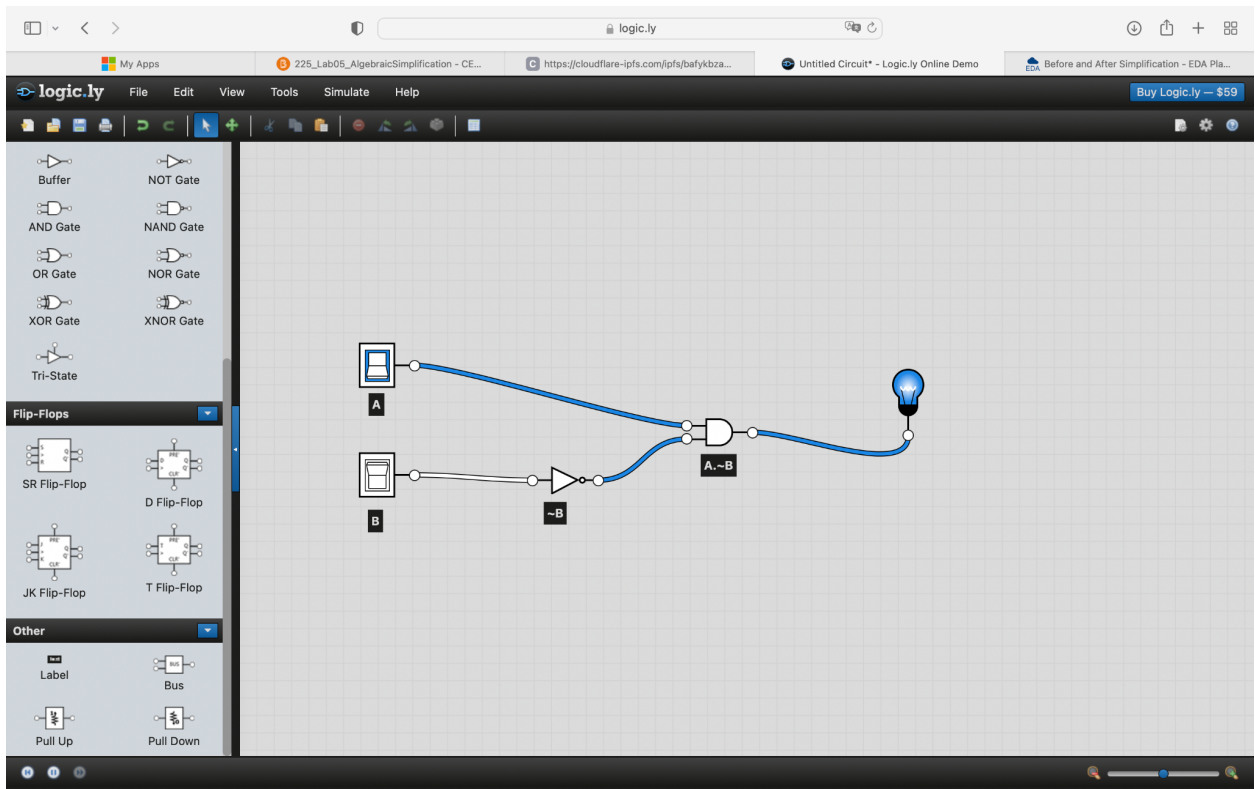


Lab 5: Algebraic Simplification

Lab 05: Algebraic Simplification
Joshua Correa ID: 029196984

Schematic of Simplified Function:



Truth Table of Simplified Function:

A	B	Z
0	0	0
0	1	0
1	0	1
1	1	0

Verilog Code for Simplified and UnSimplified Function:

The screenshot shows the EDA Playground interface. The left sidebar contains navigation options: Languages & Libraries, Testbench + Design, Tools & Simulators, Examples, and Community. The main editor area displays the following Verilog code:

```

1 // Code your design here
2 module functionNew (a, b, y, z);
3
4   input a,b;
5   output y,z;
6
7   //Before Simplification
8   assign y = a & b | a & ~b | ~a & b;
9
10  //After Simplification
11  assign z = a & ~b;
12
13 endmodule

```

The bottom right corner shows an EPWave window icon.

The screenshot shows the EDA Playground interface with the testbench code loaded. The left sidebar is the same as the previous screenshot. The main editor area displays the following Verilog testbench code:

```

2 // or browse Examples
3 timescale 1ns/1ps
4
5 module testbench();
6
7   reg a, b;
8   wire y, z;
9   functionNew fn1(a, b, y, z);
10
11   initial begin
12     //Dump Waves
13     $dumpfile("dump1.vcd");
14     $dumpvars(1, testbench);
15
16     $display("Test Case Before Simplification");
17     //Test Case Before Simplification
18     a = 1'b1;
19     $display("a = %b", a);
20     b = 1'b0;
21     $display("b = %b", b);
22     #5
23     $display("y = %b", y);
24
25     $display("Test Case After Simplification");
26     //Test Case After Simplification
27     #5
28     $display("z = %b", z);
29
30   end
31
32 endmodule

```

The bottom right corner shows an EPWave window icon.

EDA playground

Run Save Copy If this page reloads when you click "Run" please read this.

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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM

None

Other Libraries

None

Enable TL-Verilog

Enable Easier UVM

Enable VUnit

Tools & Simulators

Icarus Verilog 0.9.7

Compile Options

-Wall

Run Options

Run Options

Open EPWave after run

Download files after run

Examples

Community

Collaborate

Forum

Follow @edaplayground

testbench.sv

Log Share

```
[2022-02-22 17:36:03 EST] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3:      : confusing timing results. Affected modules are:
testbench.sv:3:      : -- module functionNew declared here: design.sv:2
VCD info: dumpfile dump1.vcd opened for output.
Test Case Before Simplification
a = 1
b = 0
y = 1
Test Case After Simplification
z = 1
Finding VCD file...
./dump1.vcd
[2022-02-22 17:36:04 EST] Opening EPWave...
Done
```

EPWave

EDA playground

Run Save Copy If this page reloads when you click "Run" please read this.

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Languages & Libraries

Testbench + Design

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UVM / OVM

None

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Test Case After Simplification
z = 1
Finding VCD file...
./dump1.vcd
[2022-02-22 17:36:04 EST] Opening EPWave...
Done
```

EPWave

From: 0ps To: 10,000ps

Get Signals Radix 100%

a

b

y

z

Note: To revert to EPWave opening in a new browser window, set that option on your user page.