

Lab 10: Full Adder

CECS 225

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Section 1: Design Module

EDA

playground

Run

Save

Copy

If this page reloads when you click "Run" please read [this](#).

design.sv

+

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DOULOS

Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM

None

Other Libraries

None

OVL 2.8.1

SVAUnit 2.11

SVAUnit 3.0

☐ Enable TL-Verilog
 ☐ Enable Easier UVM
 ☐ Enable VUnit

Tools & Simulators

Icarus Verilog 0.9.7

Compile Options

-Wall

Run Options

Run Options

☒ Open EPWave after run
 ☐ Download files after run

Examples

Community

Collaborate

Forum

Follow @edaplayground

225_lab10_EDAPlayground_Full Adder ~...

https://cloudflare-ips.com/ips/bafykbza...

Full Adder - EDA Playground

Start Page

Playgrounds

Profile

```

1 // Code your design here
2 module HalfAdder(A, B, Cout, S);
3   input A, B;
4   output Cout, S;
5
6   assign Cout = A & B;
7   assign S = A ^ B;
8
9 endmodule
10
11 module FullAdder (Cin, FA_A, FA_B, FA_S, FA_Cout);
12   input FA_A, FA_B, Cin;
13   output FA_S, FA_Cout;
14
15   wire ha0_S, ha0_C, ha1_C;
16
17   HalfAdder ha0 (
18     .A(FA_A),
19     .B(FA_B),
20     .Cout(ha0_C),
21     .S(ha0_S)
22   );
23
24   HalfAdder ha1 (
25     .A(Cin),
26     .B(ha0_S),
27     .Cout(ha1_C),
28     .S(FA_S)
29   );
30
31   assign FA_Cout = ha0_C | ha1_C; //Carry-out for full adder
32 endmodule

```

SV/Verilog Design

EPWave

Section 2: Testbench Module

The screenshot displays the EDA Playground web application. The top navigation bar includes links for "My Apps", "Full Adder - EDA Playground", "Start Page", "Playgrounds", and "Profile". The main interface is divided into several sections:

- Left Sidebar:** Contains tabs for "Languages & Libraries", "Tools & Simulators", "Examples", and "Community". Under "Languages & Libraries", there are options for "Testbench + Design" (SystemVerilog/Verilog), "UVM / OVM", and "Other Libraries".
- Main Editor Area:** Displays a Verilog testbench code file named "testbench.v". The code defines a module "timescale 1ns/1ps" and "module testbench()". It sets up signals "FA_A1", "FA_B1", "Cin1", "FA_S1", and "FA_Cout1". A "FullAdder FA1" component is instantiated with inputs "Cin1", "FA_A1", and "FA_B1", and outputs "FA_S1" and "FA_Cout1". The code includes multiple test cases (0 through 6) where specific input values are assigned and displayed.
- Right Panel:** Shows the "SV/Verilog Testbench" tab.
- Bottom Bar:** Includes a status bar indicating "EPWave" and a close button.

Section 3: Outputs

The screenshot shows the EDA Playground web interface. The left sidebar contains navigation options like 'Languages & Libraries', 'Tools & Simulators', and 'Community'. The main area displays the testbench output log for a Verilog simulation. The log shows a warning about missing timescale, followed by test case results for Cin, FA_A, FA_B, FA_Cout, and FA_S. The output ends with 'Opening EPWave...' and 'Done'.

```

[2022-04-19 21:50:06 UTC] verilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:1: warning: Some modules have no timescale. This may cause
testbench.sv:1:   : confusing timing results. Affected modules are:
testbench.sv:1:   :   -- module FullAdder declared here: design.sv:11
testbench.sv:1:   :   -- module HalfAdder declared here: design.sv:2
VCD info: dumpfile dump.vcd opened for output.
Test Case 0
Cin = 0  FA_A = 0  FA_B = 0
FA_Cout = 0  FA_S = 0
Test Case 1
Cin = 0  FA_A = 0  FA_B = 1
FA_Cout = 0  FA_S = 1
Test Case 2
Cin = 0  FA_A = 1  FA_B = 0
FA_Cout = 0  FA_S = 1
Test Case 3
Cin = 0  FA_A = 1  FA_B = 1
FA_Cout = 1  FA_S = 0
Test Case 4
Cin = 1  FA_A = 0  FA_B = 0
FA_Cout = 0  FA_S = 1
Test Case 5
Cin = 1  FA_A = 0  FA_B = 1
FA_Cout = 1  FA_S = 0
Test Case 6
Cin = 1  FA_A = 1  FA_B = 0
FA_Cout = 1  FA_S = 0
Test Case 7
Cin = 1  FA_A = 1  FA_B = 1
FA_Cout = 1  FA_S = 1
Finding VCD file...
./dump.vcd
[2022-04-19 21:50:08 UTC] Opening EPWave...
Done
  
```

At the bottom right, a small EPWave window is visible, showing a timing diagram.

Section 4: EP Wave

The screenshot shows the EPWave window, which displays a timing diagram. The top bar includes controls for 'From' and 'To' time, 'Get Signals', 'Radix', and zoom settings. The main area shows waveforms for Cin, FA_A, FA_B, FA_Cout, and FA_S. The time axis ranges from 0 to 7,000 ps. A note at the bottom states: 'Note: To revert to EPWave opening in a new browser window, set that option on your user page.'

At the bottom right, a small EPWave window is visible, showing a timing diagram.

