Lab 1: Inverter

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Description (Inverter): When you input into an inverter, your output will be the negation of your input. For example, if you input 1 your output will be 0, and if you input 0 your output will be 1.

Truth table of Inverter:

Input (A)	Output (Y)
0	1
1	0

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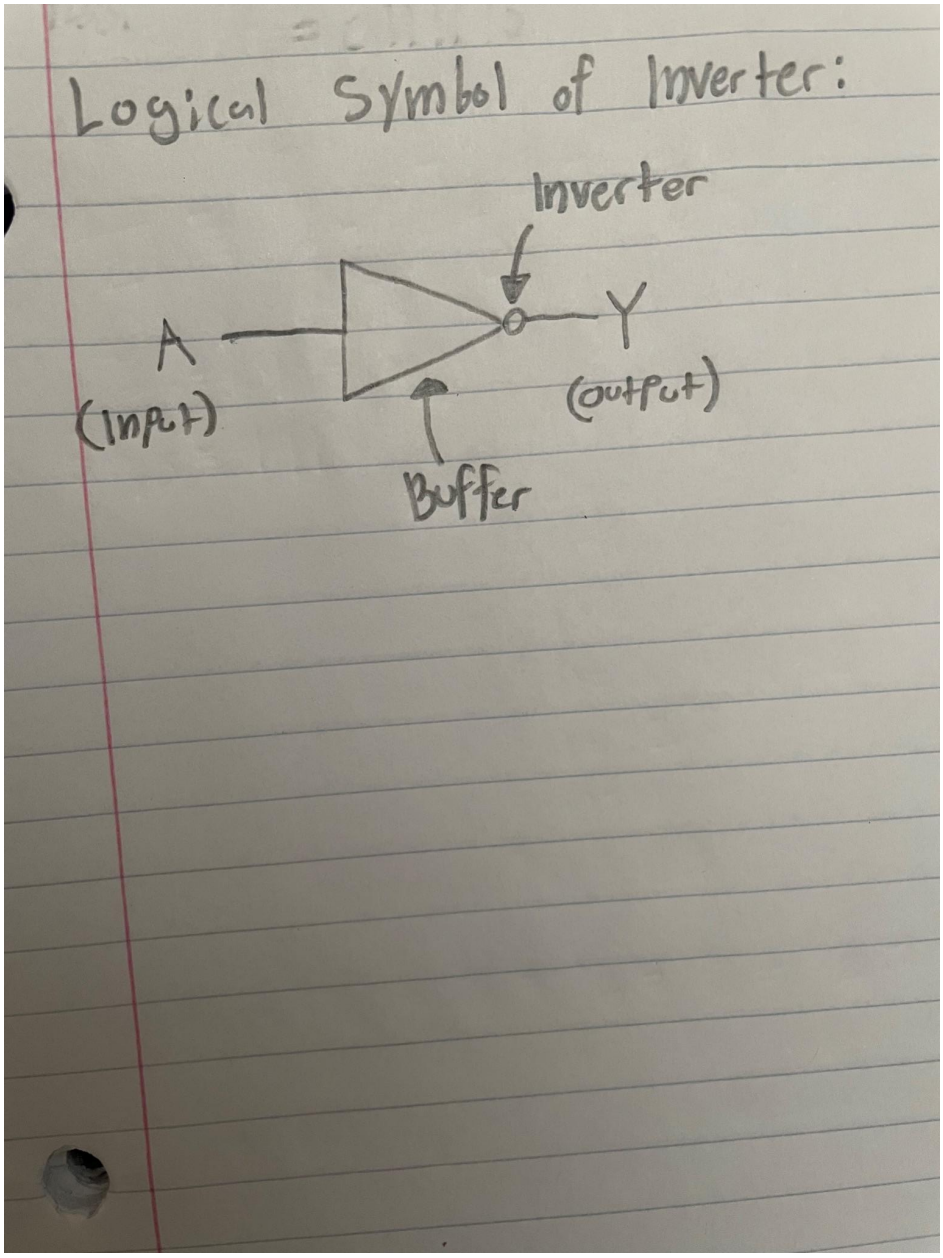
Logical Symbol of Inverter:



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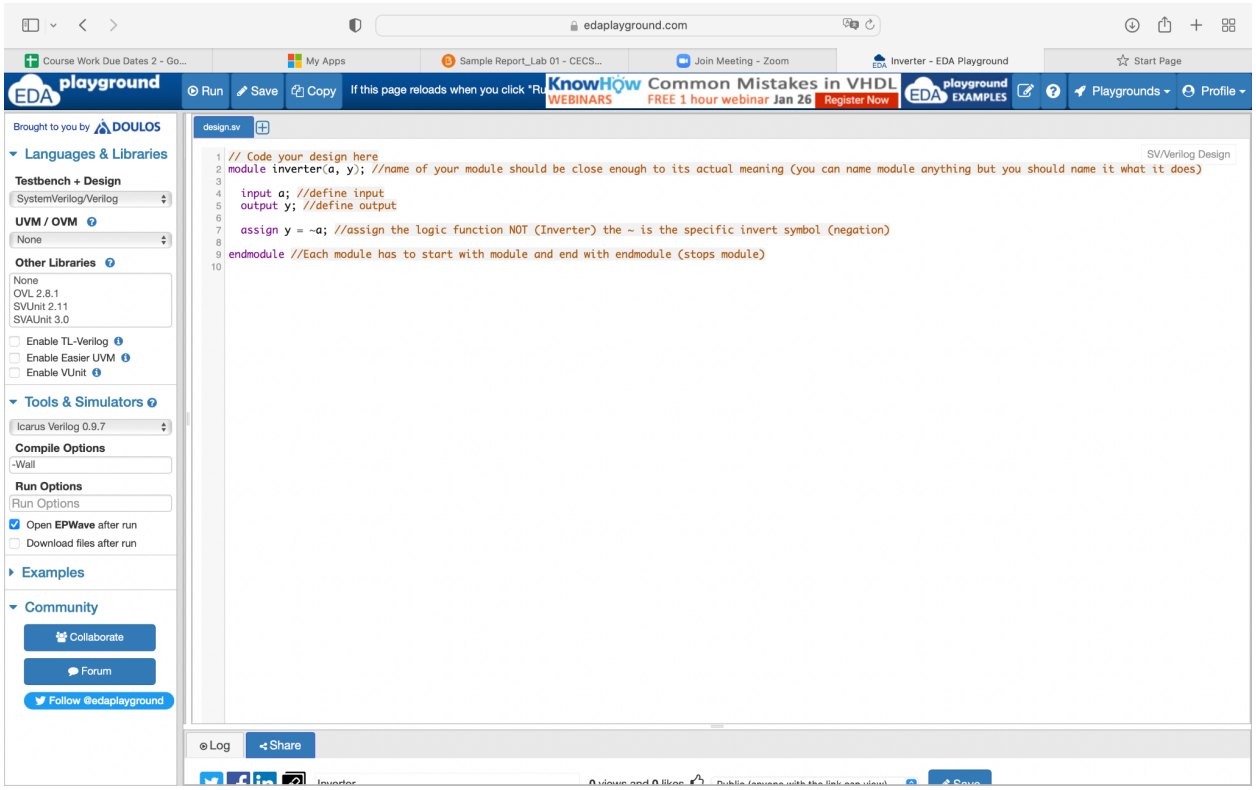
Inverter Verilog Code



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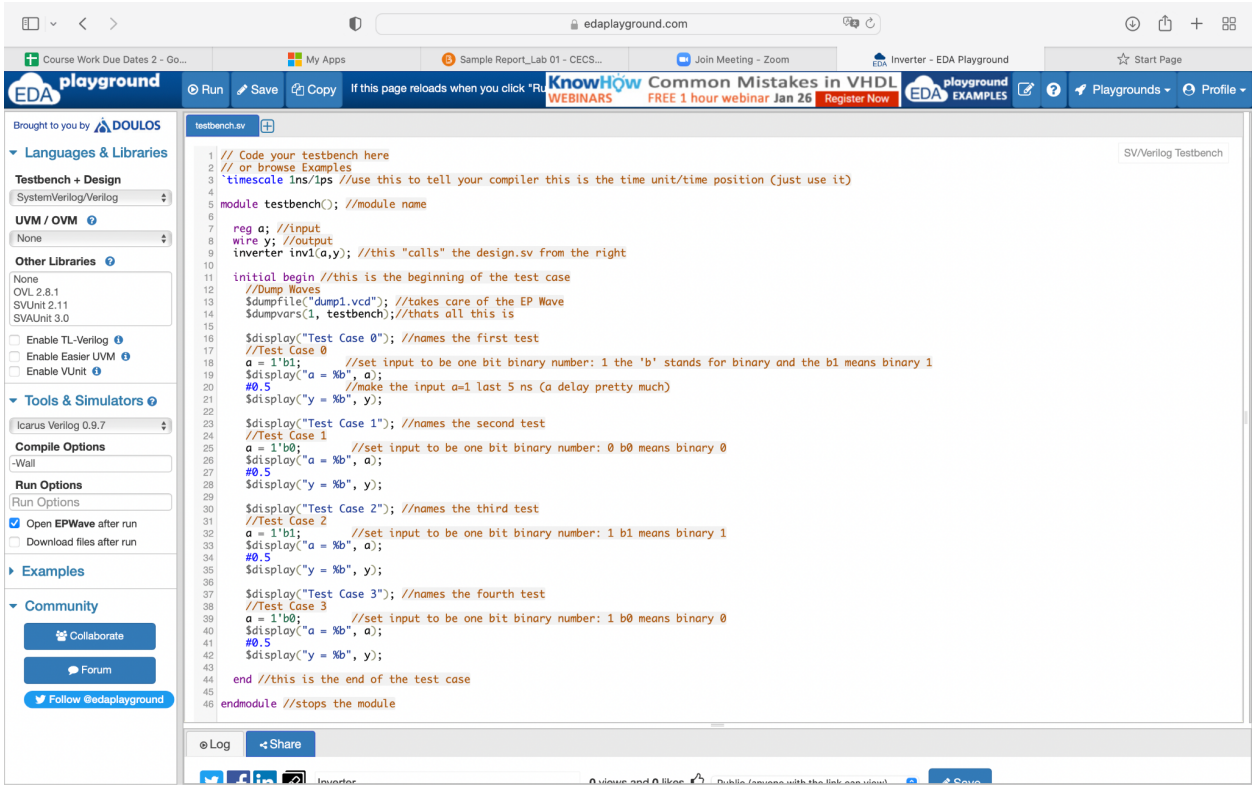

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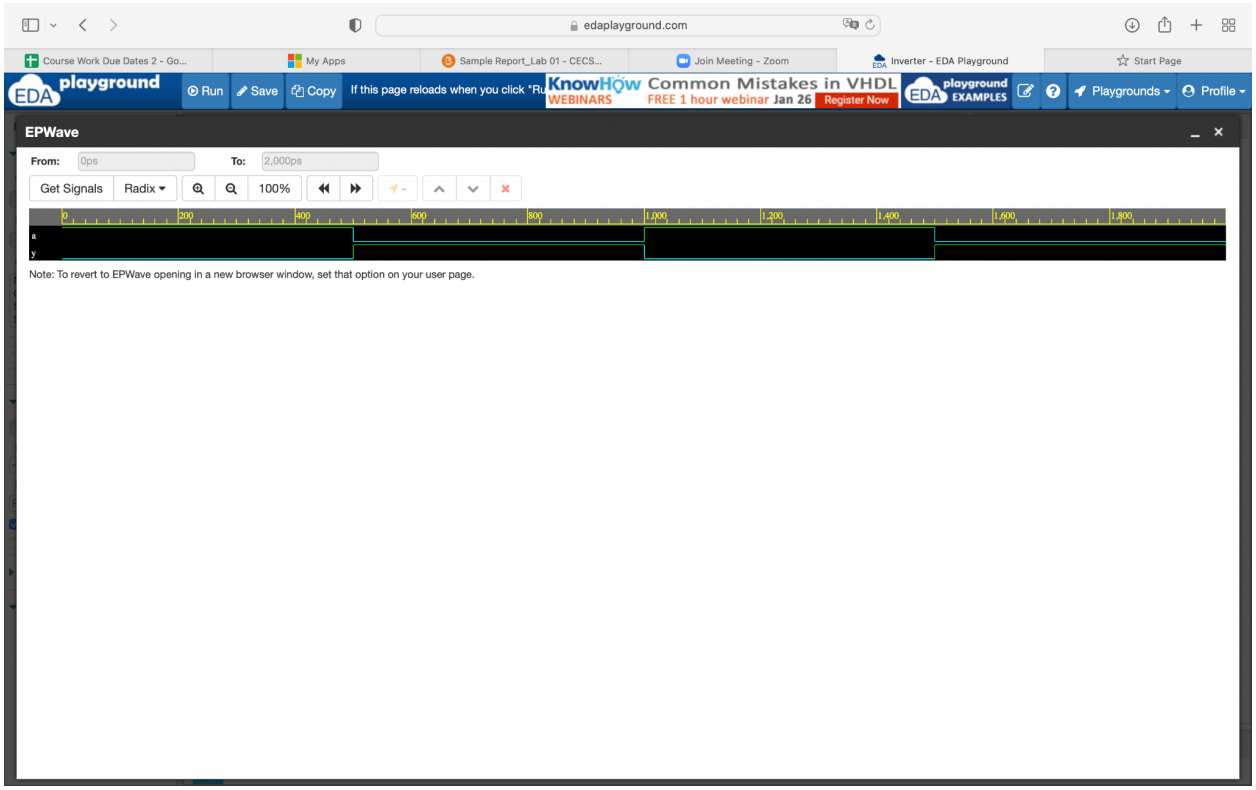
Simulator Waveform



Description: In the Simulator Waveform you can see that every 500ps the input(a) and output(y) invert from each other, so if they are close now, in 500ps they will separate and vice versa.