

Lab 1: Inverter

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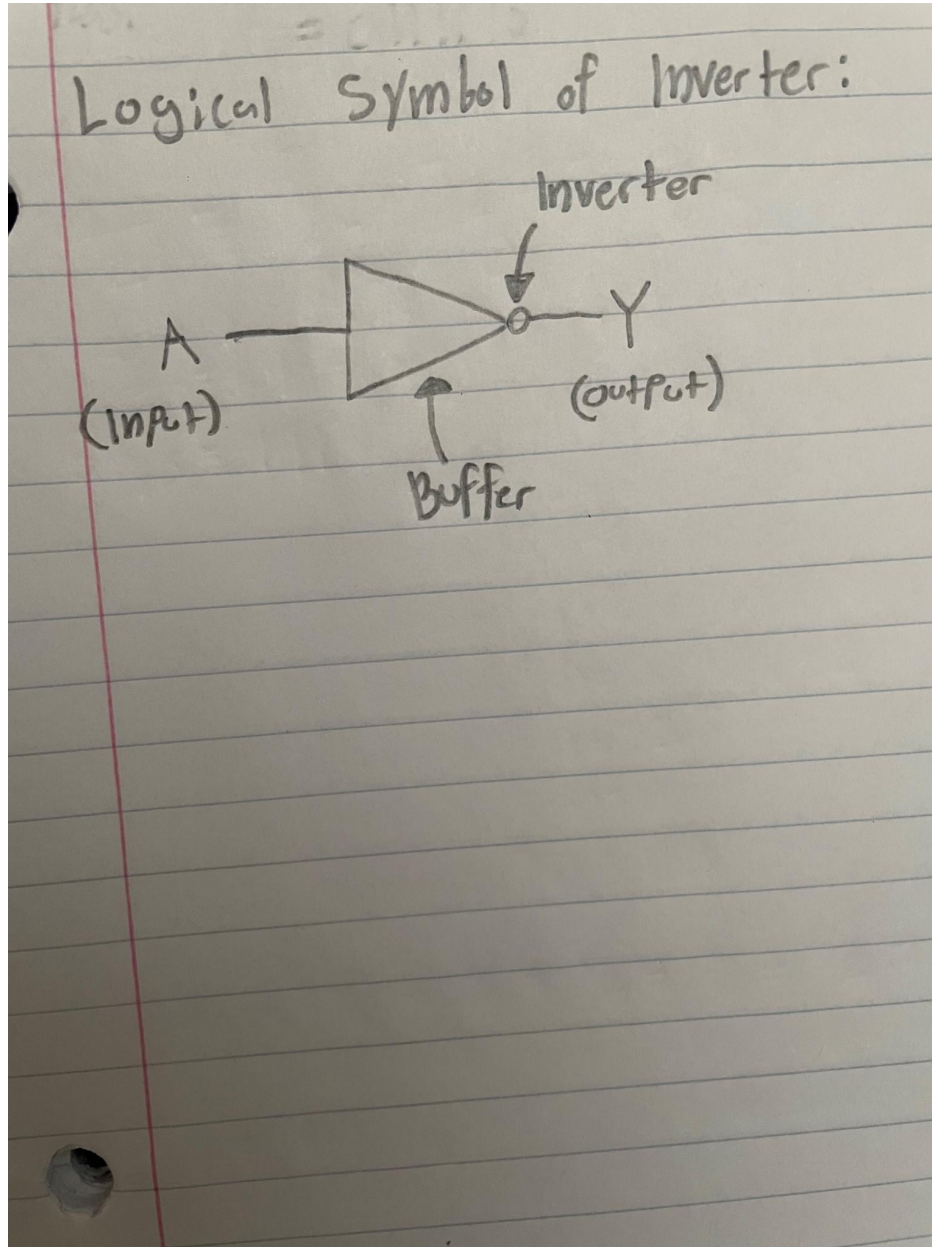
Description (Inverter): When you input into an inverter, your output will be the negation of your input. For example, if you input 1 your output will be 0, and if you input 0 your output will be 1.

Truth table of Inverter:

Input (A)	Output (Y)
0	1
1	0

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Logical Symbol of Inverter:



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Inverter Verilog Code

The screenshot displays the EDA Playground web interface. The browser address bar shows 'edaplayground.com'. The top navigation bar includes 'Run', 'Save', 'Copy', and a notification 'If this page reloads when you click "Run"'. A banner for 'KnowHow WEBINARS' is visible, advertising a 'Common Mistakes in VHDL' webinar on Jan 26. The left sidebar contains a 'Languages & Libraries' section with 'Testbench + Design' (SystemVerilog/Verilog), 'UVM / OVM', and 'Other Libraries'. The 'Tools & Simulators' section shows 'Icarus Verilog 0.9.7'. The 'Compile Options' section has a '-Wall' option. The 'Run Options' section has a 'Run Options' button. The 'Community' section includes 'Collaborate', 'Forum', and 'Follow @edaplayground'. The main code editor area, titled 'design.sv', contains the following Verilog code:

```
1 // Code your design here
2 module inverter(a, y); //name of your module should be close enough to its actual meaning (you can name module anything but you should name it what it does)
3
4   input a; //define input
5   output y; //define output
6
7   assign y = ~a; //assign the logic function NOT (Inverter) the ~ is the specific invert symbol (negation)
8
9 endmodule //Each module has to start with module and end with endmodule (stops module)
10
```

At the bottom of the editor, there are 'Log' and 'Share' buttons. The footer includes social media links and a 'Download and Upload' button.

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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM

None

Other Libraries

None

OVL 2.8.1

SVUnit 2.11

SVAUnit 3.0

Enable TL-Verilog

Enable Easier UVM

Enable VUnit

Tools & Simulators

Icarus Verilog 0.9.7

Compile Options

-Wall

Run Options

Run Options

Open EPWave after run

Download files after run

Examples

Community

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testbench.sv

SV/Verilog Testbench

```
1 // Code your testbench here
2 // or browse Examples
3 timescale 1ns/1ps //use this to tell your compiler this is the time unit/time position (just use it)
4
5 module testbench(); //module name
6
7 reg a; //input
8 wire y; //output
9 inverter inv1(a,y); //this "calls" the design.sv from the right
10
11 initial begin //this is the beginning of the test case
12 //Dump Waves
13 $dumpfile("dump1.vcd"); //takes care of the EP Wave
14 $dumpvars(1, testbench); //thats all this is
15
16 $display("Test Case 0"); //names the first test
17 //Test Case 0
18 a = 1'b1; //set input to be one bit binary number: 1 the 'b' stands for binary and the b1 means binary 1
19 $display("a = %b", a);
20 #0.5 //make the input a=1 last 5 ns (a delay pretty much)
21 $display("y = %b", y);
22
23 $display("Test Case 1"); //names the second test
24 //Test Case 1
25 a = 1'b0; //set input to be one bit binary number: 0 b0 means binary 0
26 $display("a = %b", a);
27 #0.5
28 $display("y = %b", y);
29
30 $display("Test Case 2"); //names the third test
31 //Test Case 2
32 a = 1'b1; //set input to be one bit binary number: 1 b1 means binary 1
33 $display("a = %b", a);
34 #0.5
35 $display("y = %b", y);
36
37 $display("Test Case 3"); //names the fourth test
38 //Test Case 3
39 a = 1'b0; //set input to be one bit binary number: 1 b0 means binary 0
40 $display("a = %b", a);
41 #0.5
42 $display("y = %b", y);
43
44 end //this is the end of the test case
45
46 endmodule //stops the module
```

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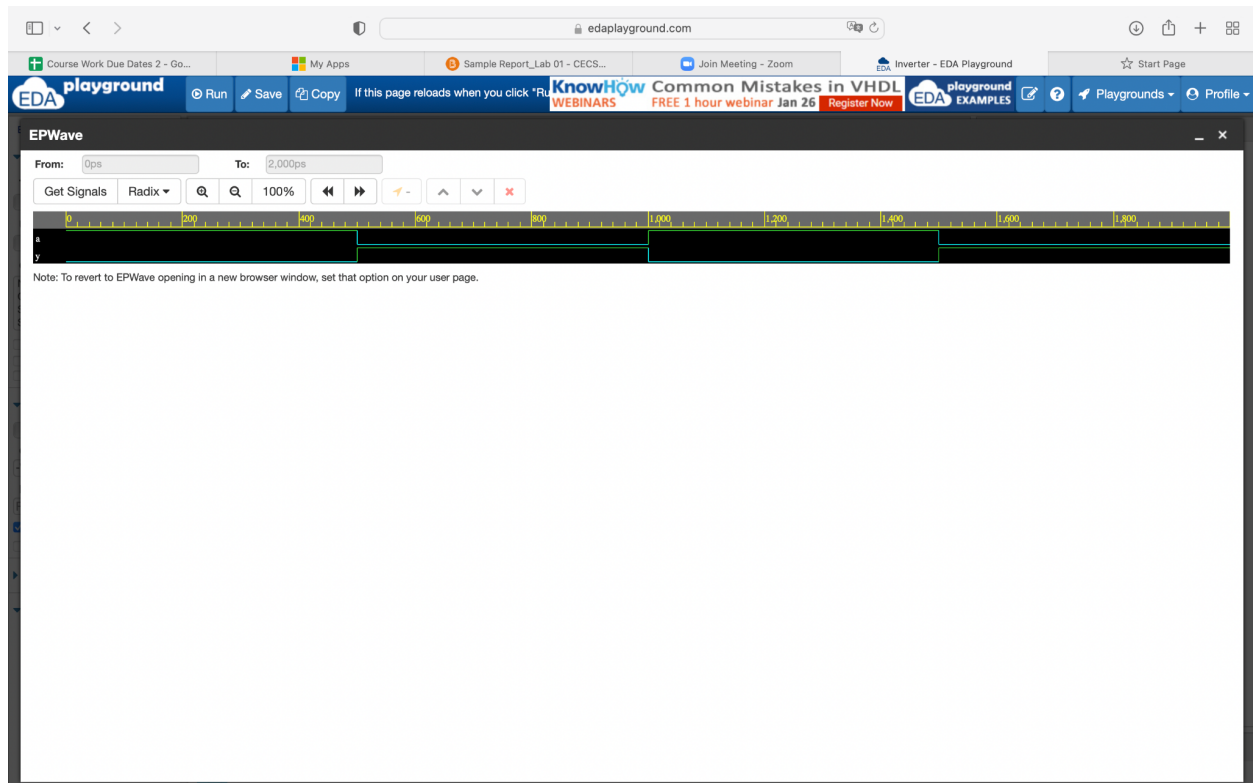
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Save

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Simulator Waveform



Description: In the Simulator Waveform you can see that every 500ps the input(a) and output(y) invert from each other, so if they are close now, in 500ps they will separate and vice versa.