

Lab 2: Using Simulator

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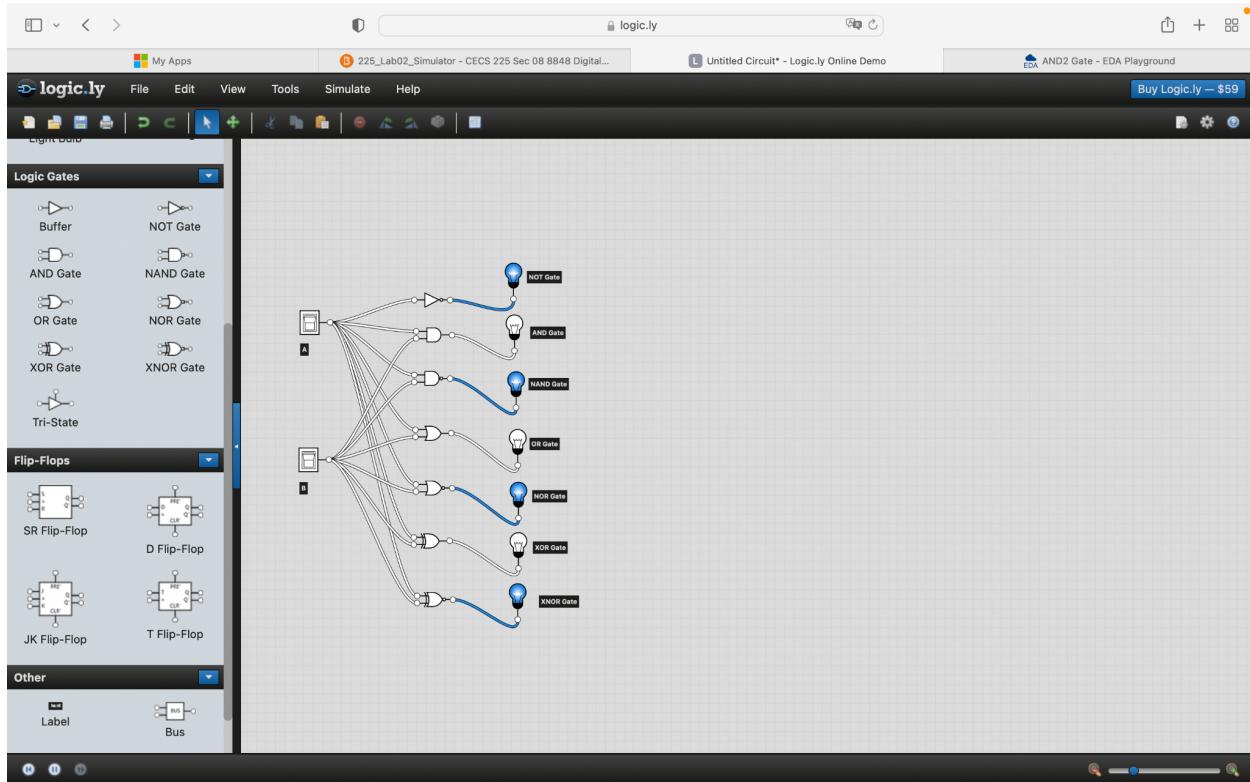
Lab 2: Using Simulator

Truth Table for Logic Gates:

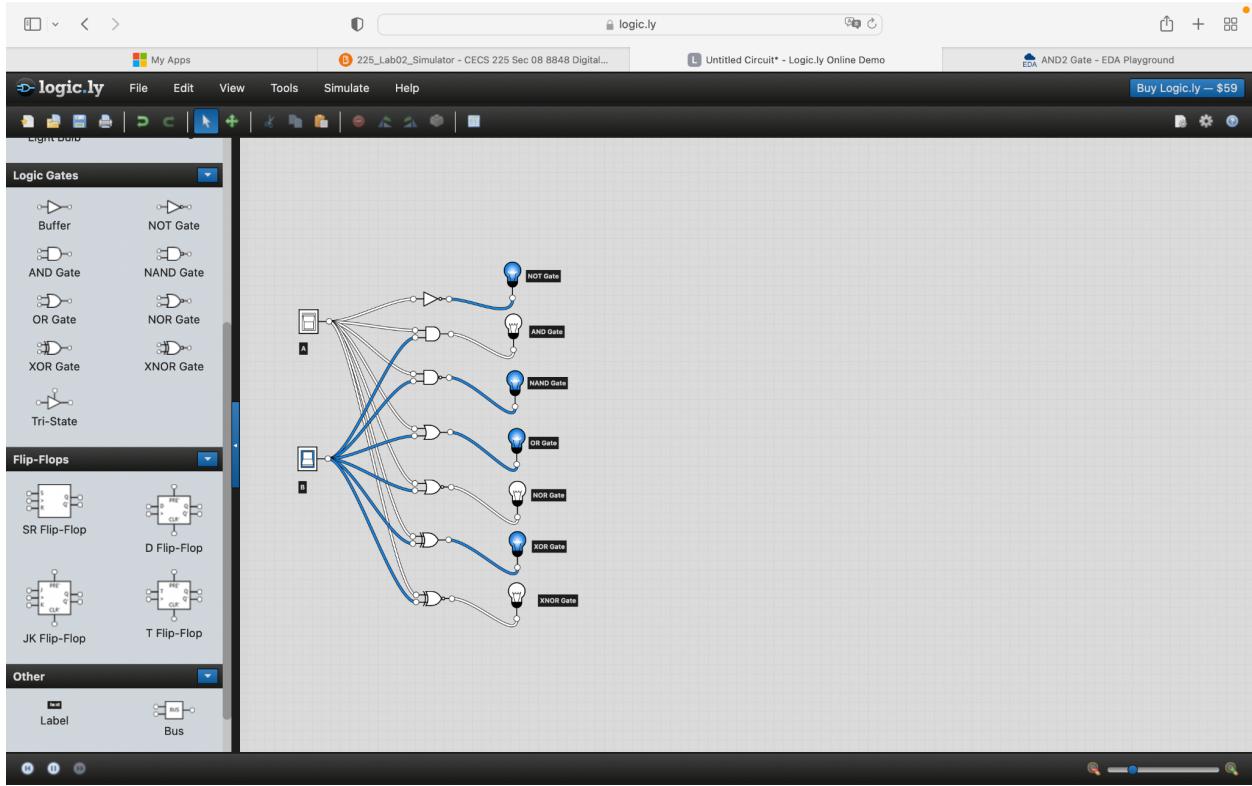
A	B	AND	OR	NAND	NOR	NOT	XOR	XNOR
0	0	0	0	1	1	1	0	1
0	1	0	1	1	0	1	1	0
1	0	0	1	1	0	0	1	0
1	1	1	1	0	0	0	0	1

Schematics Visualizing Truth Table:

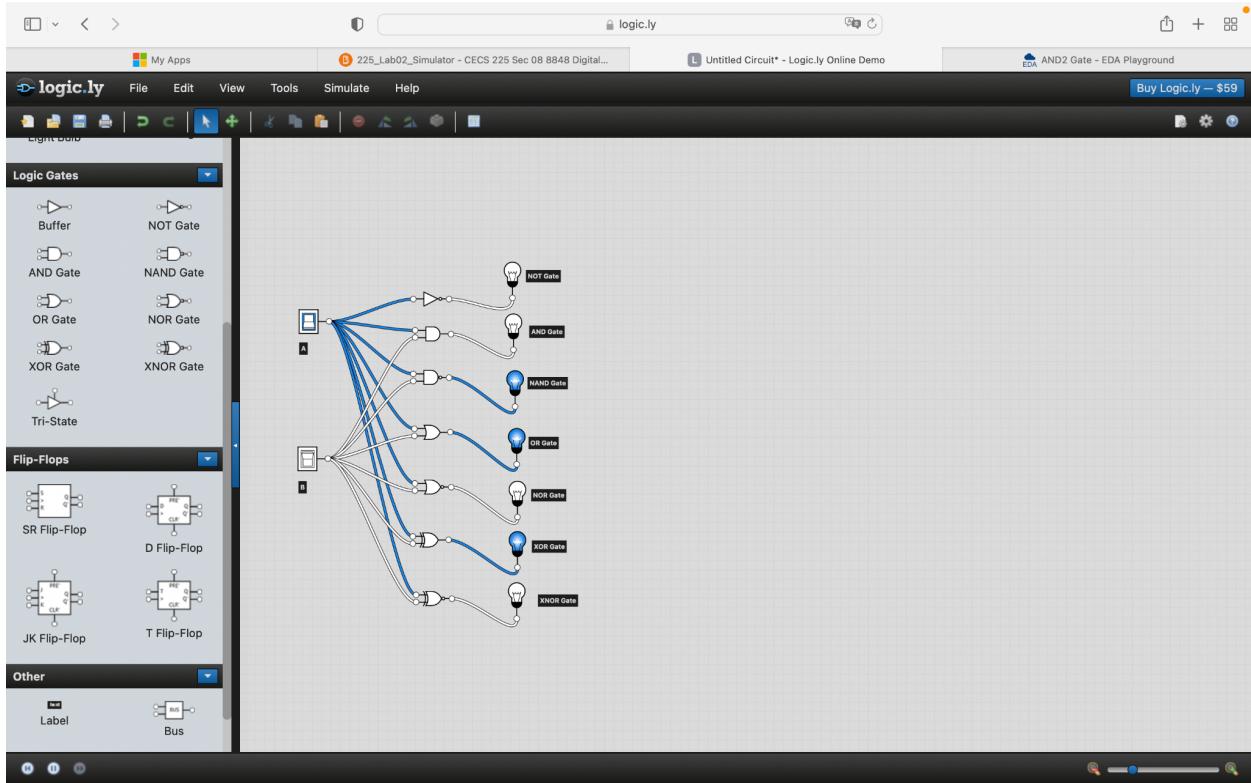
0 0 Representation



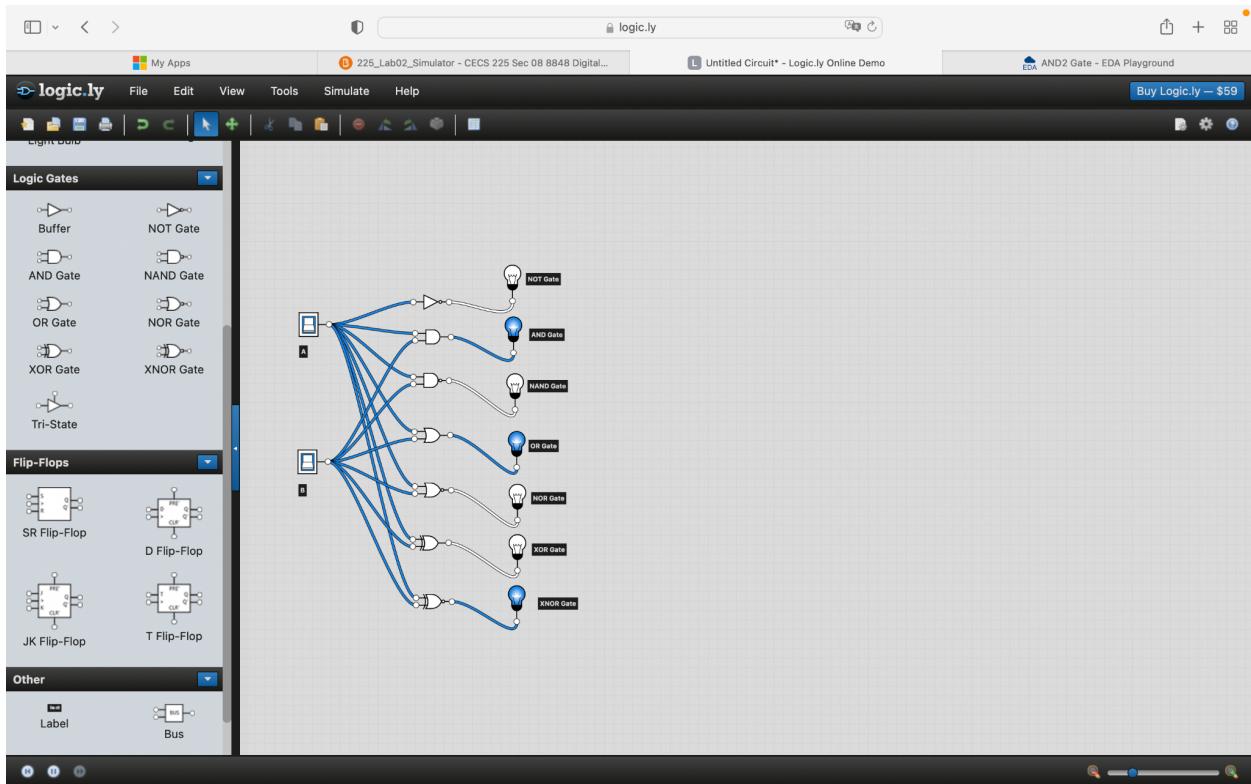
0 1 Representation:



1 0 Representation:



1 1 Representation:



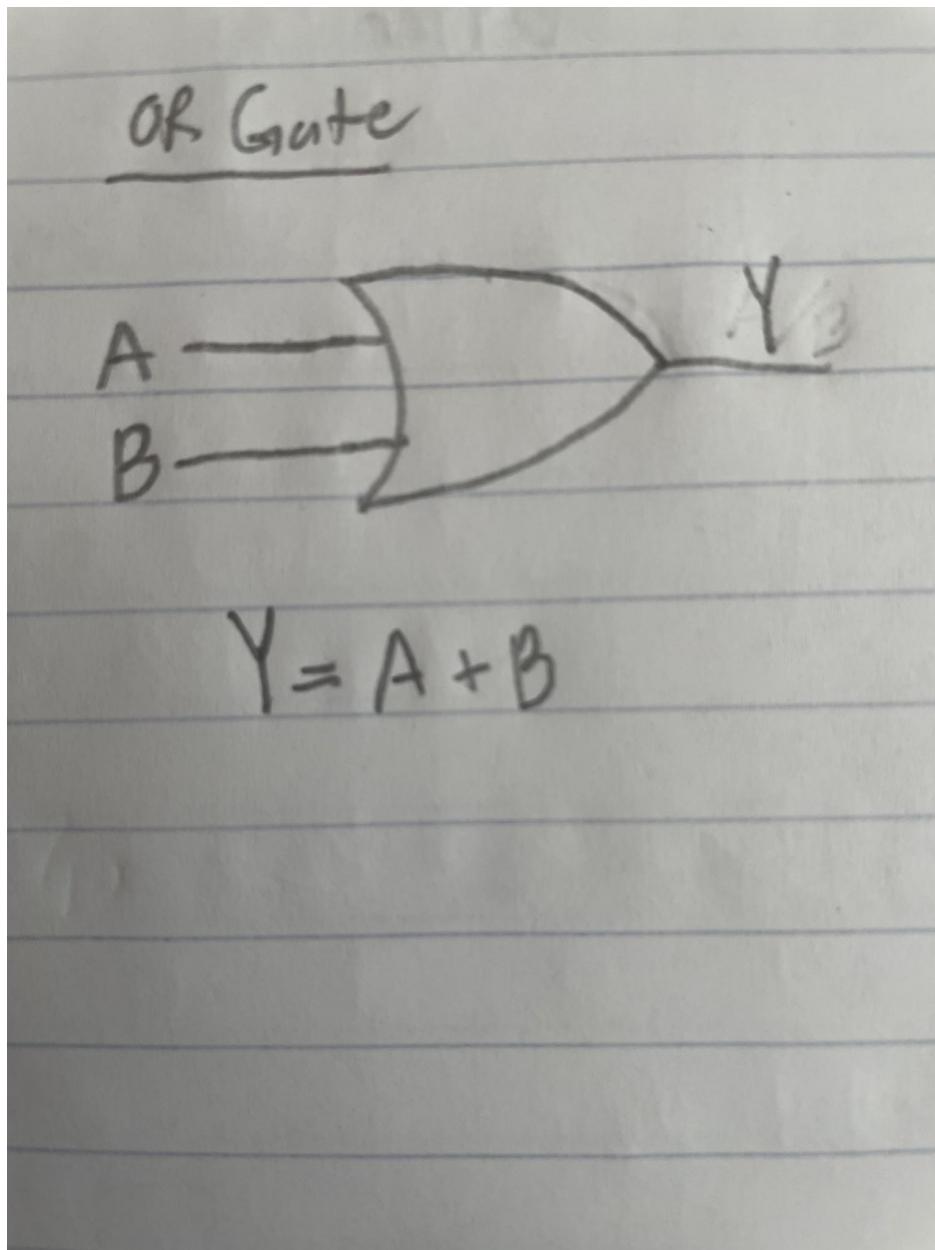
OR2 Gate

Description: The output will be 0 if none of the inputs are 1. If at least one of the inputs is 1 then the output will be 1.

Truth Table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Logical Symbol of OR Gate:



Verilog Code (OR Gate)

The screenshot shows the edaplayground.com interface. On the left, the sidebar includes sections for Languages & Libraries (Testbench + Design, UVM / OVM, Other Libraries), Tools & Simulators (Icarus Verilog 0.9.7, Compile Options, Run Options), Examples, Community (Collaborate, Forum), and social media links. The main area displays a Verilog module named `orGate`:// Code your design here
module orGate (a,b,y);
input a,b;
output y;
assign y = a|b;
endmoduleOn the right, there's a note about EPWave and a banner for a webinar.

This screenshot shows a testbench for the `orGate`. The sidebar is identical to the first screenshot. The main area displays a testbench script named `testbench.sv`:SV/Verilog Testbench

4 module testbench();
5 reg a,b;
6 wire y;
7 orgate or1(a,b,y);
8
9 initial begin
10 //Dump Waves
11 \$dumpfile("dump1.vcd");
12 \$dumpvars(1, testbench);
13
14 \$display("Test Case 0");
15 //Test Case 0
16 a = 1'b0;
17 \$display("a = %b", a);
18 b = 1'b0;
19 \$display("b = %b", b);
20 #5
21 \$display("y = %b", y);
22
23 \$display("Test Case 1");
24 //Test Case 1
25 a = 1'b0;
26 \$display("a = %b", a);
27 b = 1'b1;
28 \$display("b = %b", b);
29 #5
30 \$display("y = %b", y);
31
32 \$display("Test Case 2");
33 //Test Case 2
34 a = 1'b1;
35 \$display("a = %b", a);
36 b = 1'b0;
37 \$display("b = %b", b);
38 #5
39 \$display("y = %b", y);
40
41 \$display("Test Case 3");
42 //Test Case 3
43 a = 1'b1;
44 \$display("a = %b", a);
45 b = 1'b1;
46 \$display("b = %b", b);
47 #5
48 \$display("y = %b", y);
49
50 \$display("Test Case 4");
51 //Test Case 4
52 a = 1'b1;
53 \$display("a = %b", a);
54 b = 1'b1;
55 \$display("b = %b", b);
56 #5
57 \$display("y = %b", y);
58
59 end
60
61 endmoduleOn the right, there's a note about EPWave and a banner for a webinar.

edaplayground.com

Sample Report_Lab 01 - CECS... Correa_Lab2_Using Simulator ... OR2 Gate - EDA Playground OR Gate boolean - Google Search... Inbox (2,229) - correajoshua2...

EDA playground

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design.sv

e Log Share

```
[2022-02-02 17:58:14 EST]iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3:           : confusing timing results. Affected modules are:
testbench.sv:3:           : -- module orGate declared here: design.sv:2
VCD info: dumpfile dump1.vcd opened for output.
Test Case 0
a = 0
b = 0
y = 0
Test Case 1
a = 0
b = 1
y = 1
Test Case 2
a = 1
b = 0
y = 1
Test Case 3
a = 1
b = 1
y = 1
Finding VCD file...
./dump1.vcd
[2022-02-02 17:58:15 EST] Opening EPWave...
Done
```

EPWave

