

Lab 06: K-Map Simplification

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For Assignment Question 1(a):

Algebraic and K-Map Simplification for 1(a)

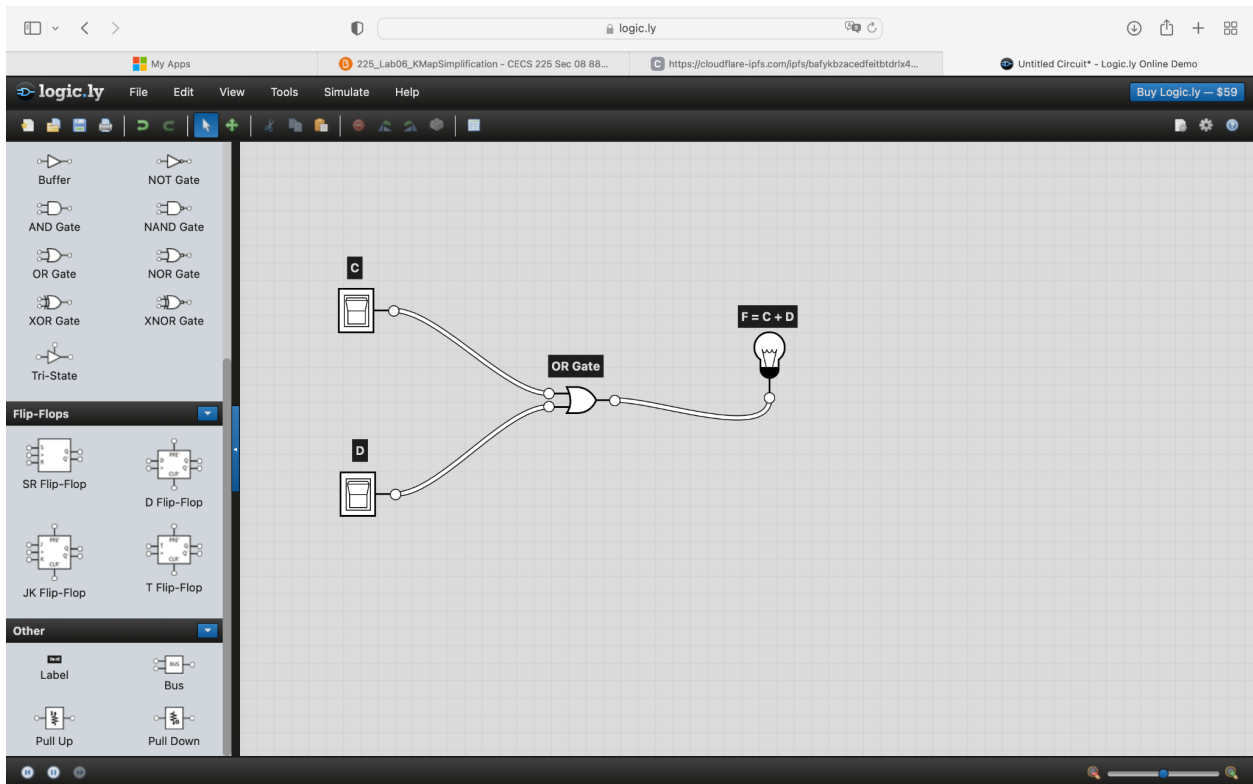
a) $f = CD + C\bar{D} + \bar{C}D$

F	C	D	F
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

$F = CD + C\bar{D} + \bar{C}D$
 $F = C(D + \bar{D}) + \bar{C}D$
 $F = C + \bar{C}D$
 $F = D + C$

$F = C + D$

Schematic for 1(a)



For Assignment Question 1(b):**K-Map Simplification for 1(b)**

	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	X
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	X
7	0	1	1	1	1
8	1	0	0	0	X
9	1	0	0	1	X
10	1	0	1	0	X
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1

CD \ AB	00	01	11	10
00	1	0	0	X
01	1	0	1	X
11	0	1	1	0
10	X	X	0	X

$$F = \bar{B}\bar{C} + ABD + BCD$$

Verilog Code for Question 1(b)

The screenshot shows the EDA Playground web interface. The left sidebar contains navigation links for Languages & Libraries, Tools & Simulators, and Community. The main editor area displays the Verilog code for 'design.av'.

```

1 module logicFunction(a, b, c, d, y);
2
3   input a, b, c, d;
4   output y;
5
6   assign y = ~b & ~c | a & b & d | b & c & d;
7
8 endmodule
  
```

The code implements a logic function with inputs a, b, c, d and output y. The logic is defined by the assignment statement on line 6.

The screenshot shows the EDA Playground web interface with the testbench file 'testbench.av' loaded. The left sidebar is the same as the previous screenshot. The main editor area displays the Verilog testbench code.

```

1 `timescale 1ns/1ps
2
3 module testbench();
4
5   reg a, b, c, d;
6   wire y;
7   logicFunction fn1(a, b, c, d, y);
8
9   initial begin
10    //Dump Waves
11    $dumpfile("dump1.vcd");
12    $dumpvars(1, testbench);
13
14    $display("After Simplification");
15    //After Simplification
16    a = 1'b1;
17    $display("a = %b", a);
18    b = 1'b0;
19    $display("b = %b", b);
20    c = 1'b1;
21    $display("c = %b", c);
22    d = 1'b1;
23    $display("d = %b", d);
24    #5
25    $display("y = %b", y);
26
27  end
28
29 endmodule
  
```

The testbench code sets up a simulation environment with a 1ns/1ps timescale. It instantiates the 'logicFunction' module as 'fn1'. The initial values for inputs a, b, c, and d are set to 1'b1, 1'b0, 1'b1, and 1'b1 respectively. The output y is displayed after a 5ns delay.

The screenshot displays the EDA Playground web interface. The browser's address bar shows the URL `edaplayground.com`. The interface includes a top navigation bar with buttons for Run, Save, and Copy, along with a warning: "If this page reloads when you click 'Run' please read this." Below this, the left sidebar contains sections for "Languages & Libraries" (with options for Testbench + Design, UVM / OVM, and Other Libraries), "Tools & Simulators" (set to Icarus Verilog 0.9.7), "Compile Options" (set to -Wall), "Run Options" (with "Open EPWave after run" checked), "Examples", and "Community" (with links to Collaborate, Forum, and Follow @edaplayground).

The main workspace shows a Verilog testbench file named `testbench.sv`. The simulation log displays the following output:

```
[2022-03-08 17:41:37 EST] iverilog '-Wall' design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:1: warning: Some modules have no timescale. This may cause
testbench.sv:1:      : confusing timing results. Affected modules are:
testbench.sv:1:      : -- module logicFunction declared here: design.sv:1
VCD info: dumpfile dump1.vcd opened for output.
After Simplification
a = 1
b = 0
c = 1
d = 1
y = 0
Finding VCD file...
./dump1.vcd
[2022-03-08 17:41:38 EST] Opening EPWave...
Done
```

A small thumbnail image of the EPWave waveform viewer is visible in the bottom right corner of the workspace.