

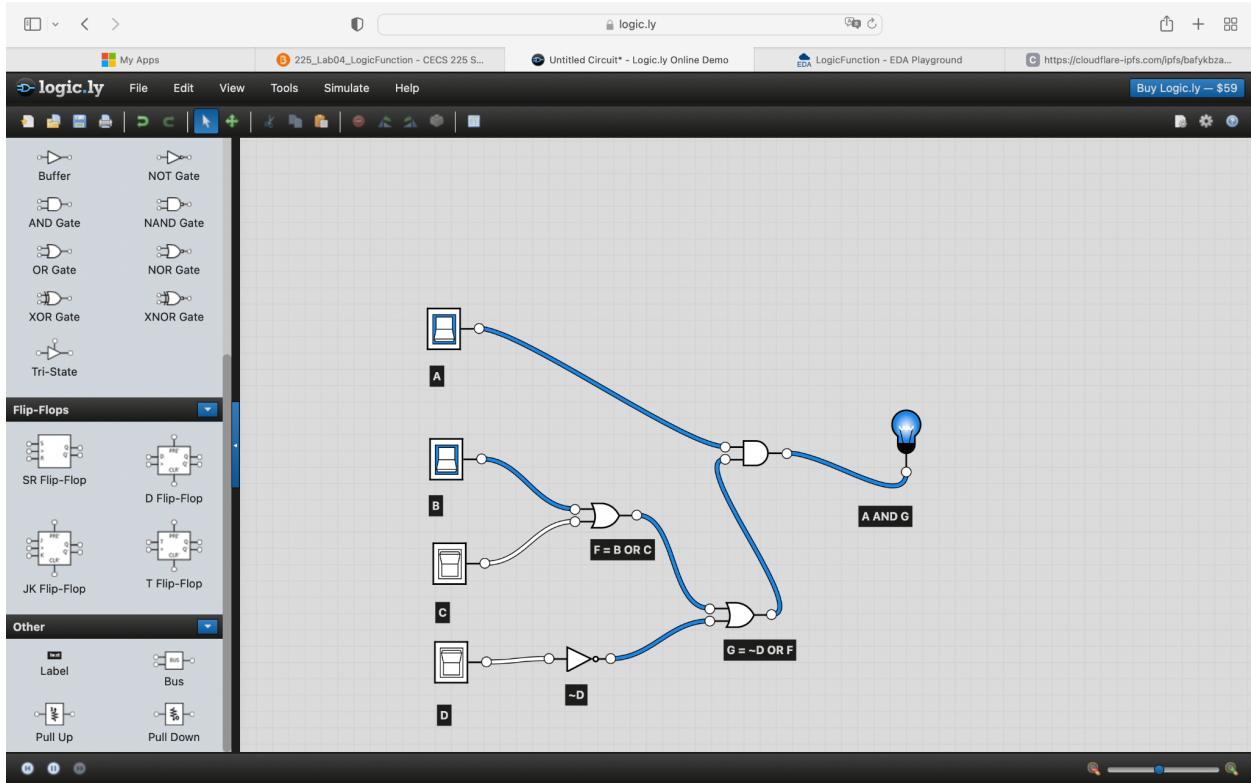
Lab 04: Logic Function

Lab 04: Logic Function  
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## TRUTH TABLE:

A	B	C	D	$\sim D$	$F = B \text{ OR } C$	$G = F \text{ OR } \sim D$	$A \text{ AND } G$
0	0	0	0	1	0	1	0
0	0	0	1	0	0	0	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	0
0	1	0	1	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
1	0	0	0	1	0	1	1
1	0	0	1	0	0	0	0
1	0	1	0	1	1	1	1
1	0	1	1	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	1	1	1
1	1	1	0	1	1	1	1
1	1	1	1	0	1	1	1

## SCHEMATIC:



## VERILOG CODE:

The image shows two screenshots of the edaplayground.com website, both displaying Verilog code in a text editor interface.

**Screenshot 1 (Top): Logic Function**

- Left Sidebar:** Shows 'Languages & Libraries' set to SystemVerilog/Verilog, 'Testbench + Design' set to Icarus Verilog 0.9.7, and 'Run Options' with 'Open EPWave after run' checked.
- Code Editor (design.sv):**

```

1 // Code your design here
2 module logicFunction(a,b,c,d,y);
3   input a,b,c,d;
4   output y;
5   assign y = a & (b | c | (~d));
6 endmodule
    
```
- Right Sidebar:** Shows 'SV/Verilog Design' and a link to https://cloudflare-ipfs.com/pfs/bafykbzacecfelbtbdhx...

**Screenshot 2 (Bottom): Testbench**

- Left Sidebar:** Shows 'Languages & Libraries' set to SystemVerilog/Verilog, 'Testbench + Design' set to Icarus Verilog 0.9.7, and 'Run Options' with 'Open EPWave after run' checked.
- Code Editor (testbench.sv):**

```

1 // Code your testbench here
2 // or browse Examples
3 `timescale 1ns/1ps
4 module testbench();
5   reg a,b,c,d;
6   wire y;
7   logicFunction fn1(a,b,c,d,y);
8
9   initial begin
10   //Dump Waves
11   $dumpfile("dump1.vcd");
12   $dumpvars(1, testbench);
13
14   $display("Test Case 0");
15   //Test Case 0
16   a = 1'b0;
17   $display("a = %b", a);
18   b = 1'b0;
19   $display("b = %b", b);
20   c = 1'b0;
21   $display("c = %b", c);
22   d = 1'b0;
23   $display("d = %b", d);
24
25   #5
26   $display("y = %b", y);
27
28   $display("Test Case 1");
29   //Test Case 1
30   a = 1'b0;
31   $display("a = %b", a);
32   b = 1'b0;
33   $display("b = %b", b);
34   c = 1'b0;
35   $display("c = %b", c);
36   d = 1'b1;
37   $display("d = %b", d);
38
39   #5
40   $display("y = %b", y);
41
42   $display("Test Case 2");
43   //Test Case 2
44   a = 1'b0;
45   $display("a = %b", a);
46   b = 1'b0;
47   $display("b = %b", b);
48   c = 1'b1;
49   $display("c = %b", c);
50   d = 1'b0;
51   $display("d = %b", d);
52
53
    
```
- Right Sidebar:** Shows 'SV/Verilog Testbench' and a link to https://cloudflare-ipfs.com/pfs/bafykbzacecfelbtbdhx...

**EDA playground**

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**Languages & Libraries**

Testbench + Design  
SystemVerilog/Verilog

UVL / OVM  
None

Other Libraries  
None  
OVL 2.8.1  
SVUnit 2.11  
SVAUUnit 3.0

Enable TL-Verilog  
 Enable Easier UVM  
 Enable VUnit

**Tools & Simulators**  
Icarus Verilog 0.9.7

Compile Options  
-Wall

Run Options  
Run Options  
 Open EPWave after run  
 Download files after run

**Examples**

**Community**  
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Follow @edaplayground

**testbench.sv**

```

55 $display("Test Case 3");
56 //Test Case 3
57 a = 1'b0;
58 $display("a = %b", a);
59 b = 1'b0;
60 $display("b = %b", b);
61 c = 1'b1;
62 $display("c = %b", c);
63 d = 1'b1;
64 $display("d = %b", d);
65 #
66 $display("y = %b", y);

67 $display("Test Case 4");
68 //Test Case 4
69 a = 1'b0;
70 $display("a = %b", a);
71 b = 1'b1;
72 $display("b = %b", b);
73 c = 1'b0;
74 $display("c = %b", c);
75 d = 1'b0;
76 $display("d = %b", d);
77 #
78 $display("y = %b", y);

79 $display("Test Case 5");
80 //Test Case 5
81 a = 1'b0;
82 $display("a = %b", a);
83 b = 1'b1;
84 $display("b = %b", b);
85 c = 1'b0;
86 $display("c = %b", c);
87 d = 1'b1;
88 $display("d = %b", d);
89 #
90 $display("y = %b", y);

91 $display("Test Case 6");
92 //Test Case 6
93 a = 1'b0;
94 $display("a = %b", a);
95 b = 1'b0;
96 $display("b = %b", b);
97 c = 1'b0;
98 $display("c = %b", c);
99 d = 1'b1;
100 $display("d = %b", d);
101 #
102 $display("y = %b", y);

103 $display("Test Case 7");
104 //Test Case 7
105 a = 1'b0;
106 $display("a = %b", a);
107 b = 1'b1;
108 $display("b = %b", b);
109 c = 1'b1;
110 $display("c = %b", c);
111 d = 1'b1;
112 $display("d = %b", d);
113 #
114 $display("y = %b", y);

115 $display("Test Case 8");
116 //Test Case 8
117 a = 1'b1;
118 $display("a = %b", a);
119 b = 1'b0;
120 $display("b = %b", b);
121 c = 1'b0;
122 $display("c = %b", c);
123 d = 1'b0;
124 $display("d = %b", d);
125 #
126 $display("y = %b", y);

127 $display("Test Case 9");
128 //Test Case 9
129 a = 1'b1;
130 $display("a = %b", a);
131 b = 1'b0;
132 $display("b = %b", b);
133 c = 1'b0;
134 $display("c = %b", c);
135 d = 1'b1;
136 $display("d = %b", d);
137 #
138 $display("y = %b", y);

139 $display("Test Case 10");
140 //Test Case 10
141 a = 1'b1;
142 $display("a = %b", a);
143 b = 1'b0;
144 $display("b = %b", b);
145 c = 1'b1;
146 $display("c = %b", c);
147 d = 1'b0;
148 $display("d = %b", d);
149 #
150 $display("y = %b", y);

```

**EDA playground**

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**Languages & Libraries**

Testbench + Design  
SystemVerilog/Verilog

UVL / OVM  
None

Other Libraries  
None  
OVL 2.8.1  
SVUnit 2.11  
SVAUUnit 3.0

Enable TL-Verilog  
 Enable Easier UVM  
 Enable VUnit

**Tools & Simulators**  
Icarus Verilog 0.9.7

Compile Options  
-Wall

Run Options  
Run Options  
 Open EPWave after run  
 Download files after run

**Examples**

**Community**  
Collaborate  
Forum  
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**testbench.sv**

```

107 $display("Test Case 7");
108 //Test Case 7
109 a = 1'b0;
110 $display("a = %b", a);
111 b = 1'b1;
112 $display("b = %b", b);
113 c = 1'b1;
114 $display("c = %b", c);
115 d = 1'b1;
116 $display("d = %b", d);
117 #
118 $display("y = %b", y);

119 $display("Test Case 8");
120 //Test Case 8
121 a = 1'b1;
122 $display("a = %b", a);
123 b = 1'b0;
124 $display("b = %b", b);
125 c = 1'b0;
126 $display("c = %b", c);
127 d = 1'b0;
128 $display("d = %b", d);
129 #
130 $display("y = %b", y);

131 $display("Test Case 9");
132 //Test Case 9
133 a = 1'b1;
134 $display("a = %b", a);
135 b = 1'b0;
136 $display("b = %b", b);
137 c = 1'b0;
138 $display("c = %b", c);
139 d = 1'b1;
140 $display("d = %b", d);
141 #
142 $display("y = %b", y);

143 $display("Test Case 10");
144 //Test Case 10
145 a = 1'b1;
146 $display("a = %b", a);
147 b = 1'b1;
148 $display("b = %b", b);
149 c = 1'b0;
150 $display("c = %b", c);
151 d = 1'b0;
152 $display("d = %b", d);
153 #
154 $display("y = %b", y);

```

**EDA playground**

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**Languages & Libraries**

- Testbench + Design
  - SystemVerilog/Verilog
- UVM / OVM
  - None
- Other Libraries
  - None
  - OVL 2.8.1
  - SVUnit 2.11
  - SVAUUnit 3.0
- Enable TL-Verilog
- Enable Easier UVM
- Enable VUnit

**Tools & Simulators**

- Icarus Verilog 0.9.7
- Compile Options
  - Wall
- Run Options
  - Run Options
- Open EPWave after run
- Download files after run

**Examples**

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**testbench.sv**

```

159 $display("Test Case 11");
160 //Test Case 11
161 a = 1'b1;
162 $display(`"a = %b", a);
163 b = 1'b0;
164 $display(`"b = %b", b);
165 c = 1'b1;
166 $display(`"c = %b", c);
167 d = 1'b1;
168 $display(`"d = %b", d);
169 #5
170 $display(`"y = %b", y);
171
172 $display("Test Case 12");
173 //Test Case 12
174 a = 1'b1;
175 $display(`"a = %b", a);
176 b = 1'b1;
177 $display(`"b = %b", b);
178 c = 1'b0;
179 $display(`"c = %b", c);
180 d = 1'b0;
181 $display(`"d = %b", d);
182 #5
183 $display(`"y = %b", y);
184
185 $display("Test Case 13");
186 //Test Case 13
187 a = 1'b1;
188 $display(`"a = %b", a);
189 b = 1'b1;
190 $display(`"b = %b", b);
191 c = 1'b0;
192 $display(`"c = %b", c);
193 d = 1'b1;
194 $display(`"d = %b", d);
195 #5
196 $display(`"y = %b", y);
197
198 $display("Test Case 14");
199 //Test Case 14
200 a = 1'b1;
201 $display(`"a = %b", a);
202 b = 1'b1;
203 $display(`"b = %b", b);
204 c = 1'b1;
205 $display(`"c = %b", c);
206 d = 1'b0;
207 $display(`"d = %b", d);
208 #5
209 $display(`"y = %b", y);

```

**design.sv**

**eLog**

```

[2022-02-15 17:05:06 EST]iverilog -Wall design.sv testbench.sv && unbuffer vvp a.out
testbench.sv:3: warning: Some modules have no timescale. This may cause
testbench.sv:3:           : confusing timing results. Affected modules are:
testbench.sv:3:           : -- module logicfunction declared here: design.sv:2
VCD info: dumpfile dump1.vcd opened for output.
Test Case 0
a = 0
b = 0
c = 0
d = 0
y = 0
Test Case 1
a = 0
b = 0
c = 0
d = 1
y = 0
Test Case 2
a = 0
b = 0
c = 1
d = 0
y = 0
Test Case 3
a = 0
b = 0
c = 1
d = 1
y = 0
Test Case 4
a = 0
b = 1
c = 0
d = 0
y = 0
Test Case 5
a = 0
b = 1
c = 0

```

My Apps 225\_Lab04\_LogicFunction - CECS 225 Sec 08 8848 D... LogicFunction - EDA Playground https://cloudflare-ipfs.com/pfs/bafykbzacedfeitbtldr4...

**EDA playground**

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**Languages & Libraries**

Testbench + Design SystemVerilog/Verilog

UVM / OVM None

Other Libraries None  
OVL 2.8.1  
SVUnit 2.11  
SVAUnit 3.0  
 Enable TL-Verilog  
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Tools & Simulators Icarus Verilog 0.9.7

Compile Options -Wall

Run Options Run Options  
 Open EPWave after run  
 Download files after run

Examples

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eLog Share

```
design.sv
Test Case 5
a = 0
b = 1
c = 0
d = 1
y = 0
Test Case 6
a = 0
b = 1
c = 1
d = 0
y = 0
Test Case 7
a = 0
b = 1
c = 1
d = 1
y = 0
Test Case 8
a = 1
b = 0
c = 0
d = 0
y = 1
Test Case 9
a = 1
b = 0
c = 0
d = 1
y = 0
Test Case 10
a = 1
b = 0
c = 1
d = 0
y = 0
Test Case 11
a = 1
b = 0
c = 1
d = 1
y = 1
Test Case 12
a = 1
b = 1
c = 0
d = 0
y = 1
Test Case 13
a = 1
b = 1
c = 0
d = 1
y = 1
Test Case 14
a = 1
b = 1
c = 1
d = 0
y = 1
Test Case 15
a = 1
b = 1
c = 1
d = 1
y = 1
Finding VCD file...
./dump1.vcd
[2022-02-15 17:05:06 EST] Opening EPWave...
Done
```

My Apps 225\_Lab04\_LogicFunction - CECS 225 Sec 08 8848 D... LogicFunction - EDA Playground https://cloudflare-ipfs.com/pfs/bafykbzacedfeitbtldr4...

**EDA playground**

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**Languages & Libraries**

Testbench + Design SystemVerilog/Verilog

UVM / OVM None

Other Libraries None  
OVL 2.8.1  
SVUnit 2.11  
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Tools & Simulators Icarus Verilog 0.9.7

Compile Options -Wall

Run Options Run Options  
 Open EPWave after run  
 Download files after run

Examples

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eLog Share

```
design.sv
a = 1
b = 0
c = 1
d = 0
y = 1
Test Case 11
a = 1
b = 0
c = 1
d = 1
y = 1
Test Case 12
a = 1
b = 1
c = 0
d = 0
y = 1
Test Case 13
a = 1
b = 1
c = 0
d = 1
y = 1
Test Case 14
a = 1
b = 1
c = 1
d = 0
y = 1
Test Case 15
a = 1
b = 1
c = 1
d = 1
y = 1
Finding VCD file...
./dump1.vcd
[2022-02-15 17:05:06 EST] Opening EPWave...
Done
```

