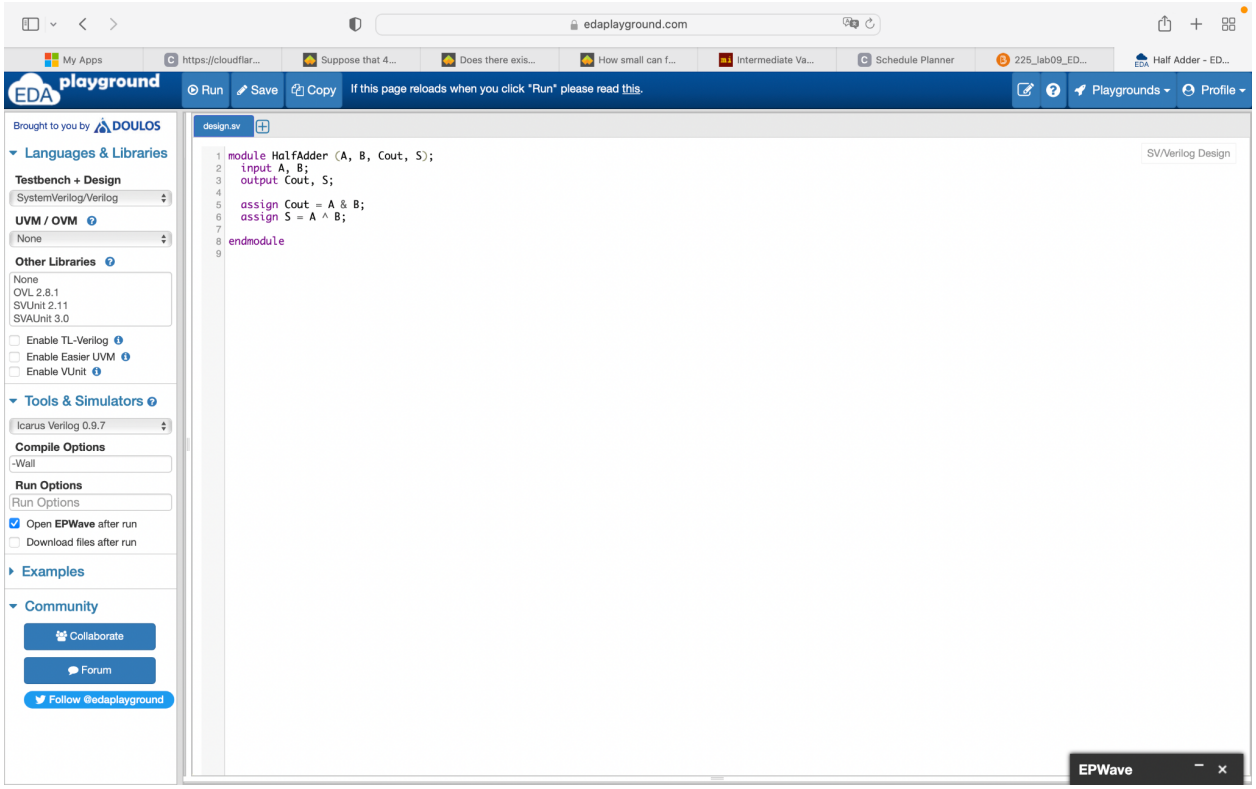
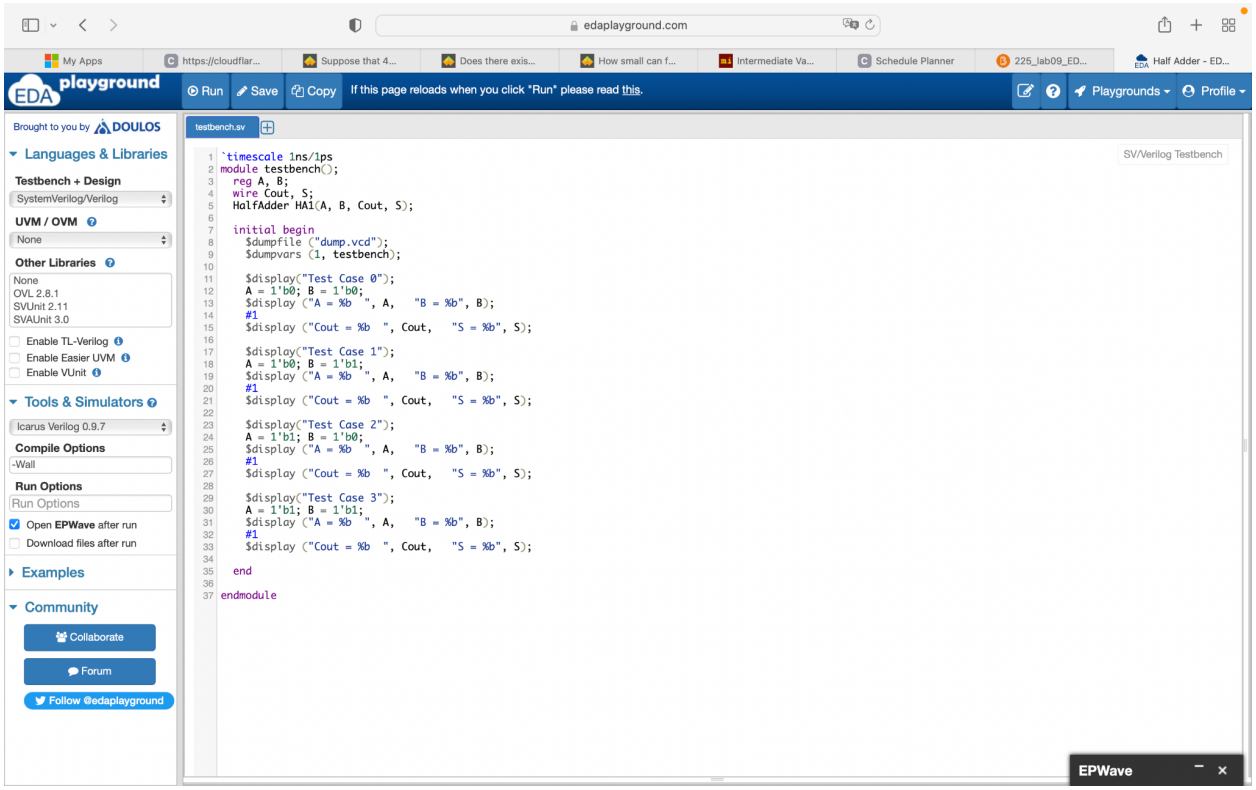
CECS 225
Lab 9: Half Adder
Joshua Correa ID: 029196984

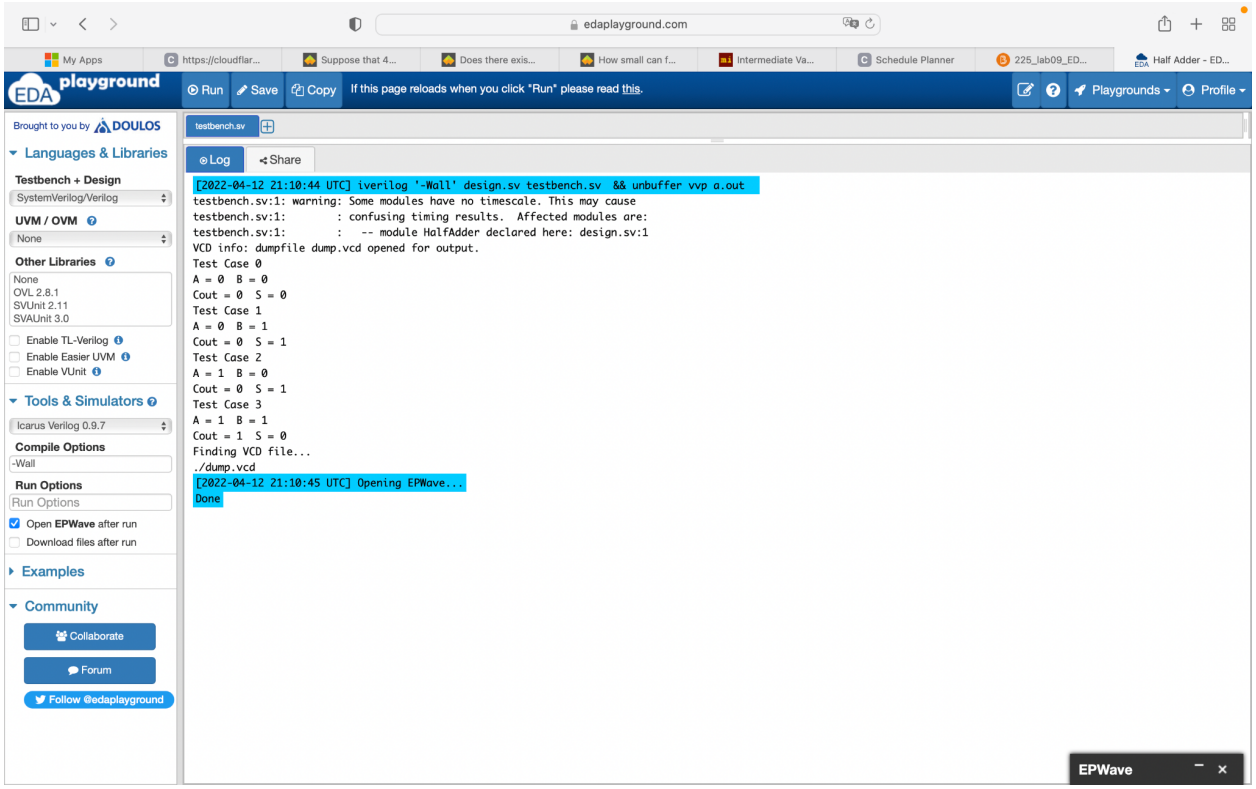
Section 1: Half Adder Verilog Module Source Code

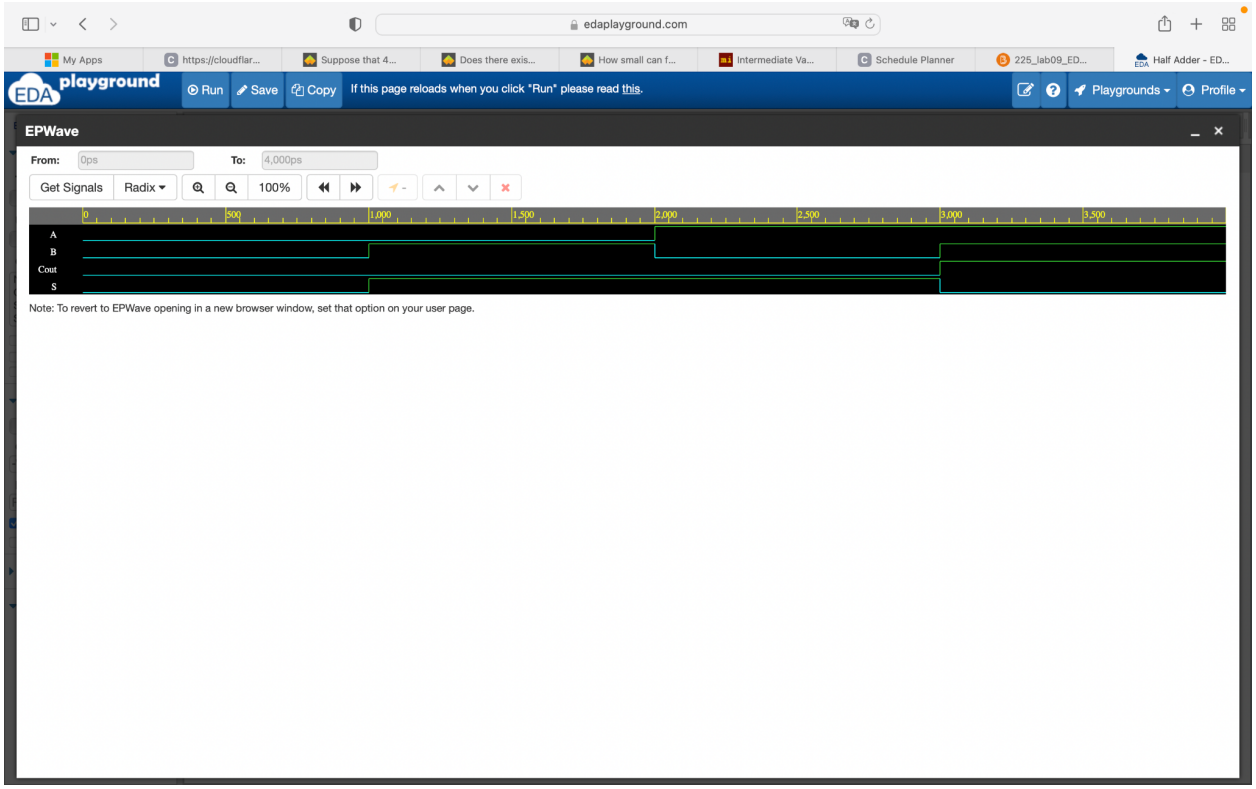


Section 2: Half Adder Verilog Test Code



Section 3: Half Adder Simulation Screenshot showing correct results





Section 4: Short Description Observation

From what I can see we are adding two binary digits using logic gates. When the number of 1 inputs is odd the S goes to 1, and when all the inputs are 1 the Cout goes to 1. This logic helps replicate the adding of binary digits we learned in Chapter 1.