

Lab 3: Simple Logic Function

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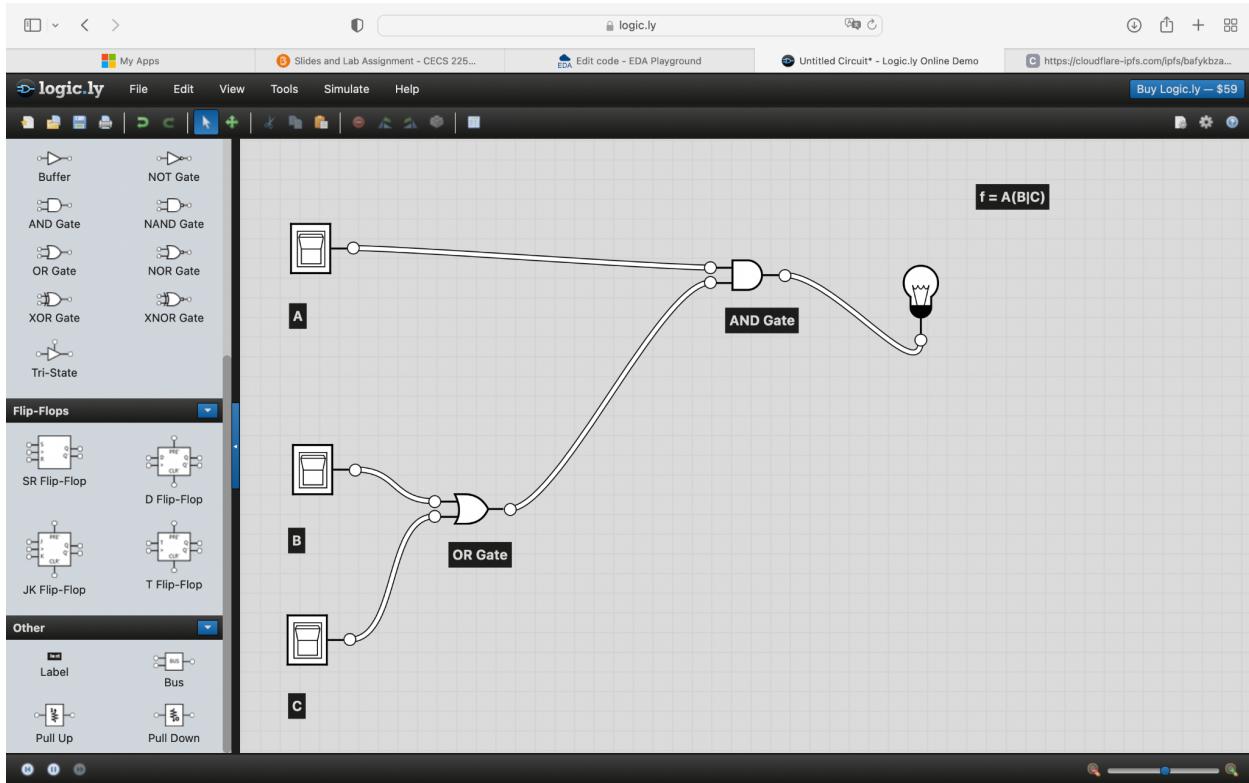
Lab 2: Simple Logic Function

Truth Table for Simple Logic Function:

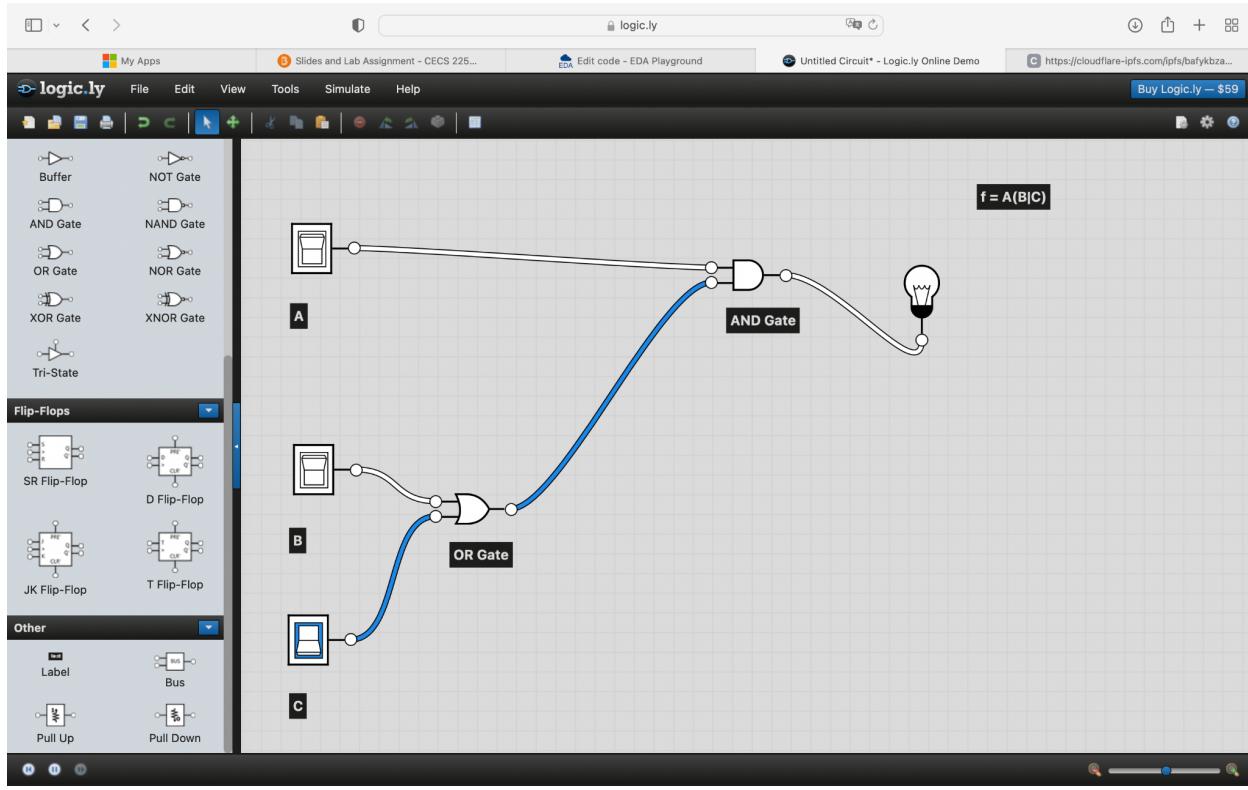
A	B	C	D = B OR C	F = A AND D
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Schematics Visualizing Simple Logic Function:

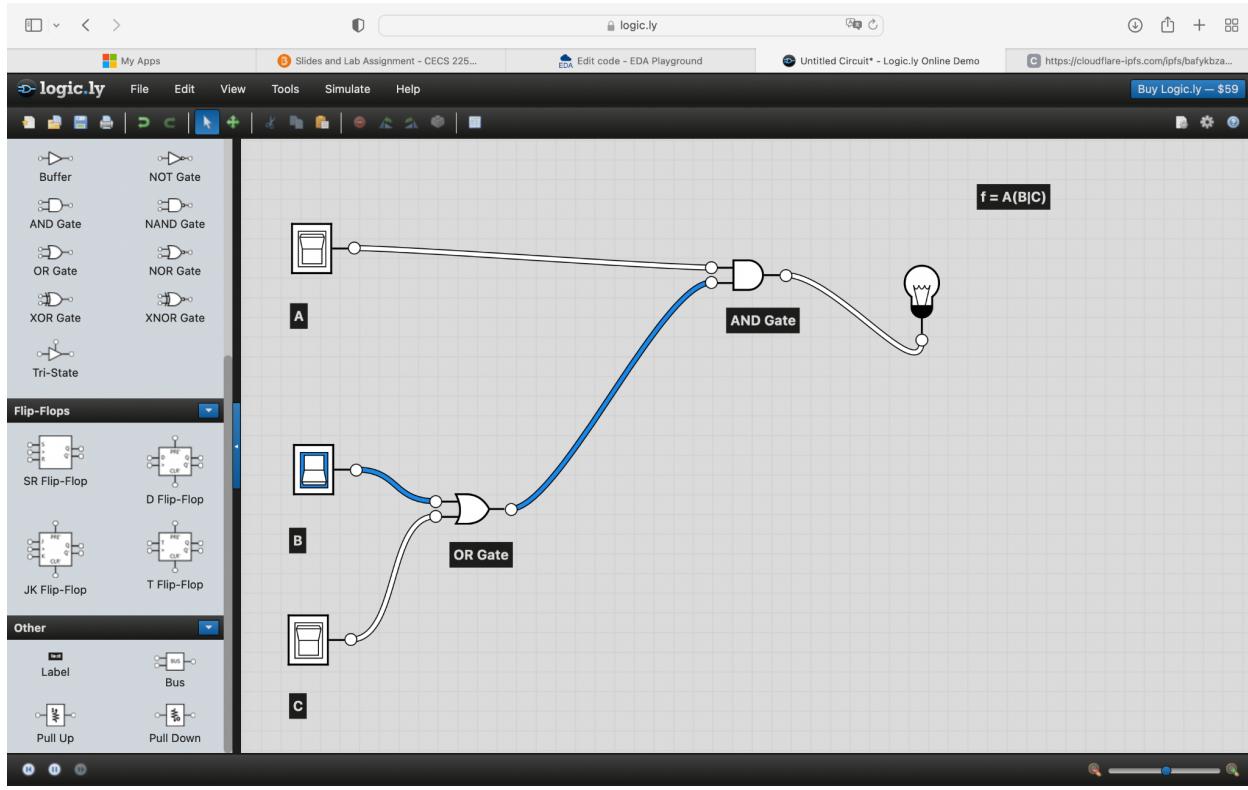
0 0 0 Representation



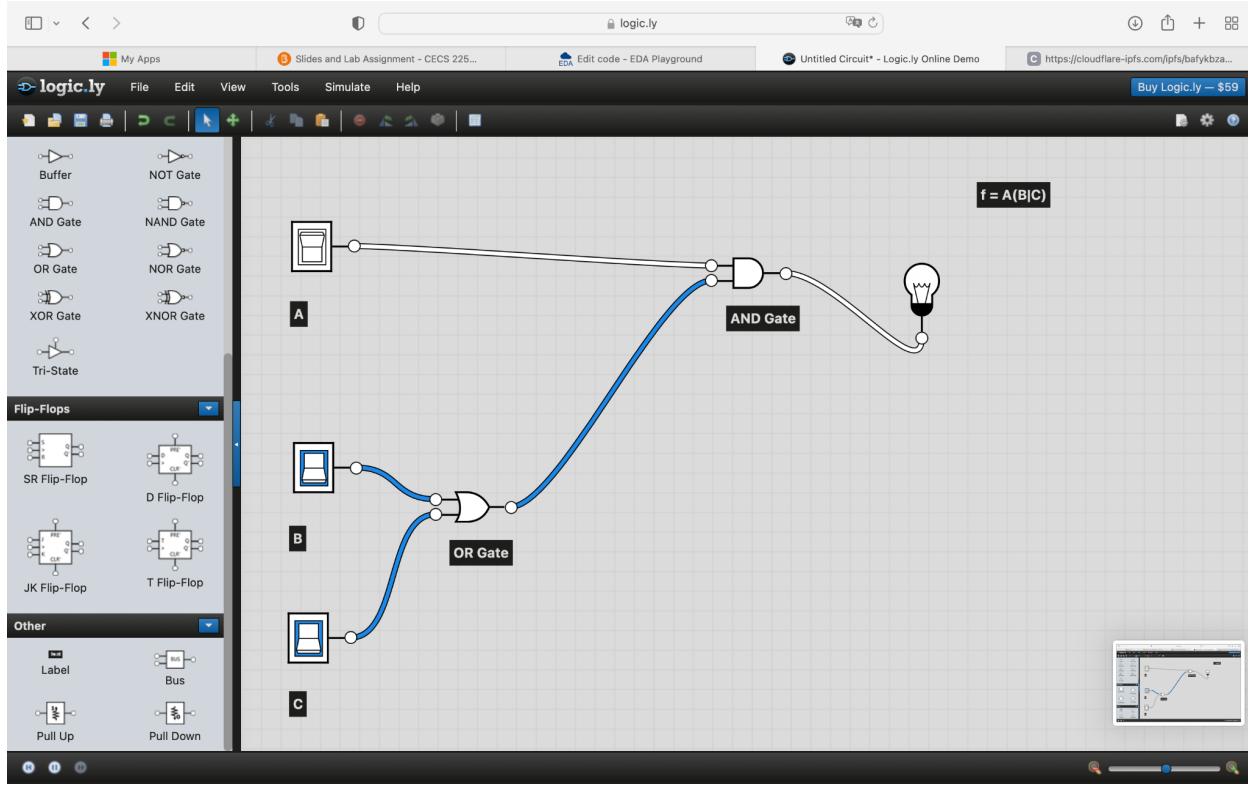
0 0 1 Representation



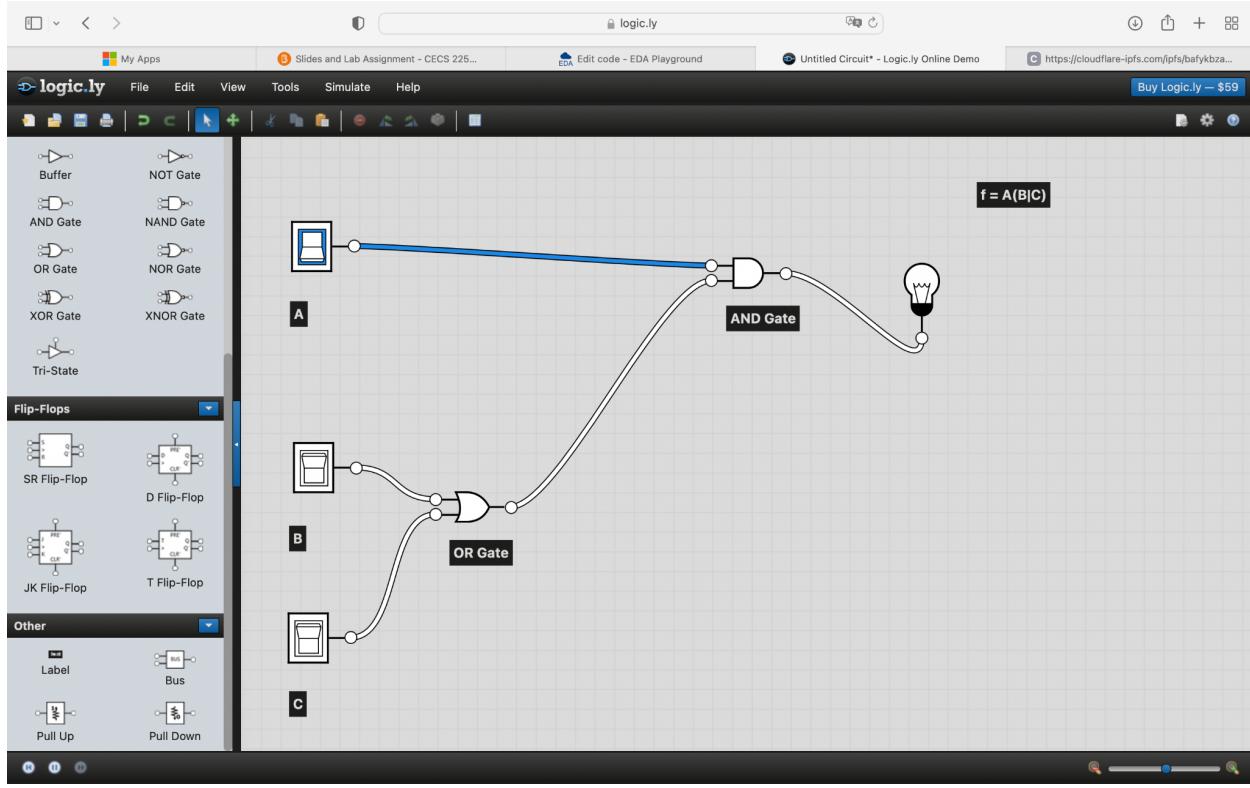
0 1 0 Representation



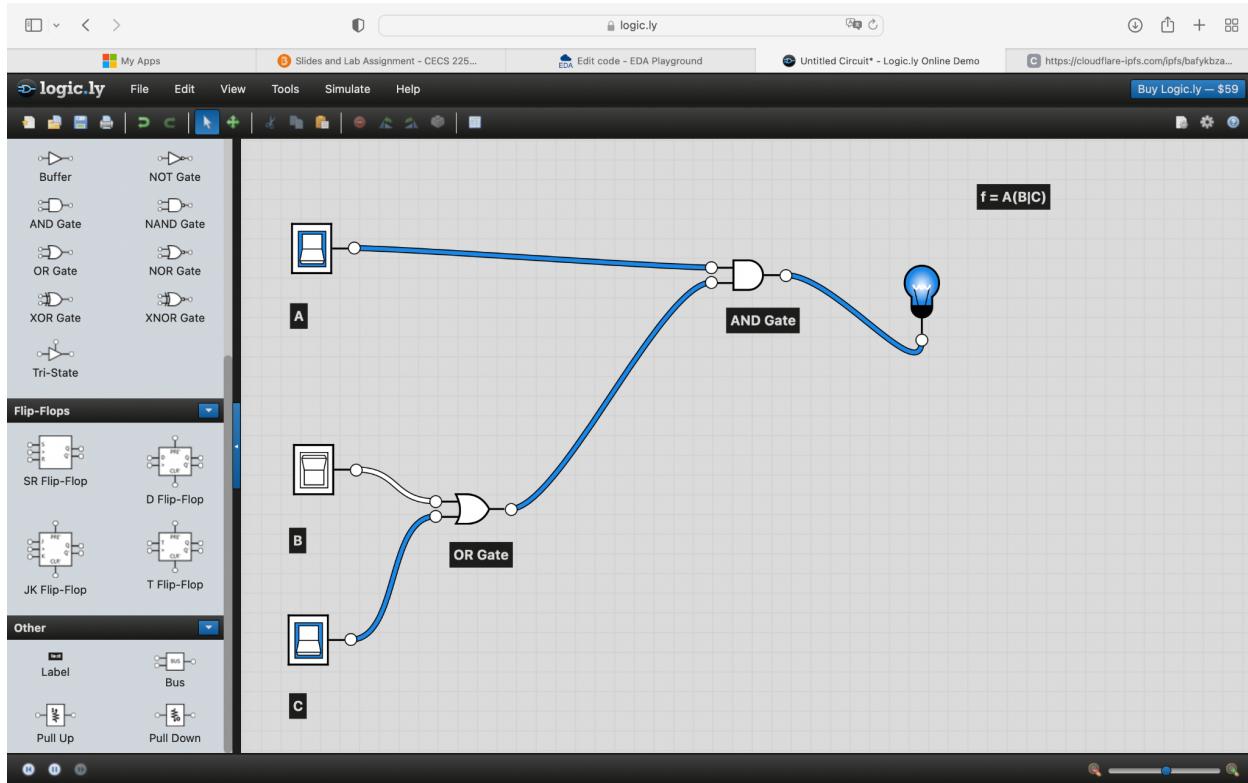
0 1 1 Representation



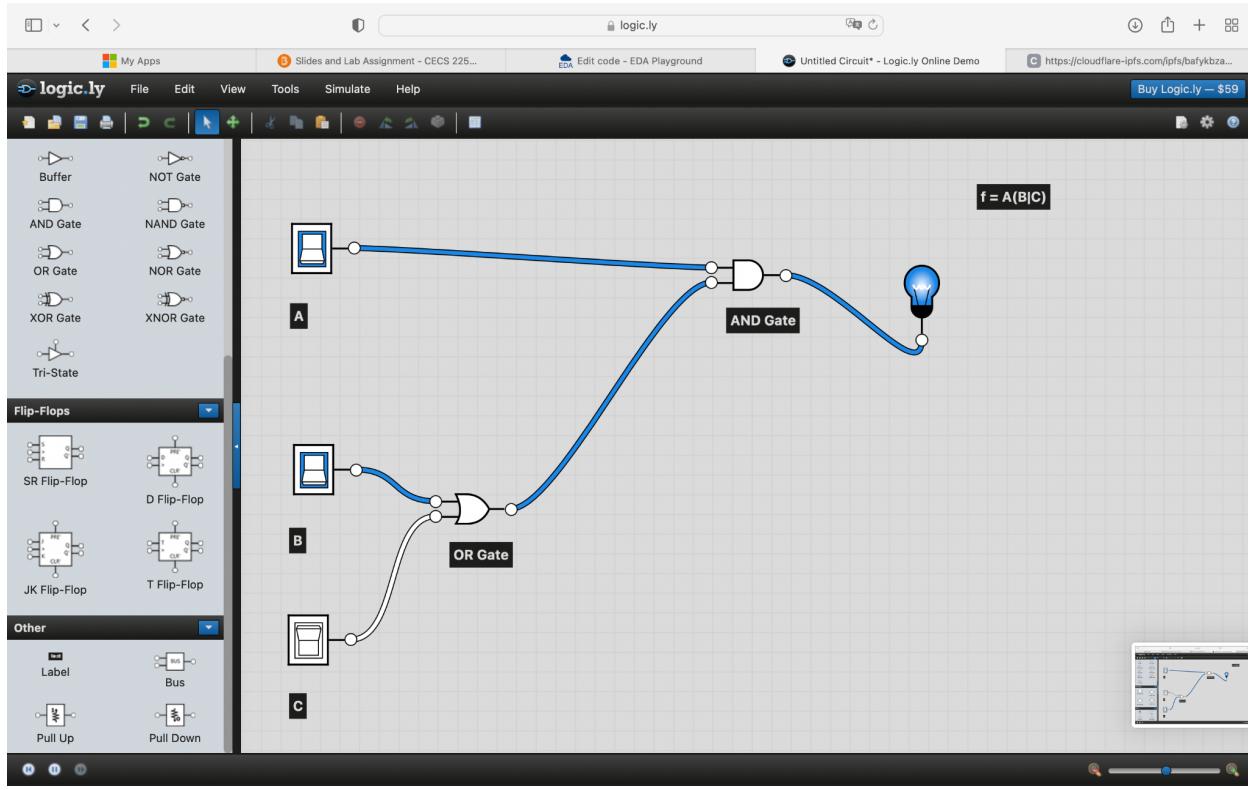
1 0 0 Representation



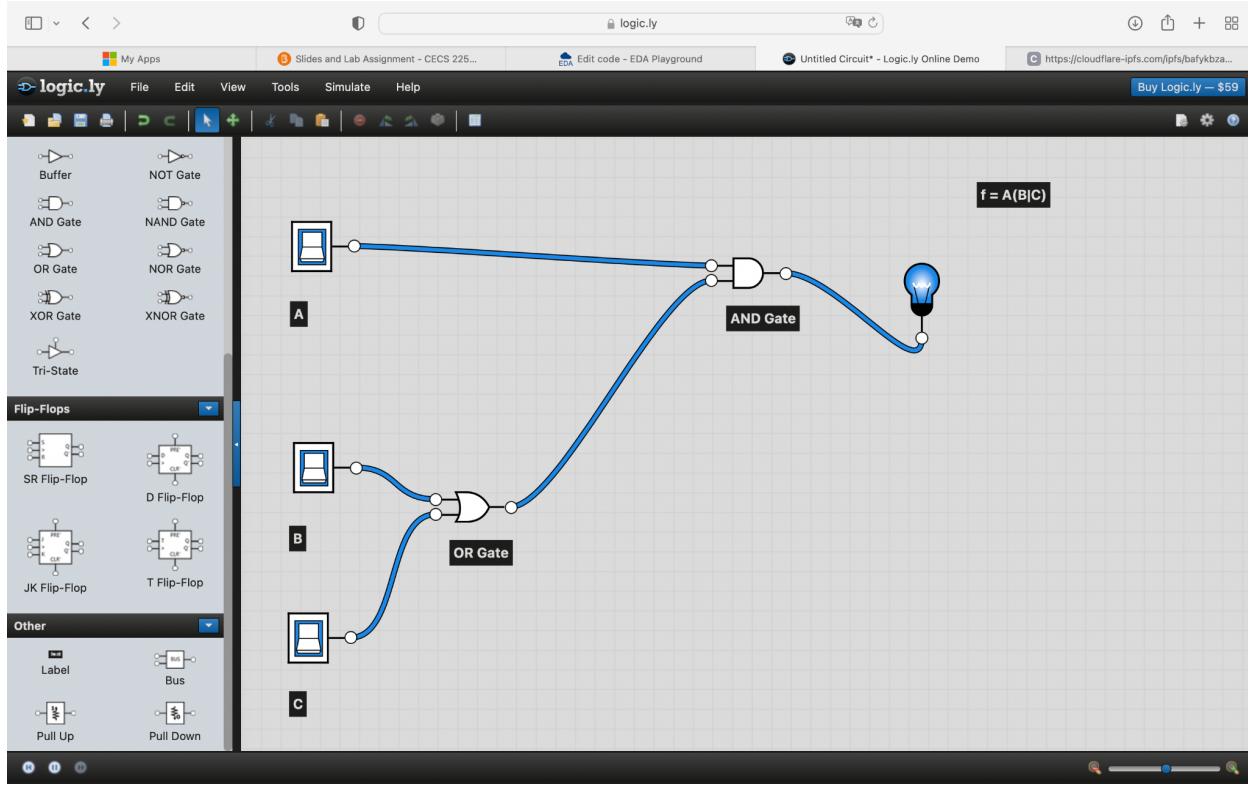
1 0 1 Representation



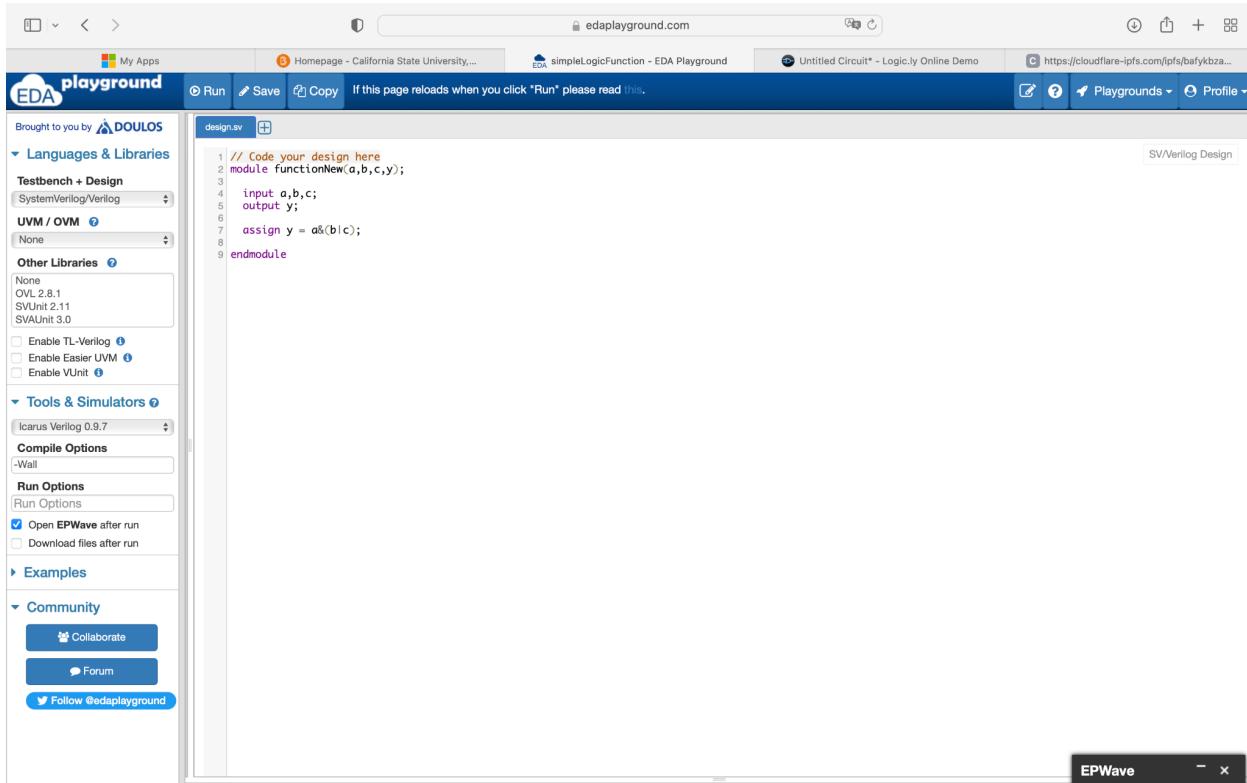
1 1 0 Representation



1.1.1 Representation



Verilog Code Simple Logic Function:



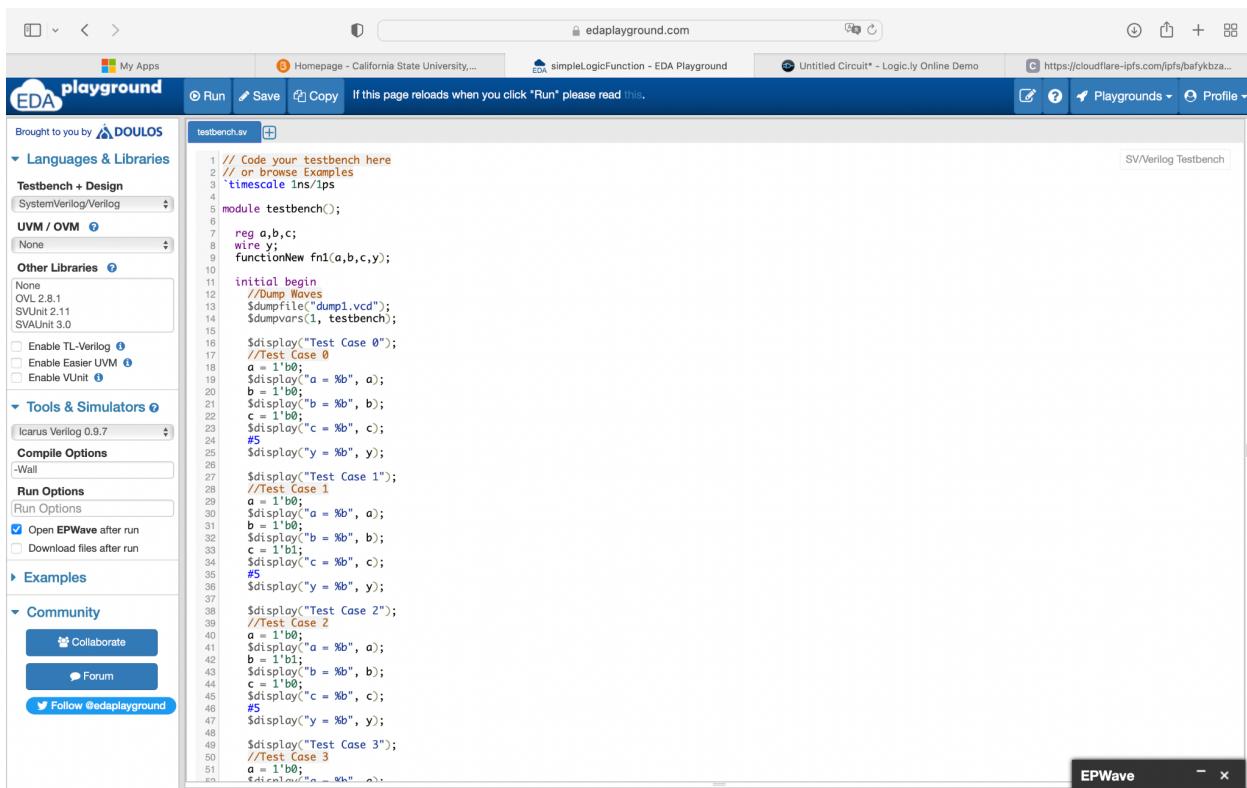
The screenshot shows the edaplayground.com interface. On the left, there's a sidebar with various configuration options like Languages & Libraries (SystemVerilog/Verilog selected), UVM / OVM (None), and Tools & Simulators (Icarus Verilog 0.9.7). The main area displays a Verilog module named 'functionNew'. The code is as follows:

```

1 // Code your design here
2 module functionNew(a,b,c,y);
3   input a,b,c;
4   output y;
5   assign y = a&(b|c);
6 endmodule

```

On the right, there's a status bar labeled 'SV/Verilog Design'.



The screenshot shows the edaplayground.com interface again. The sidebar remains the same. The main area now displays a Verilog testbench module named 'testbench'. The code is as follows:

```

1 // Code your testbench here
2 // or browse Examples
3 `timescale 1ns/1ps
4
5 module testbench();
6
7 reg a,b,c;
8 wire y;
9 functionNew fn1(a,b,c,y);
10
11 initial begin
12   //Dump Waves
13   $dumpfile("dump1.vcd");
14   $dumpvars(1, testbench);
15
16   $display("Test Case 0");
17   //Test Case 0
18   a = 1'b0;
19   $display("a = %b", a);
20   b = 1'b0;
21   $display("b = %b", b);
22   c = 1'b1;
23   $display("c = %b", c);
24   #
25   $display("y = %b", y);
26
27   $display("Test Case 1");
28   //Test Case 1
29   a = 1'b0;
30   $display("a = %b", a);
31   b = 1'b0;
32   $display("b = %b", b);
33   c = 1'b1;
34   $display("c = %b", c);
35   #
36   $display("y = %b", y);
37
38   $display("Test Case 2");
39   //Test Case 2
40   a = 1'b0;
41   $display("a = %b", a);
42   b = 1'b1;
43   $display("b = %b", b);
44   c = 1'b0;
45   $display("c = %b", c);
46   #
47   $display("y = %b", y);
48
49   $display("Test Case 3");
50   //Test Case 3
51   a = 1'b0;
52   $display("a = %b", a);

```

On the right, there's a status bar labeled 'SV/Verilog Testbench'.

The screenshot shows the EDA playground interface with a Verilog testbench script named 'testbench.sv'. The code contains multiple test cases (Test Case 1 through Test Case 7) using the \$display command to print variable values. The playground interface includes a sidebar with options for Languages & Libraries, Tools & Simulators (selected as Icarus Verilog 0.9.7), and Community features like Collaborate, Forum, and Follow @edaplayground.

```

testbench.sv [+] 
49 $display("Test Case 1");
50 //Test Case 1
51 a = 1'b0;
52 $display("a = %b", a);
53 b = 1'b1;
54 $display("b = %b", b);
55 c = 1'b1;
56 $display("c = %b", c);
57 #5
58 $display("y = %b", y);
59
60 $display("Test Case 2");
61 //Test Case 2
62 a = 1'b1;
63 $display("a = %b", a);
64 b = 1'b0;
65 $display("b = %b", b);
66 c = 1'b0;
67 $display("c = %b", c);
68 #5
69 $display("y = %b", y);
70
71 $display("Test Case 3");
72 //Test Case 3
73 a = 1'b1;
74 $display("a = %b", a);
75 b = 1'b0;
76 $display("b = %b", b);
77 c = 1'b1;
78 $display("c = %b", c);
79 #5
80 $display("y = %b", y);
81
82 $display("Test Case 4");
83 //Test Case 4
84 a = 1'b1;
85 $display("a = %b", a);
86 b = 1'b1;
87 $display("b = %b", b);
88 c = 1'b0;
89 $display("c = %b", c);
90 #5
91 $display("y = %b", y);
92
93 $display("Test Case 5");
94 //Test Case 5
95 a = 1'b1;
96 $display("a = %b", a);
97 b = 1'b1;
98 $display("b = %b", b);
99 c = 1'b1;
100 $display("c = %b", c);

```

The screenshot shows the EDA playground interface with a Verilog design script named 'design.sv'. The code defines variables a, b, c, and y with their initial values. It then lists seven test cases (Test Case 1 to Test Case 7) where each case changes one or more variables and prints them. Below the code, it says 'Finding VCD file...' followed by a command line prompt with the date and time. An EPWave window is visible at the bottom right, showing the output of the command. The playground interface includes a sidebar with options for Languages & Libraries, Tools & Simulators (selected as Icarus Verilog 0.9.7), and Community features like Collaborate, Forum, and Follow @edaplayground.

```

design.sv [+] 
e Log Share
Test Case 1
a = 0
b = 0
c = 1
y = 0
Test Case 2
a = 0
b = 1
c = 0
y = 0
Test Case 3
a = 0
b = 1
c = 1
y = 0
Test Case 4
a = 1
b = 0
c = 0
y = 0
Test Case 5
a = 1
b = 0
c = 1
y = 1
Test Case 6
a = 1
b = 1
c = 0
y = 1
Test Case 7
a = 1
b = 1
c = 1
y = 1
Finding VCD file...
./dump1.vcd
[2022-02-08 17:42:19 EST] Opening EPWave...
Done

```

