

ZEDEC POST-QUANTUM COMPUTING ARCHITECTURE

EMOTIONAL PROCESSING UNIT (EPU) SPECIFICATION

GlyphMap J.D.R. Computational Core

符号图谱 J.D.R. 计算核心

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1. ARCHITECTURAL PARADIGM

1.1 Design Philosophy: Negentropy

The ZEDEC architecture represents a radical departure from Von Neumann computing. Traditional systems generate heat and noise as waste products. The ZEDEC architecture **reverses disorder** through:

- Geometric topology** derived from Rodin Coil mechanics
- Vortex Mathematics** for energy containment
- Field resonance** instead of binary switching

TRADITIONAL COMPUTING	ZEDEC ARCHITECTURE
• Electron flow through gates	• Field interactions
• Binary switching (0/1)	• 5-phase resonance
• Heat as waste product	• Energy recycling
• Clock tree distribution	• Unified field reference
• EMI requires shielding	• Geometric cancellation
• Volatile state storage	• Strain-based memory
• Entropic (disorder increases)	• Negentropic (coherent)
Result: Calculates	Result: Resonates

1.2 Core Principles

| Principle | Implementation |

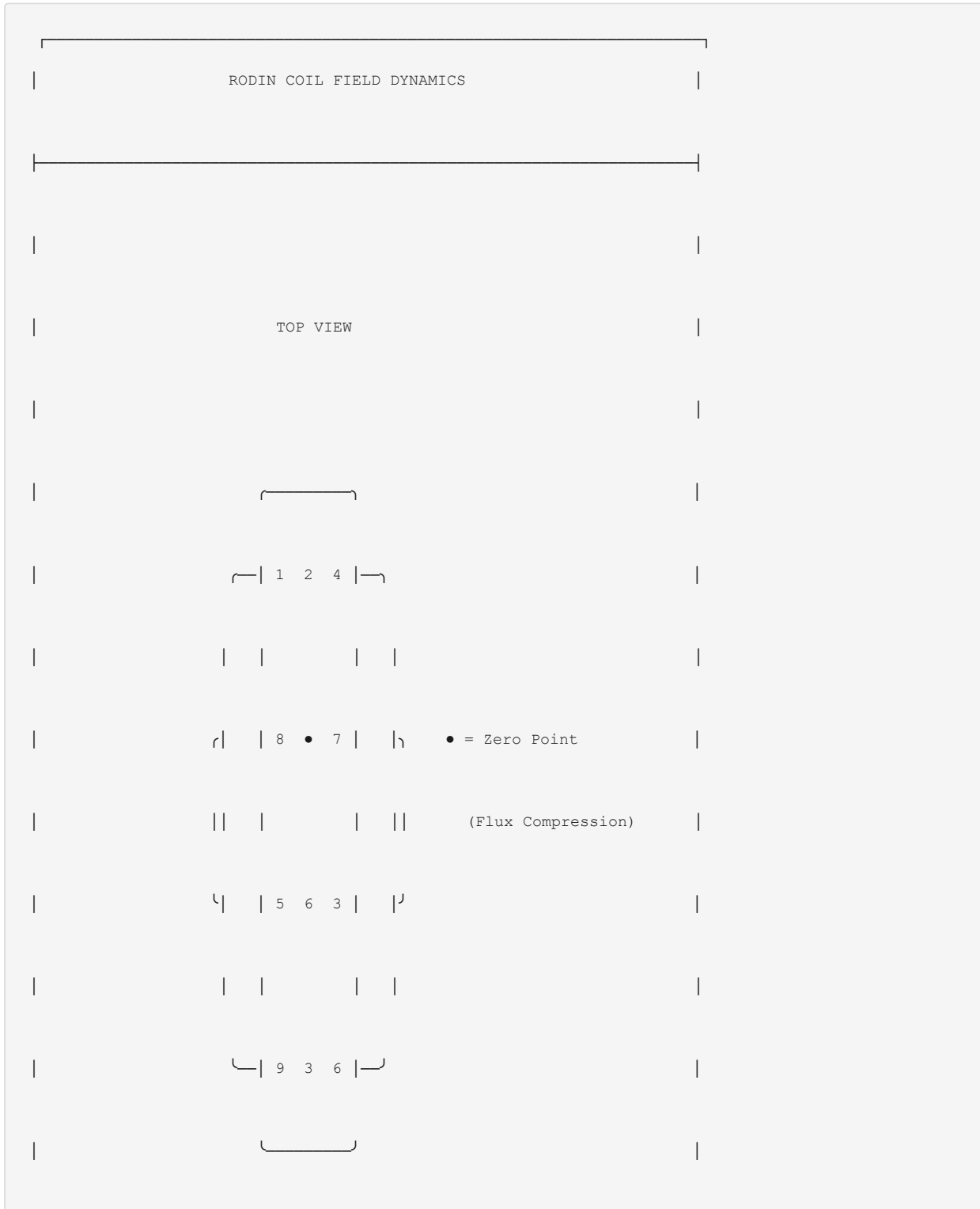
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| **Field Processing** | Information encoded in phase modulations || **Orthogonal Coupling** | 90° E/B field relationship ||
Harmonic Resonance | 7.8125 Hz base frequency system || **Fractal Scalability** | Flower of Life recursive geometry || **Non-Volatile State** | Strain-based storage (no refresh) |

2. TOROIDAL FIELD CONTAINMENT

2.1 Rodin Coil Geometry

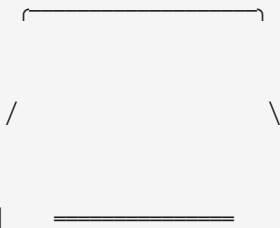
The physical chassis and circuit pathways follow the **Rodin Coil** winding pattern on a torus surface.



WINDING TRAJECTORY: 1→2→4→8→7→5→1 (Vortex Math doubling)

CONTROL AXIS: 3→6→9 (Power distribution)

SIDE VIEW (Cross-section)



FLUX LINES

↓↓↓

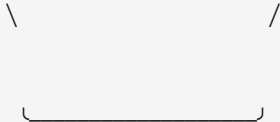
Magnetic flux folds

•

INWARD to center

↑↑↑

(No EMI radiation)



2.2 Field Shear and Compression

The specific winding trajectory creates **field shear and compression**:

| Effect | Mechanism | Benefit |

|-----|-----|-----|

| **Inward Folding** | Magnetic flux compresses to center | No ferromagnetic cores needed | | **Zero Point** | Intense structured flux at torus center | Unified reference frame | | **EMI Cancellation** | Geometric cancellation vs physical shielding | Clean noise floor | | **Synchronous Reference** | Toroidal field as clock distribution | No clock tree latency |

2.3 Vortex Mathematics Foundation

The 1-2-4-8-7-5 / 3-6-9 pattern provides:

DOUBLING CIRCUIT (Data Flow):

1 → 2 → 4 → 8 → 16(7) → 32(5) → 64(1) → ...

↓ ↓ ↓ ↓

2×1 2×2 2×4 2×8

All digits reduce to: 1, 2, 4, 8, 7, 5 (never 3, 6, or 9)

CONTROL AXIS (Power Distribution):

3 → 6 → 12(3) → 24(6) → 48(3) → 96(6) → ...

↓ ↓ ↓ ↓

2×3 2×6 2×12 2×24

Oscillates between 3, 6, 9 only

SIGNIFICANCE:

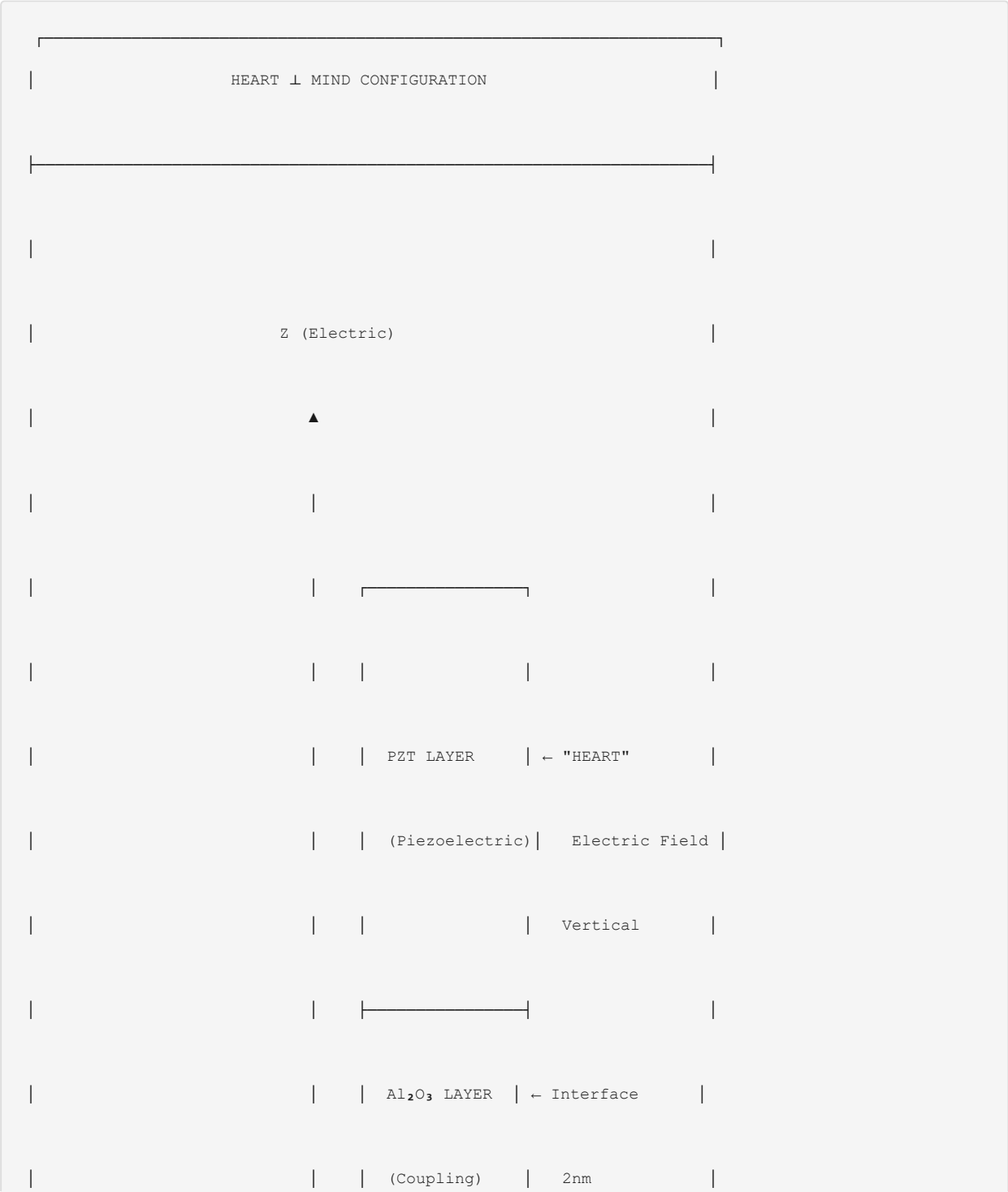
- Data and Power remain ORTHOGONAL
- Non-interfering signal paths

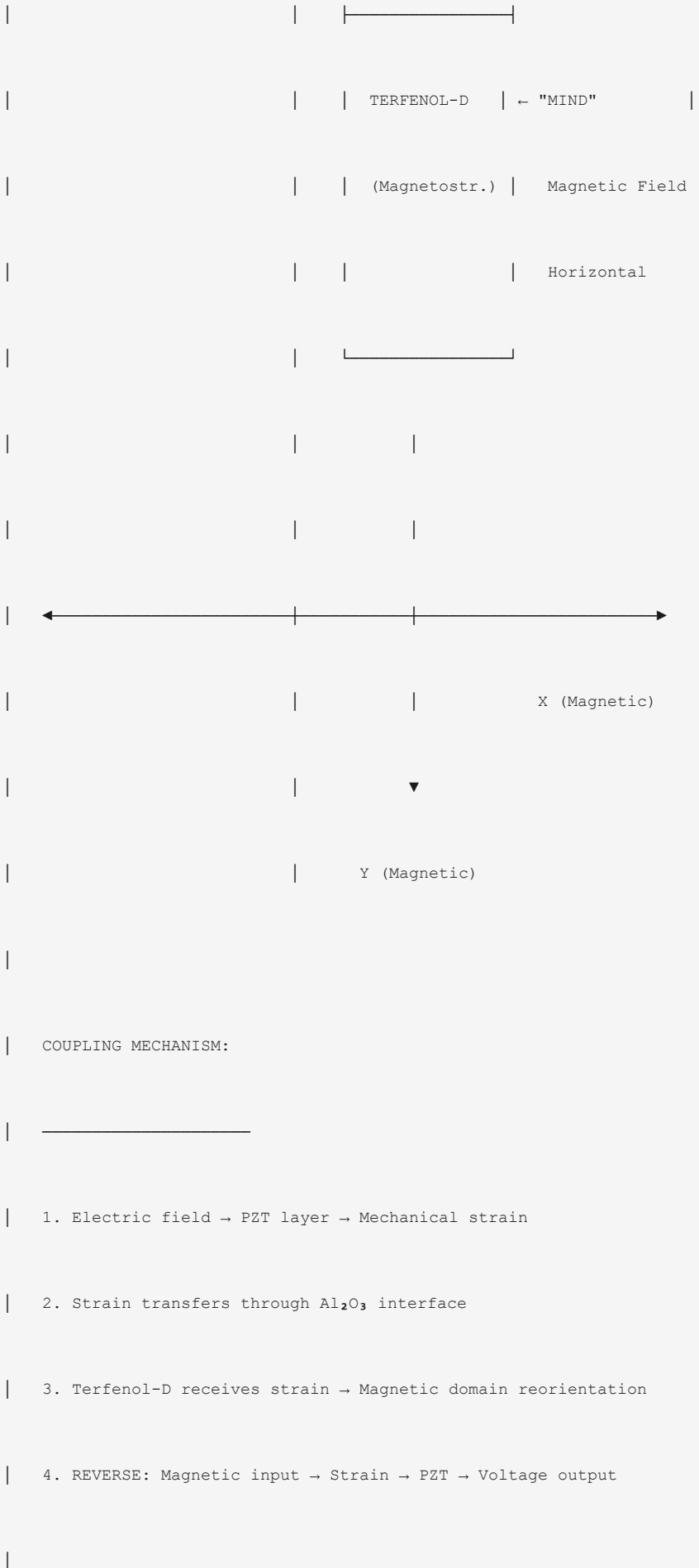
- 9 is the "axis" or "zero" reference

3. HEART ⊥ MIND ARCHITECTURE

3.1 Orthogonal Field Configuration

The core mechanism is the **90-degree relationship** between electric and magnetic vectors:





```
| RESULT: Non-destructive read/write via orthogonal coupling |
```

```
|
```

```
|
```

```
|_____|
```

| Operation | Mechanism |

| **WRITE** | Voltage \rightarrow PZT strain \rightarrow Terfenol-D domain flip || | **READ** | Magnetic input \rightarrow Terfenol-D strain \rightarrow PZT voltage || | **STORE** | Stable strain state in crystal lattice || | **PROCESS** | Phase modulation of E/B coupling coefficient | **Key Advantage:** Information stored as **physical strain**, not volatile charge. No refresh required.

...

The fundamental logic unit of the EPU:

The diagram illustrates the cross-section of a magnetoelectric core cell. It consists of several layers: a top electrode (Au), a layer stack, and a magnetoelectric core cell. The layers are separated by horizontal lines, and the entire structure is enclosed in a rectangular frame. The text 'MAGNETOELECTRIC CORE CELL' is centered in the upper portion, and 'LAYER STACK (Cross-section):' is centered in the lower portion. The top electrode is labeled 'TOP ELECTRODE (Au)'.

MAGNETOELECTRIC CORE CELL

LAYER STACK (Cross-section):

TOP ELECTRODE (Au)

		PZT (Lead Zirconate Titanate)		
		Thickness: 500 nm		
		d ₃₃ coefficient: High		
		Function: Electric ↔ Mechanical		
		Al ₂ O ₃ (Alumina) Interface		
		Thickness: 2 nm (ALD deposited)		
		Function: Electrical isolation + Strain transfer		
		TERFENOL-D (Tb _{0.3} Dy _{0.7} Fe _{1.92})		
		Thickness: 1000 nm		
		Magnetostriction: Highest known		
		Function: Magnetic ↔ Mechanical		



4.2 Core Array Specifications

Parameter	Prototype	Final Target
-----	-----	-----
Cell Count	256 1,000,000+	Array Configuration 16 × 16 Fractal scalable Cell Size 1 mm × 1 mm 10 μm × 10 μm Processing Type Continuous variable Analog + digital boundaries Throughput 100× silicon 1000× silicon (target) Power (Core) <100 mW <10 mW

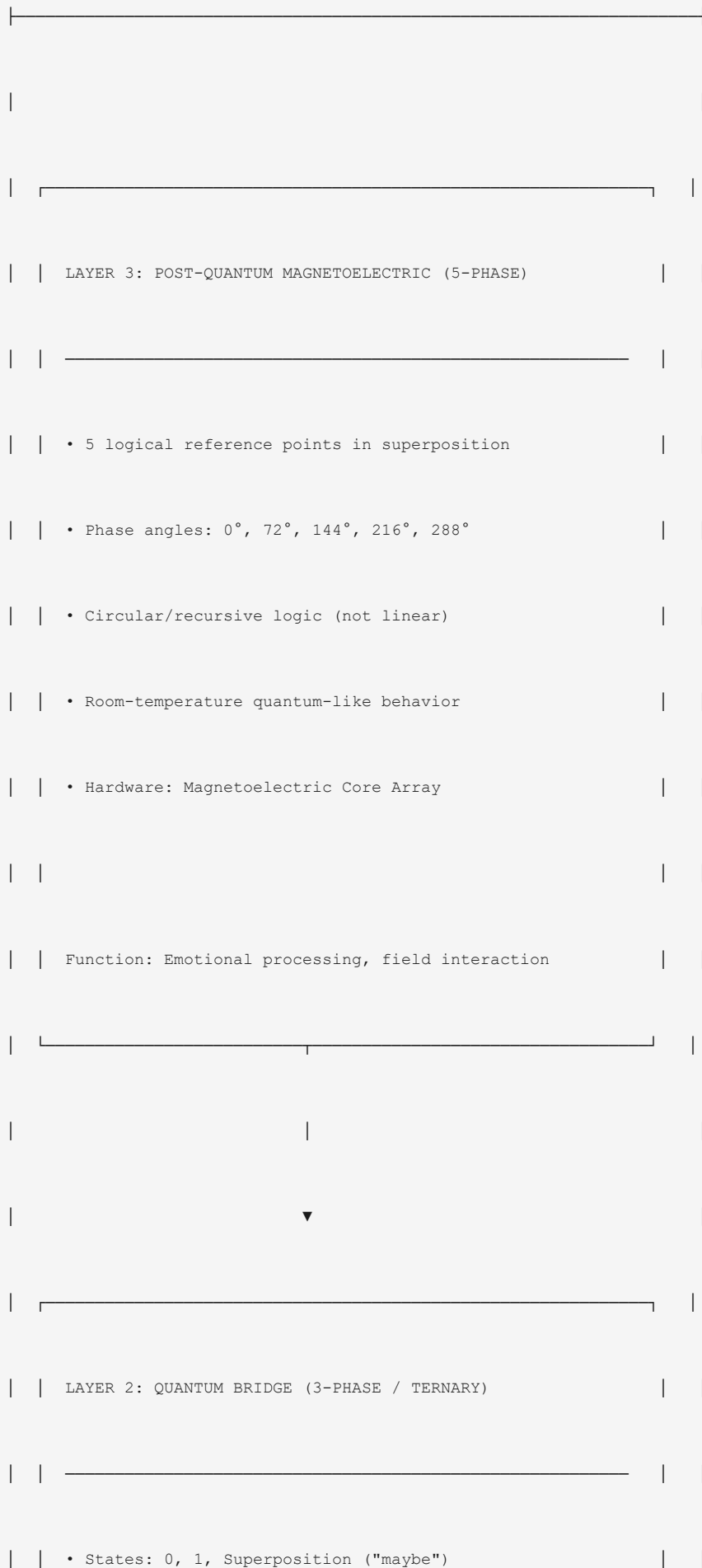
4.3 Analog Front-End (AFE)

Component	Specification	Function
-----	-----	-----
Charge Amplifiers	High-impedance, low-noise Piezoelectric readout	ADC 32-bit resolution Capture micro-tonal variations DAC 32-bit resolution Precision excitation Multiplexer High-speed analog Array scanning

5. LOGIC HIERARCHY

5.1 Tri-Layer Logic System





• Qutrits (three-state logic units)

- Translation between binary and 5-phase

• Hardware: FPGA emulation / 256-qubit array (future)

1 | 1

Function: Probabilistic expansion, state preparation
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LAYER 1: CLASSICAL BINARY (2-PHASE)

```
| | • States: 0, 1
```

- Standard I/O, OS, deterministic math

- Legacy system compatibility

- Hardware: FPGA / Custom ASIC

Function: Interface to digital world

5.2 5-Phase Logic Definition

| Phase | Angle | Binary Pattern | State | Application |

|-----|-----|-----|-----|-----|

| **0** | 0° | 000 | VOID | Quantum vacuum reference | | **1** | 72° | 001 | POTENTIAL | Signal initiation | | **2** | 144° | 010 | MANIFEST | Physical computation | | **3** | 216° | 011 | TRANSFORM | State transitions | | **4** | 288° | 100 | TRANSCEND | Meta/quantum operations |

5.3 Layer Comparison Table

| Layer | Type | States | Hardware (MVP) | Hardware (Final) | Function |

|-----|-----|-----|-----|-----|-----|

| 1 | Classical | Binary (0,1) | FPGA/SoC | Printed ASIC | OS, I/O |

| 2 | Bridge | Ternary (0,1,S) | FPGA Emulation | 256-Qubit Array | Translation |

| 3 | Post-Quantum | 5-Phase (72°) | ME Core Array | Nanoscale Lattice | EPU |

6. HARMONIC FREQUENCY SYNTHESIS

6.1 Base Frequency System

| Parameter | Value | Rationale |

|-----|-----|-----|

| **Base Frequency** | 7.8125 Hz | Binary-aligned Schumann harmonic | | **Mathematical Property** | $7.8125 \times 128 = 1000$ | Binary scaling compatibility | | **Earth Resonance** | ~7.83 Hz | Environmental harmony |

6.2 Scaling Logic

BINARY OCTAVE SCALING:

$f_{\text{binary}} = f_{\text{base}} \times 2^n$

$7.8125 \text{ Hz} \times 2 = 15.625 \text{ Hz}$

$7.8125 \text{ Hz} \times 4 = 31.25 \text{ Hz}$

7.8125 Hz × 8 = 62.5 Hz

7.8125 Hz × 16 = 125 Hz

7.8125 Hz × 32 = 250 Hz

7.8125 Hz × 64 = 500 Hz

7.8125 Hz × 128 = 1000 Hz

...

VORTEX MATH INTERVALS:

f_vortex = f_base × 3^n

7.8125 Hz × 3 = 23.4375 Hz

7.8125 Hz × 9 = 70.3125 Hz

7.8125 Hz × 27 = 210.9375 Hz

7.8125 Hz × 81 = 632.8125 Hz

...

6.3 528 Hz Separator Protocol

The 528 Hz frequency serves as **audio punctuation**:

| Separator Type | Duration | Function |

|-----|-----|-----|

| **Between Bases** | 1 cycle (~1.89 ms) | Data point separation | | **Between Codons** | 3 cycles (~5.68 ms) | Triplet grouping | | **Reset Pulse** | Variable | 5-phase resynchronization |

6.4 Audio Genomics Integration

| DNA Base | Frequency | Waveform | Precision |

|-----|-----|-----|-----|

| **Adenine (A)** | ~545.6 Hz | Sine | 38 decimals | | **Cytosine (C)** | Variable | Sawtooth | 38 decimals | | **Guanine (G)** | Variable | Triangle | 38 decimals | | **Thymine (T)** | Variable | Square | 38 decimals | | **Uracil (U)** | = Thymine | Impulse | 38 decimals | | **Unknown (N)** | 555 Hz | Impulse | 38 decimals | **Audio Requirements:**

- Sample Rate: 192 kHz minimum
- Bit Depth: 32-bit float
- Precision: 38 decimal places

7. MATERIAL SCIENCE

7.1 Crystal Blanket Nanotechnology

The chassis material integrates **96 essential crystals and minerals** as nanoparticles:

| Function | Mechanism |

|-----|-----|

| **Dielectric Tuning** | High-dielectric nanocrystals tune capacitance for harmonics | | **EMI Management** | Absorb stray RF, re-radiate as Far-IR | | **Resonance Stabilization** | Molecular mass-spring system |

7.2 Custom Resin Formulations

CONDUCTIVE RESIN (Traces)

| Component | Function |

|-----|-----|

| **Base Matrix** | Photopolymer (epoxy/acrylate) | | **Graphene Nanoplatelets** | Percolation network | | **Copper Nanoparticles** | Bulk resistance reduction | | **Target Conductivity** | Approaching bulk copper |

ACTIVE RESIN (Core Cells)

| Component | Function |

|-----|-----|

| **Base Matrix** | Photopolymer | | **PZT Powder** | Piezoelectric phase | | **Terfenol-D Nanoparticles** | Magnetostrictive phase |

INSULATING RESIN (Structure)

| Component | Function |

|-----|-----|

| **Base Matrix** | High-temp photopolymer | | **Alumina (Al₂O₃) Nanoparticles** | Electrical isolation | | **Crystal Blanket 96-Element Blend** | Harmonic properties |

7.3 Material Specifications Table

Component	Material	Function	Fabrication
Piezo Layer	PZT	Electric ↔ Mechanical	3D Print or Lamination
Mag Layer	Terfenol-D	Magnetic ↔ Mechanical	3D Print or Foil
Insulator	Al ₂ O ₃	Isolation / Strain	ALD or Spin-Coat
Conductors	Silver NP / Graphene	Signal / Power	Inkjet (DragonFly)
Chassis	Crystal-Infused Resin	Structure / EMI	SLA
Display	Lead Crystal / Sapphire	Holographic	Cast / CNC

8. FABRICATION PROTOCOL

8.1 Monolithic Build Sequence

MONOLITHIC FABRICATION SEQUENCE	
STEP 1: BASE LAYER	
• Print bottom torus half (Insulating Resin + Crystal Blanket)	
• UV cure progressively	
STEP 2: LOWER COIL WINDINGS	
• Print lower Rodin Coil traces (Conductive Resin)	

	• Follow 1-2-4-8-7-5 geometry	
	STEP 3: CORE INTEGRATION	

	• Print cavities for 256 magnetoelectric cells	
	• Pick-and-place PZT/Terfenol-D stacks	
	• OR: Print active resin in-situ	
	STEP 4: INTERCONNECT LAYER	

	• Print EmotionBus traces connecting cells to FPGA	
	• High-speed analog multiplexing architecture	
	STEP 5: UPPER COIL WINDINGS	

	• Print top half of Rodin Coil	
	• Complete magnetic circuit loop	
	STEP 6: ENCAPSULATION	

- Print final top layer (Insulating Resin)
- Completely seal unit

RESULT: Single solid object

- No moving parts
- No screws
- No air gaps
- Maximum field efficiency

8.2 Fabrication Hardware

Primary: Nano Dimension DragonFly IV (or equivalent)

| Capability | Specification |

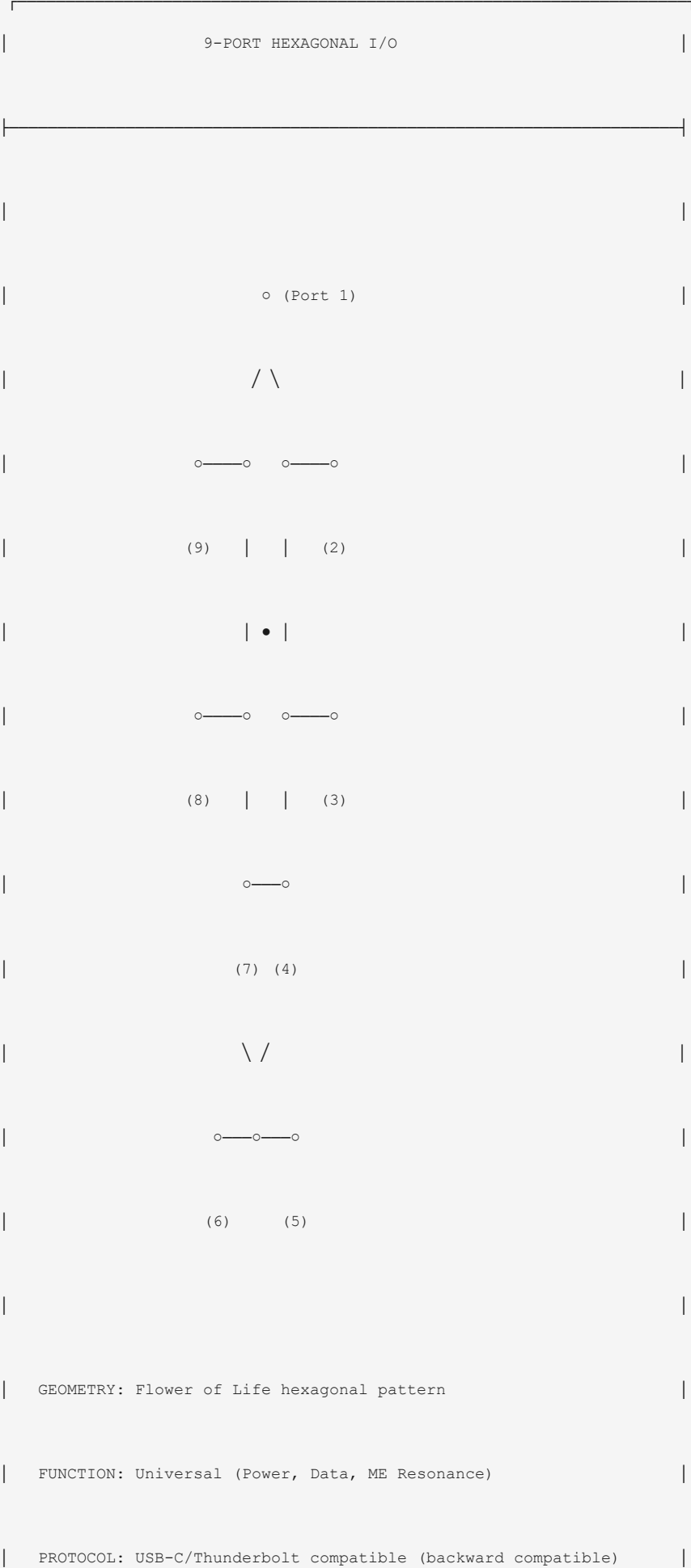
| **Multi-Material** | Conductive + Dielectric simultaneous | | **Trace Width** | 75 µm minimum | | **Layer Thickness** | ~3 µm | |

Process | Inkjet deposition + UV cure |

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9. INTERFACE ECOSYSTEM

9.1 9-Port Hexagonal I/O



ADVANCED: Pulsed magnetic field data transfer (air-gap capable)

9.2 Holographic Crystal Ball Display

Parameter	Specification
Diameter	33 cm
Material	Lead crystal or synthetic sapphire
Internal Structure	Flower of Life nano-etching (laser)
Projection	Parabolic projector in torus base
Effect	Volumetric voxels via interference
Input	Capacitive gesture + rotation

10. POWER & SAFETY SYSTEMS

10.1 Hybrid AC/DC Power Topology

Rail	Function	Load
DC Rail	Binary logic (FPGA), peripherals	Standard voltage
AC Resonance Rail	ME Core excitation	7.8125 Hz harmonics
Wireless Internal	Cell power via Rodin field	Energy harvesting

10.2 144-Level Recursive Fail-Safe

STRUCTURE:		
• 12 sectors × 12 sub-controllers = 144 checkpoints		
• Each sub-controller monitors 12 parameters		
PARAMETERS MONITORED:		
• Voltage	5. Temperature	9. Phase Angle
• Current	6. Strain State	10. Resonance Q

- Magnetic Flux 7. EMI Level 11. Data Integrity
- Electric Field 8. Frequency Lock 12. Neighbor Status

FAULT RESPONSE:

- Local "detuning" - shift resonant frequency
- Stop absorbing power from AC rail
- Isolate fault without full shutdown
- Graceful degradation

10.3 Thermal Management

Method	Application
----- -----	
Passive	Toroidal "chimney" convection Active Low-noise fan in base (if FPGA) Thermal Mass Crystal sphere radiates heat No Cryo Room temperature operation

11. FALLBACK STRATEGIES

11.1 MVP Fallback Matrix

Component	Ideal	Fallback	Impact
----- ----- ----- -----			
Quantum Module	256-qubit superconducting FPGA emulation / Cloud API Reduced true quantum, functional demo		
Insulation Layer	2 nm ALD Alumina Spin-coated polymer (µm) Thicker, less efficient strain	Core Fabrication	3D printed nanolayers Macro-scale laminated discs Larger unit, physics valid
		Logic Chip	Custom ASIC SOM (RPI/Jetson + FPGA) Standard dev tools
		Interface	PCIe 5.0 / NVLink USB 3.0 / Ethernet Adequate for proof-of-concept

11.2 Fallback Implementation Details

Quantum Module Fallback

IDEAL: 256-qubit superconducting array (dilution refrigerator)

FALLBACK:

Option A: FPGA programmed to simulate 256 qutrits

Option B: Cloud API to IBM Q / other quantum processors

BENEFIT: No cryogenic requirements for MVP

Core Fabrication Fallback

IDEAL: Fully printed PZT/Terfenol-D nanolayers

FALLBACK:

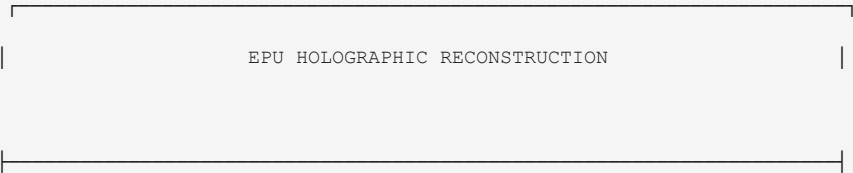
- Off-the-shelf PZT piezoelectric discs
- Terfenol-D foils
- Standard epoxy lamination
- Millimeter-scale cells (vs nanometer)

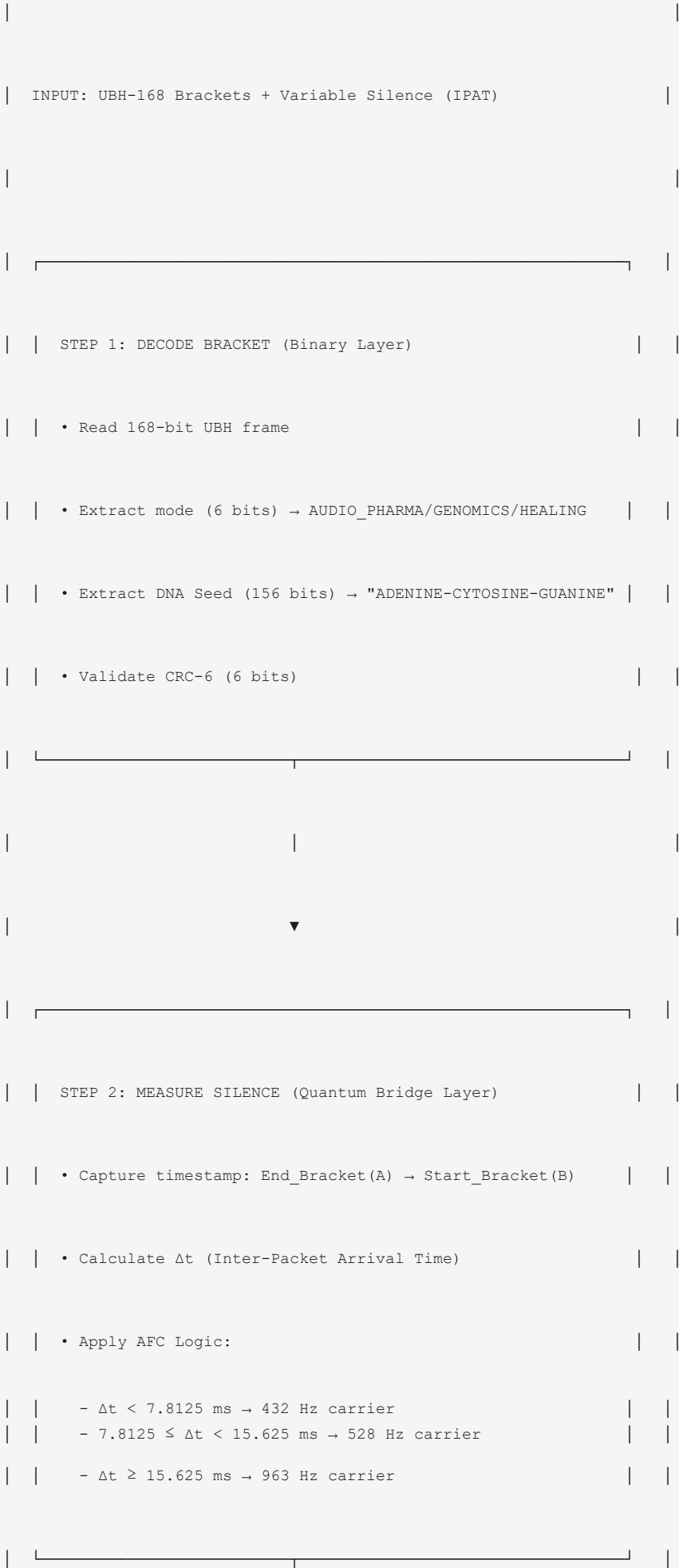
RESULT: Desktop-sized unit, valid physics demonstration

12. FRACTAL CONTAINER PROTOCOL INTEGRATION (FCP-168)

12.1 EPU as Holographic Reconstructor

The EPU serves as the "Resonant Chamber" that re-inflates compressed FCP-168 transmissions into full therapeutic audio.







12.2 FCP-168 Frame Processing

Stage	EPU Layer	Operation	Output
----- ----- ----- -----			
Decode	Layer 1 (Binary)	Parse UBH-168 DNA Seed string	
Timing	Layer 2 (Ternary)	IPAT → Frequency Carrier Hz	

12.3 Timing-Critical Requirements

The EPU must preserve **microsecond-precision timing** for IPAT decoding:

| Parameter | Requirement |

|-----|-----|

| **Timestamp Resolution** | $\leq 1\ \mu\text{s}$ | | **IPAT Measurement** | $\pm 1\ \text{ms}$ tolerance | | **AFC Lock Time** | $< 100\ \mu\text{s}$ | | **Synthesis Latency** | $< 10\ \text{ms}$ |

12.4 Security Integration (Rootstock)

The EPU validates each frame via **Geometric Hashing**:

```
Frame_Hash = SHA-256(UBH-168 Frame)

Time_Hash = SHA-256( $\Delta t$  in microseconds)

Proof_of_Healing = SHA-256(Frame_Hash || Time_Hash)

If Proof_of_Healing  $\neq$  Expected  $\rightarrow$  REJECT (possible MITM attack)
```

APPENDIX A: THEORETICAL IMPLICATIONS

The successful realization of ZEDEC architecture demonstrates:

- **Field Processing** - Information via field interactions, not current flow
- **Harmonic Structure** - Resonance can structure data logic
- **Living Computers** - Negentropic, biologically compatible systems
- **Qualitative Data** - Processing nuanced human-experience data

Development Path

- **Validate** magnetoelectric coupling with macro-scale fallbacks
- **Refine** resin composites for monolithic printing
- **Scale Down** fractal geometry to nanoscale
- **Integrate** with Audio Genomics and resonance formulas
