Основи рачунарске технике 2

Испит – Л3

Основи рачунарске технике 2

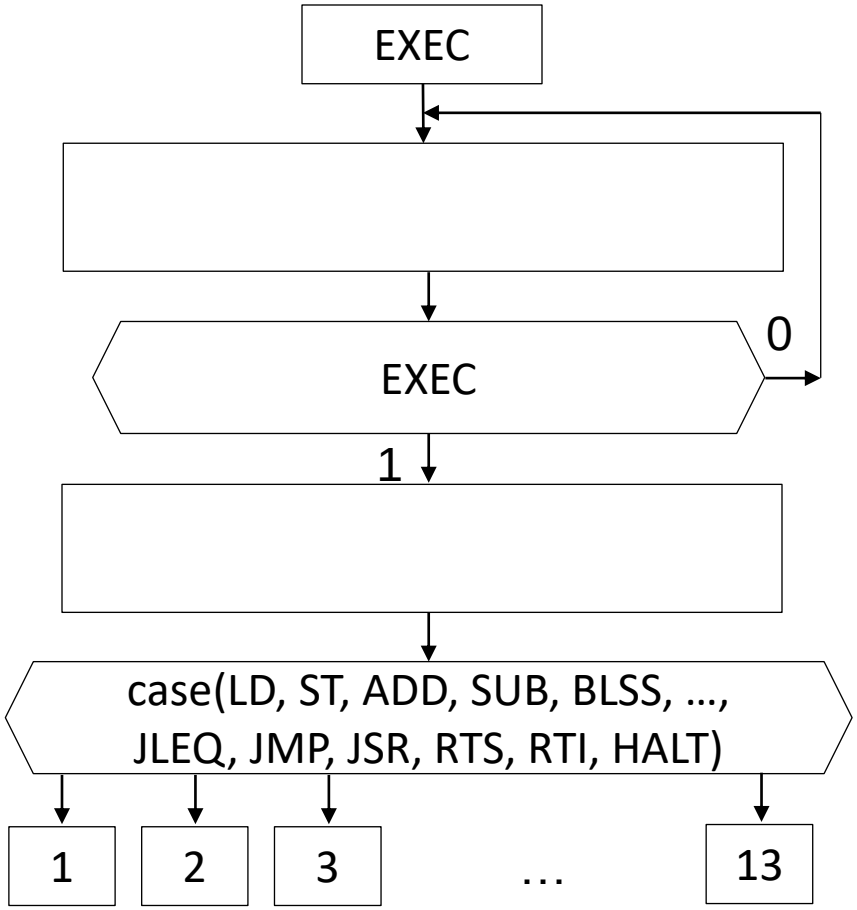
EXEC блок

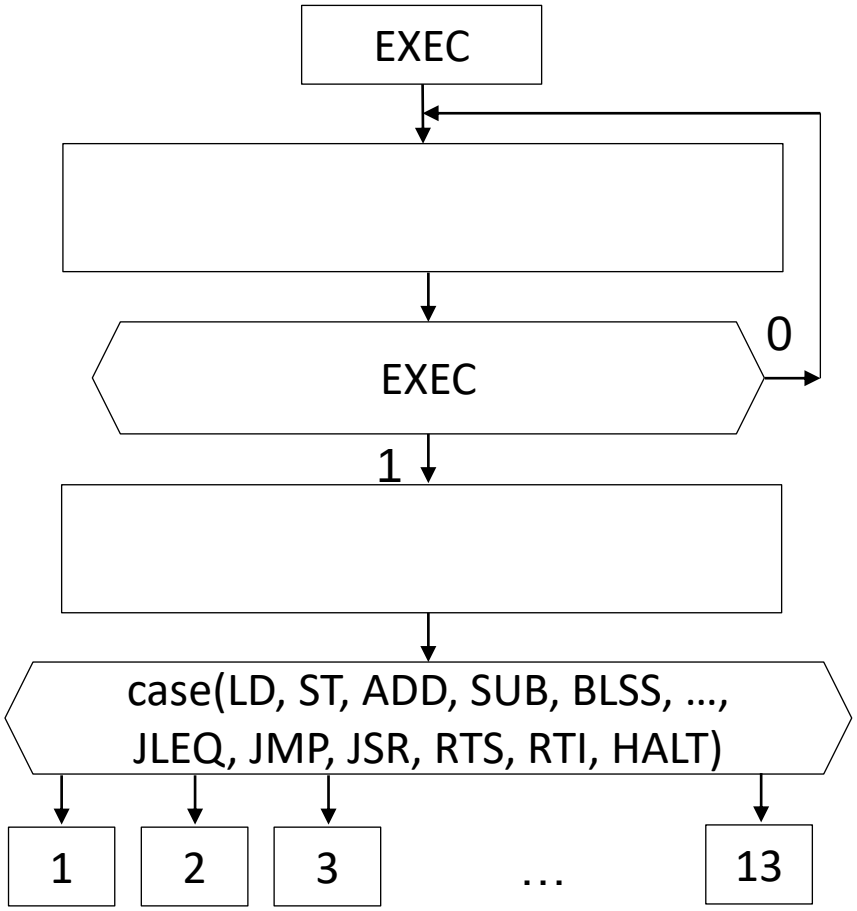
Инструкција	$IR_{23..19}$
LD	0011 0b
ST	0011 1b
ADD	0100 0b
SUB	0100 1b

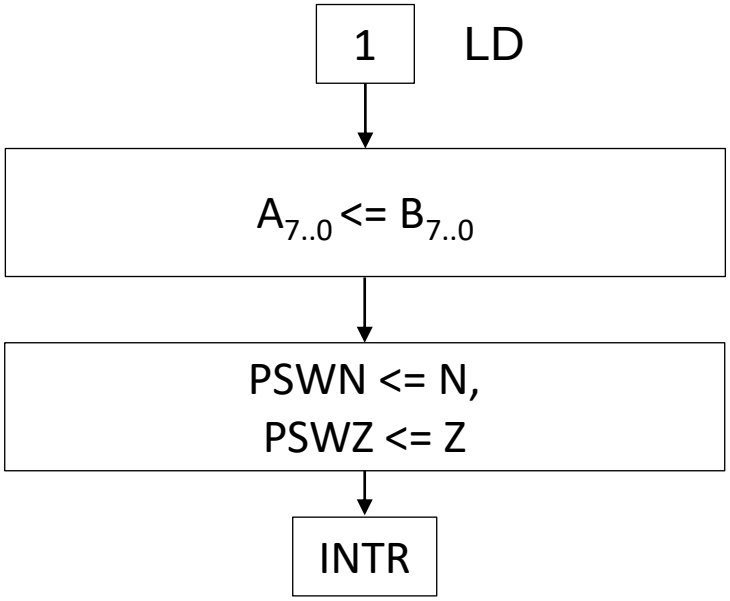
Инструкција	$IR_{23..16}$	$IR_{15..8}$	$IR_{7..0}$	Дужина
JSR	0010 0001b	млађи бајт	старији бајт	3B
JMP	0010 0000b	млађи бајт	старији бајт	3B
JLEQ	0001 0010b	млађи бајт	старији бајт	3B
BGREU	0001 0001b	померај	/	2B
BLSS	0001 0000b	померај	/	2B
POPGPR	0000 0100b	/	/	1B
PUSHGPR	0000 0011b	/	/	1B
RTI	0000 0010b	/	/	1B
RTS	0000 0001b	/	/	1B
HALT	0000 0000b	/	/	1B

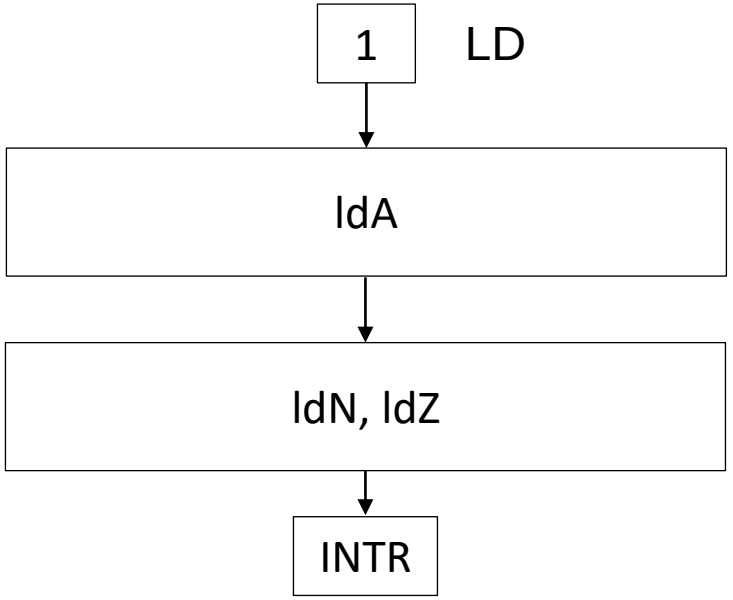
Адресирања	$IR_{18..16}$	$IR_{15..8}$	$IR_{7..0}$	Дужина
regindpom	011b	PPPP PRRRb	/	2B
regdir	010b	XXXX XRRRb	/	2B
memdir	001b	млађи бајт	старији бајт	3B
immed	000b	податак	/	2B

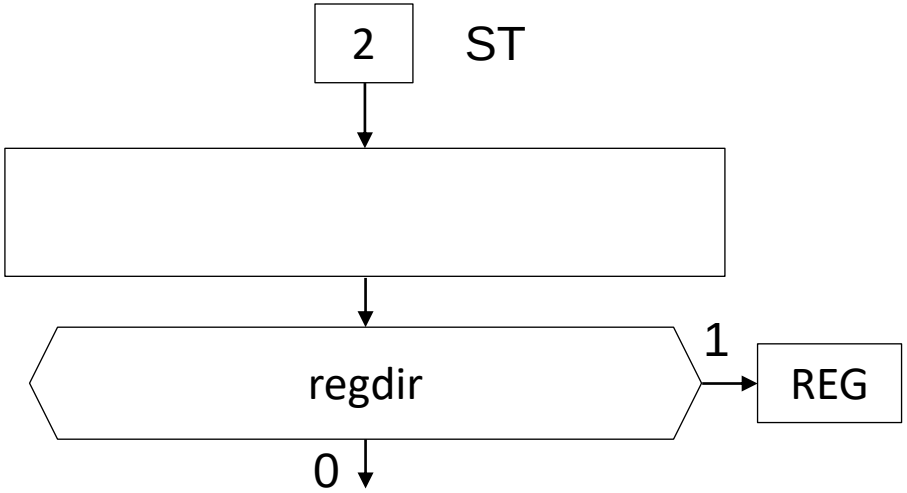
	Нижа адреса	Виша адреса
Адреса	млађи	старији

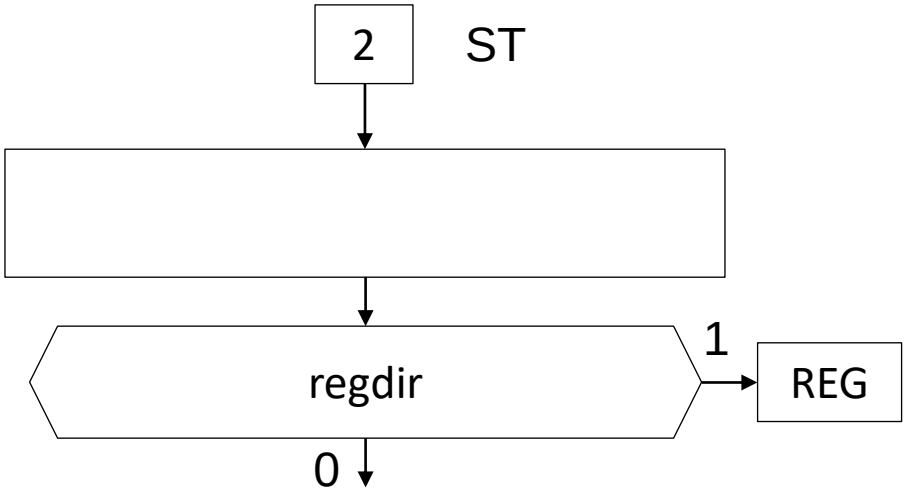

EXEC
EXEC
0
1
case(LD, ST, ADD, SUB, BLSS, …,
JLEQ, JMP, JSR, RTS, RTI, HALT)
1
2
3
…
13

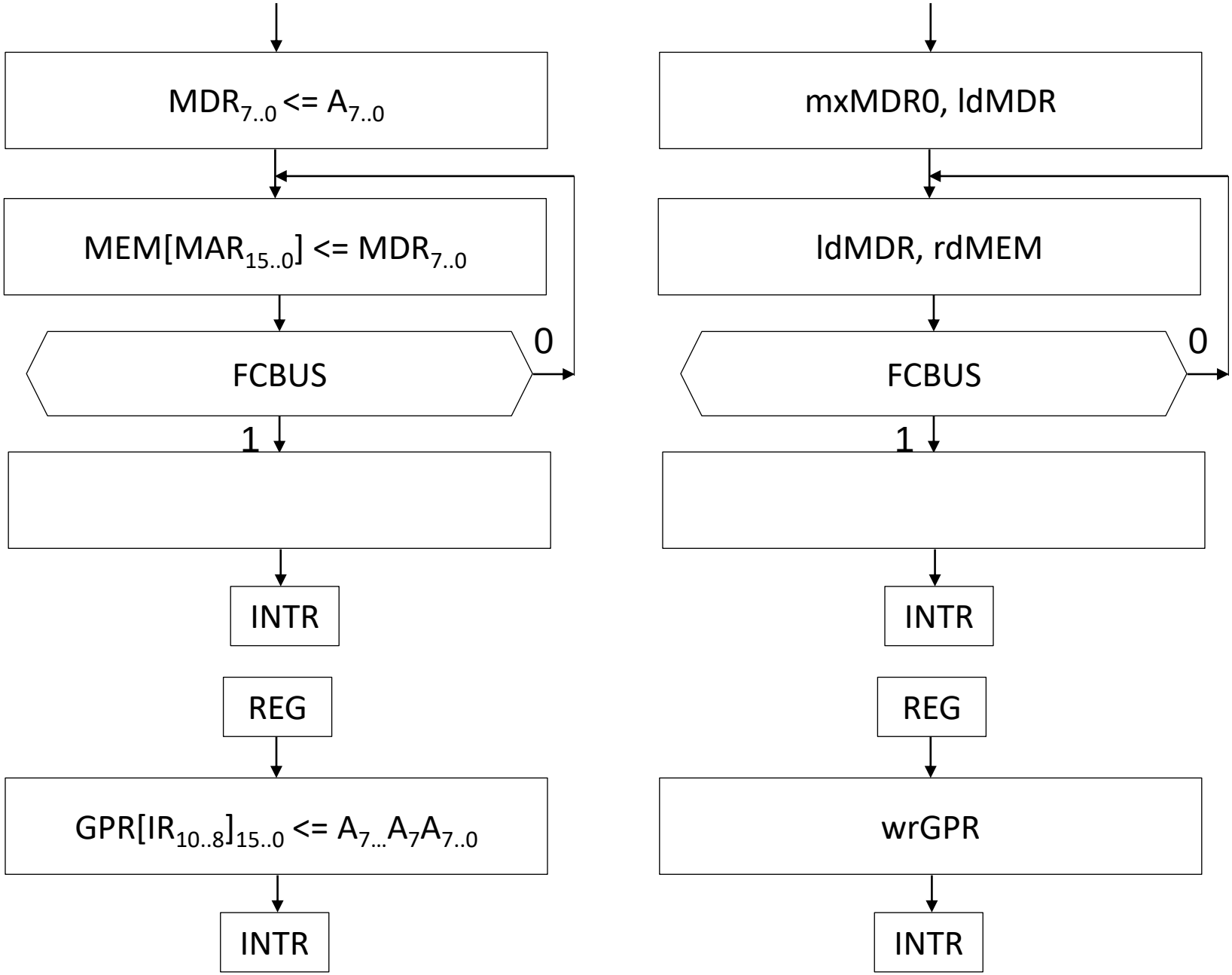

EXEC
EXEC
0
1
case(LD, ST, ADD, SUB, BLSS, …,
JLEQ, JMP, JSR, RTS, RTI, HALT)
1
2
3
…
13

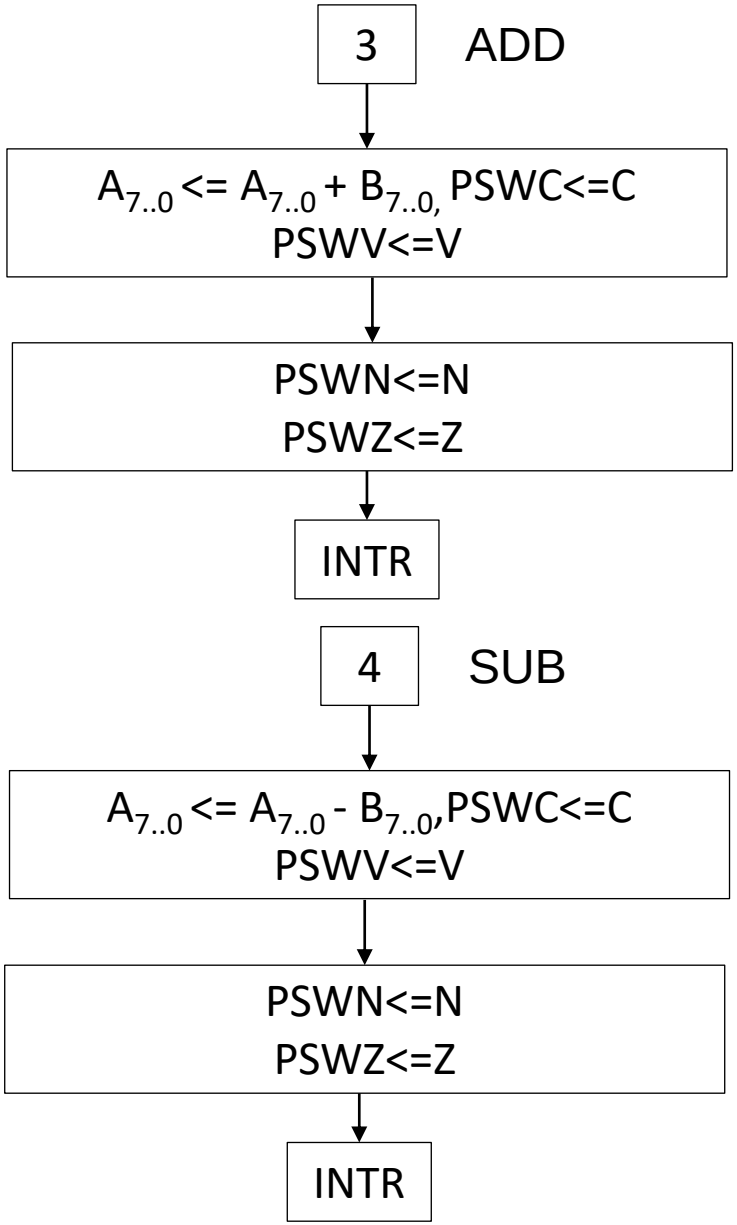

1
LD
A7..0 <= B7..0
PSWN <= N,
PSWZ <= Z
INTR

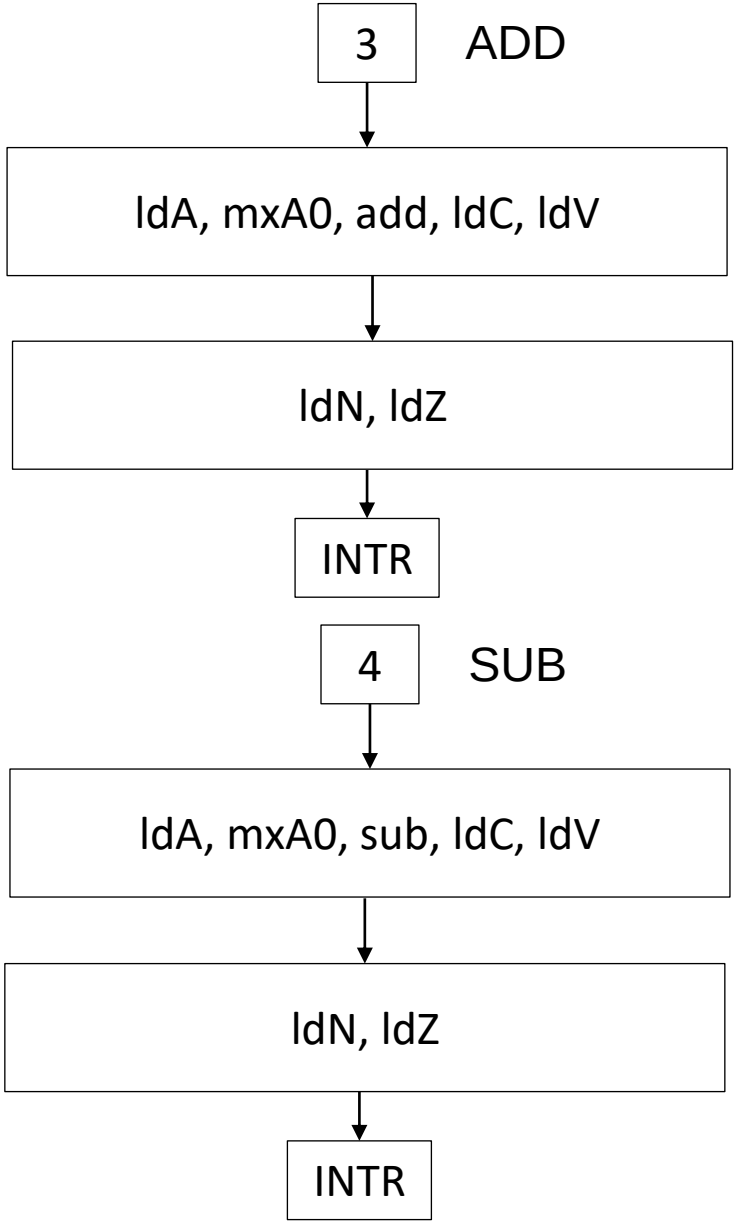

1
LD
ldA
ldN, ldZ
INTR

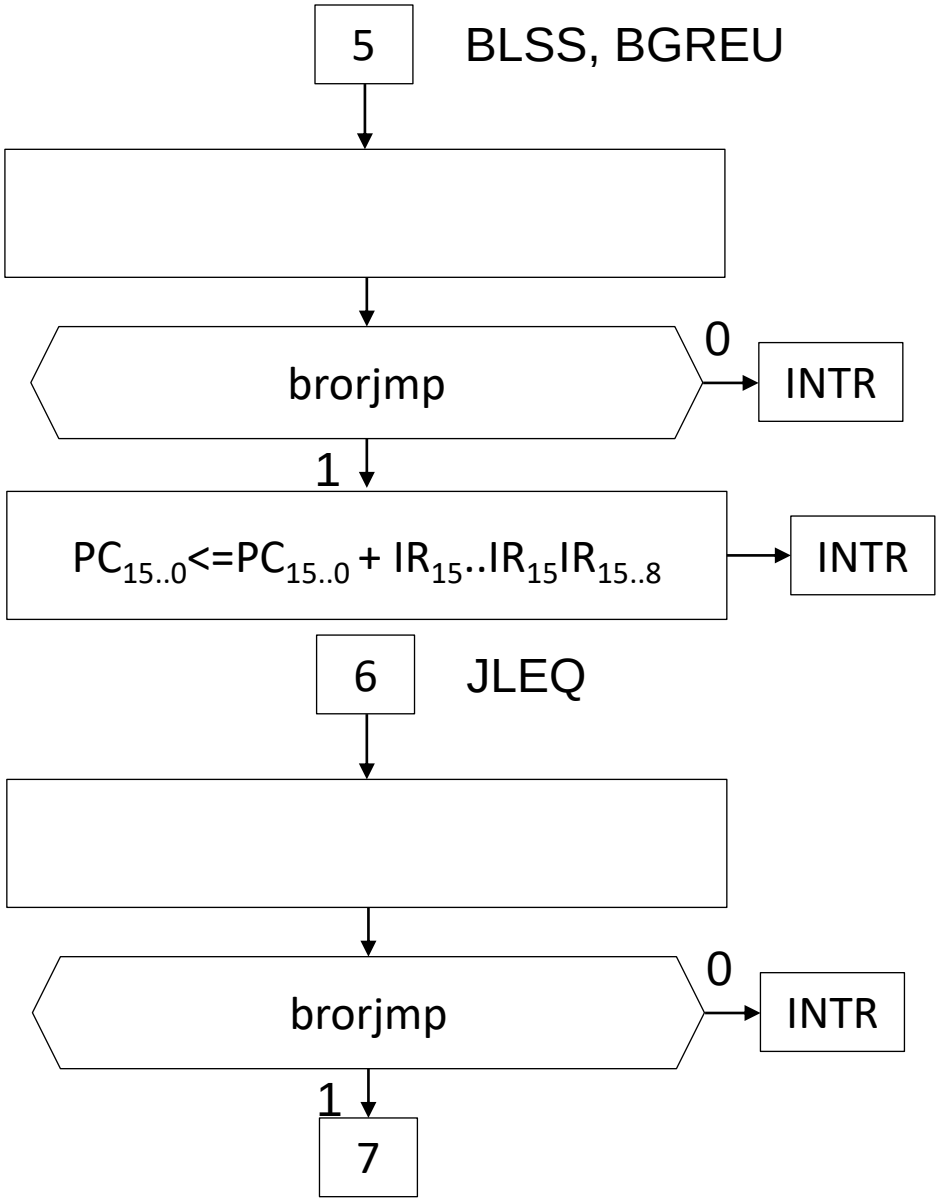

2
ST
regdir
1
REG
0

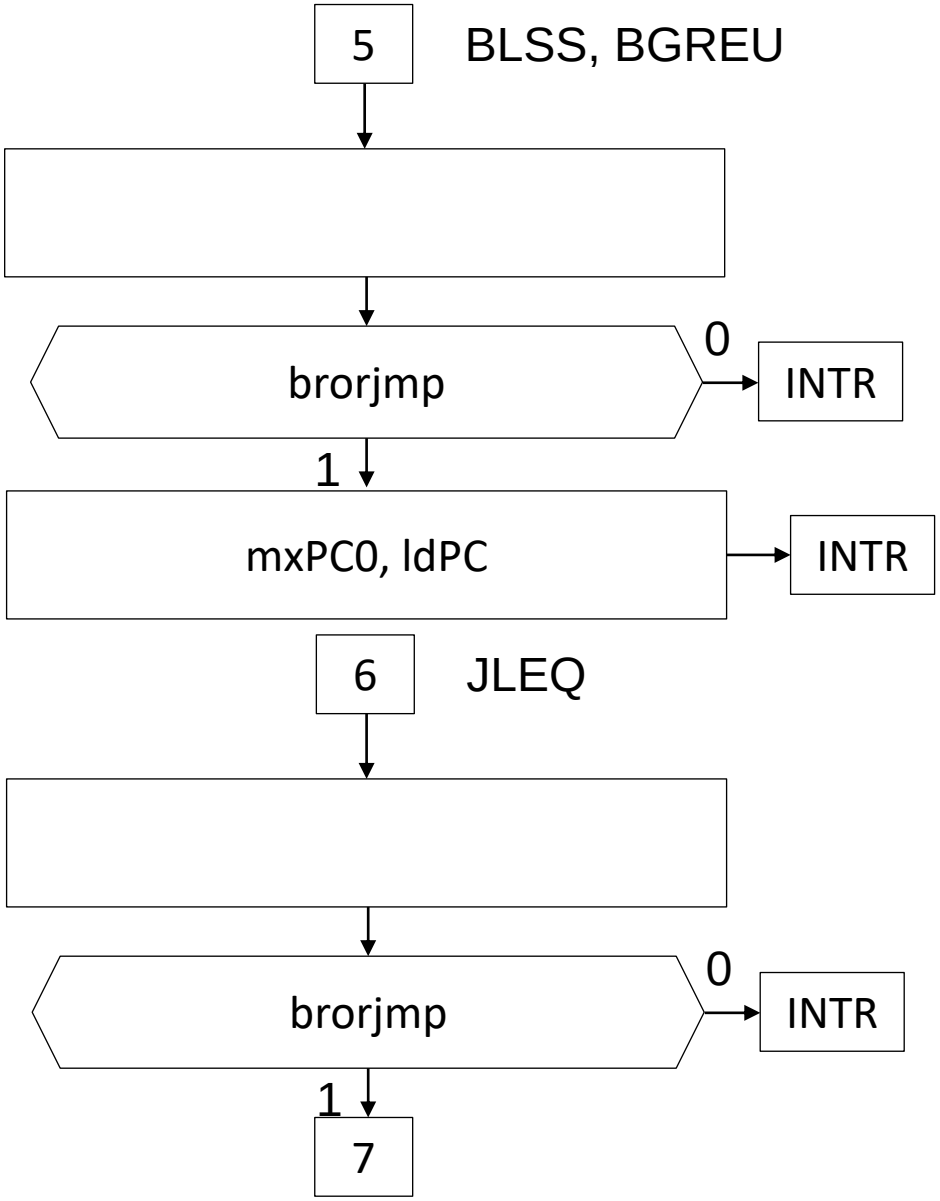

2
ST
regdir
1
REG
0

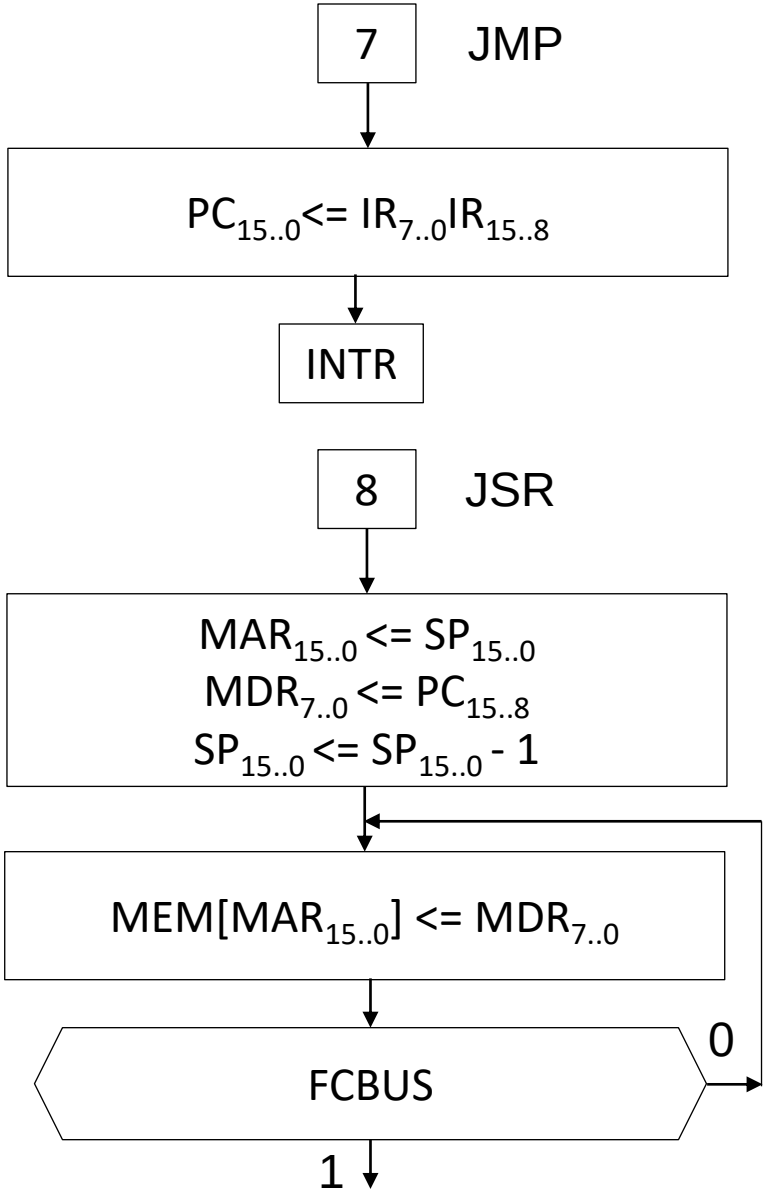

MDR7..0 <= A7..0
MEM[MAR15..0] <= MDR7..0
FCBUS
0
1
INTR
REG
GPR[IR10..8]15..0 <= A7…A7A7..0
INTR
mxMDR0, ldMDR
ldMDR, rdMEM
FCBUS
0
1
INTR
REG
wrGPR
INTR

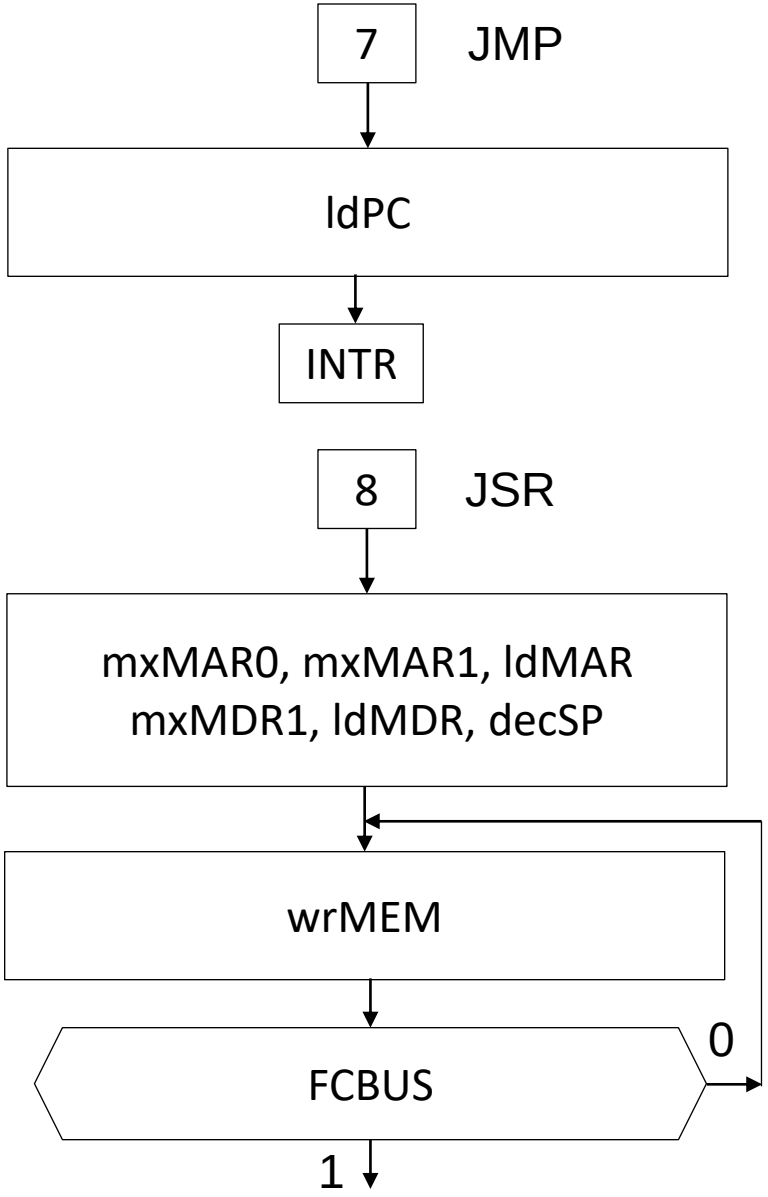

3
ADD
$A_{7..0}$ <= $A_{7..0}$ + $B_{7..0,}$ PSWC<=C
PSWV<=V
PSWN<=N
PSWZ<=Z
INTR
4
SUB
$A_{7..0}$ <= $A_{7..0}$ - $B_{7..0}$,PSWC<=C
PSWV<=V
PSWN<=N
PSWZ<=Z
INTR

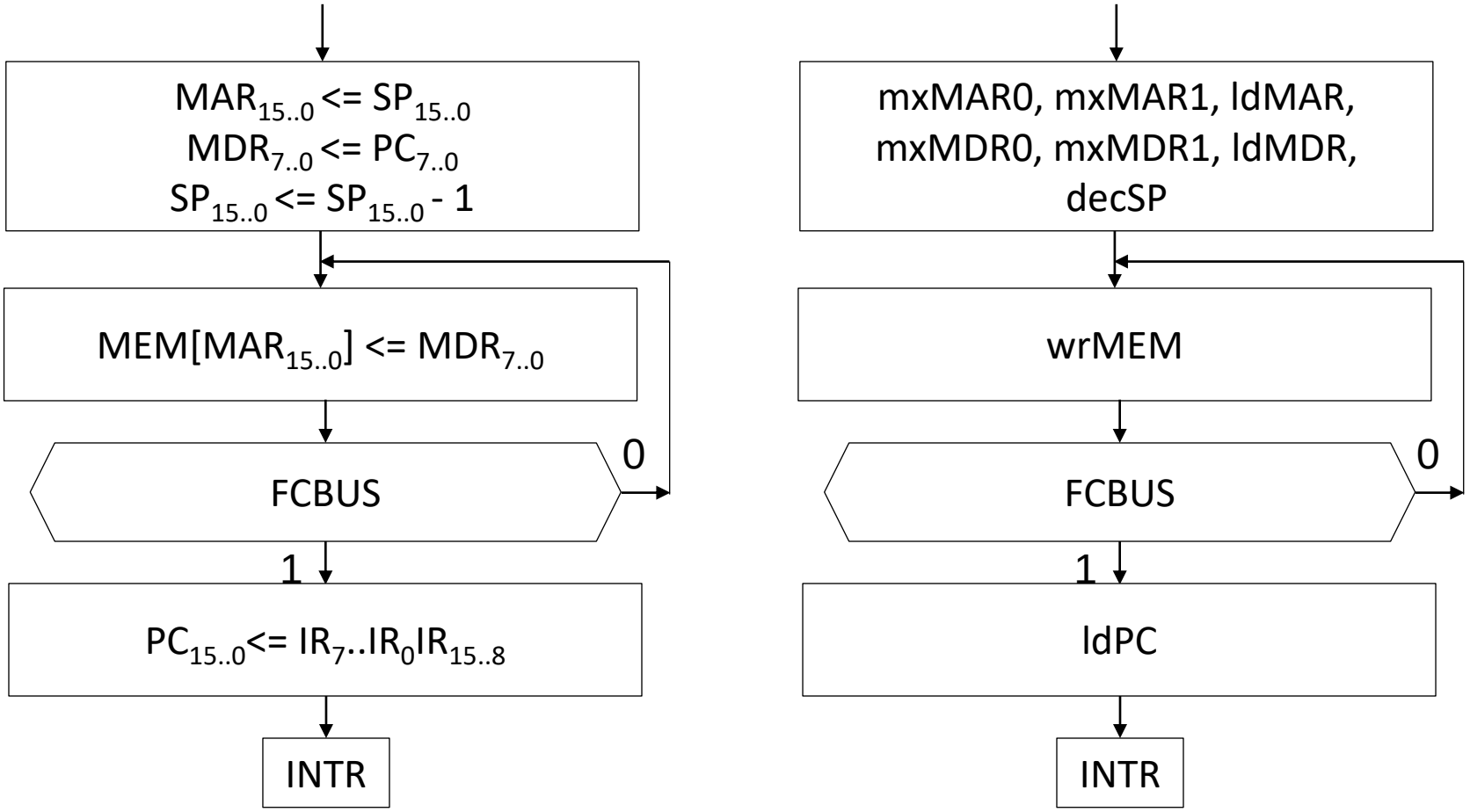

3
ADD
ldA, mxA0, add, ldC, ldV
ldN, ldZ
INTR
4
SUB
ldA, mxA0, sub, ldC, ldV
ldN, ldZ
INTR

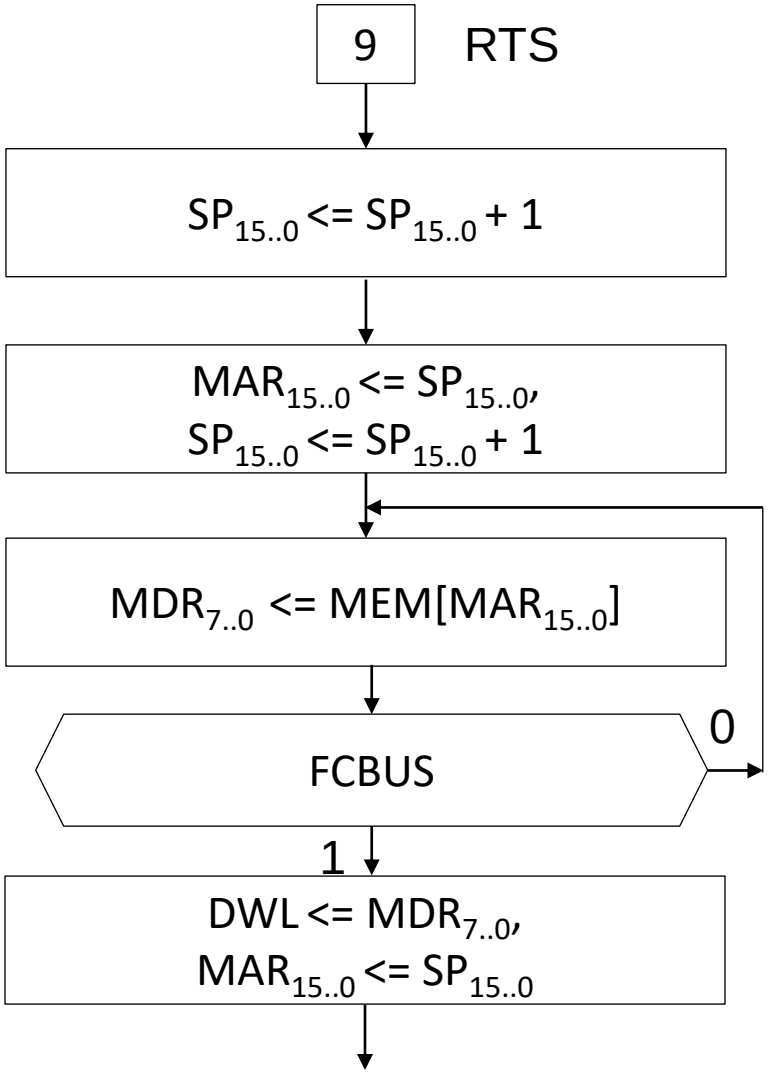

5
BLSS, BGREU
brorjmp
0
INTR
1
PC15..0<=PC15..0 + IR15..IR15IR15..8
INTR
6
JLEQ
brorjmp
0
INTR
1
7

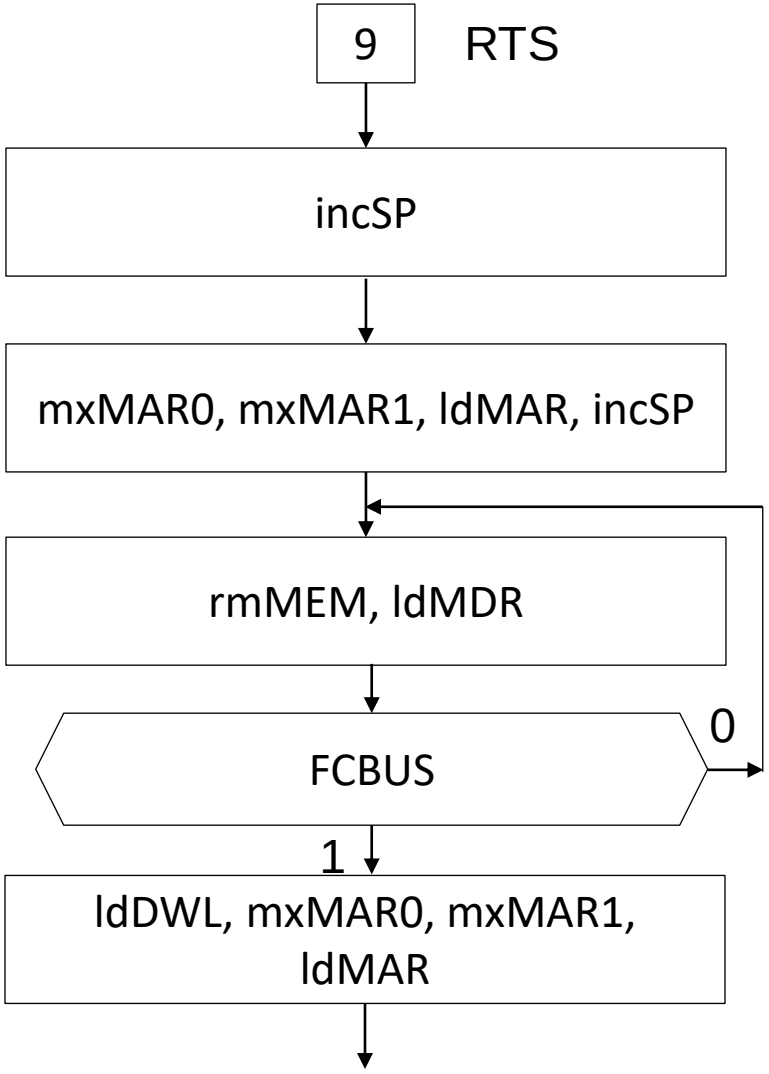

5
BLSS, BGREU
brorjmp
0
INTR
1
mxPC0, ldPC
INTR
6
JLEQ
brorjmp
0
INTR
1
7

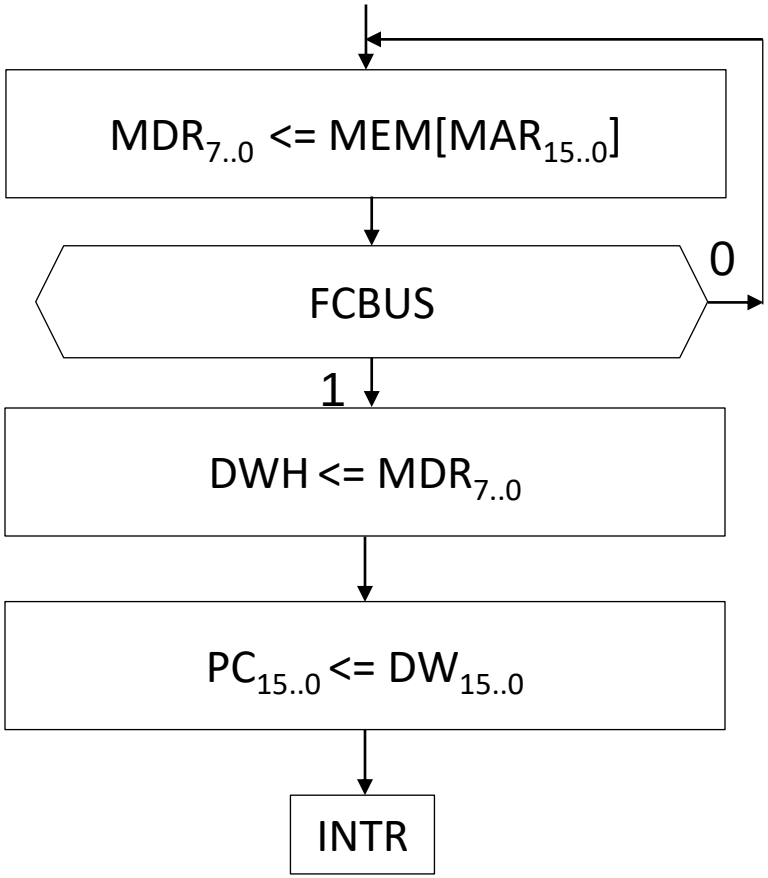

7
JMP
PC15..0<= IR7..0IR15..8
INTR
8
JSR
MAR15..0 <= SP15..0
MDR7..0 <= PC15..8
SP15..0 <= SP15..0 - 1
MEM[MAR15..0] <= MDR7..0
FCBUS
0
1

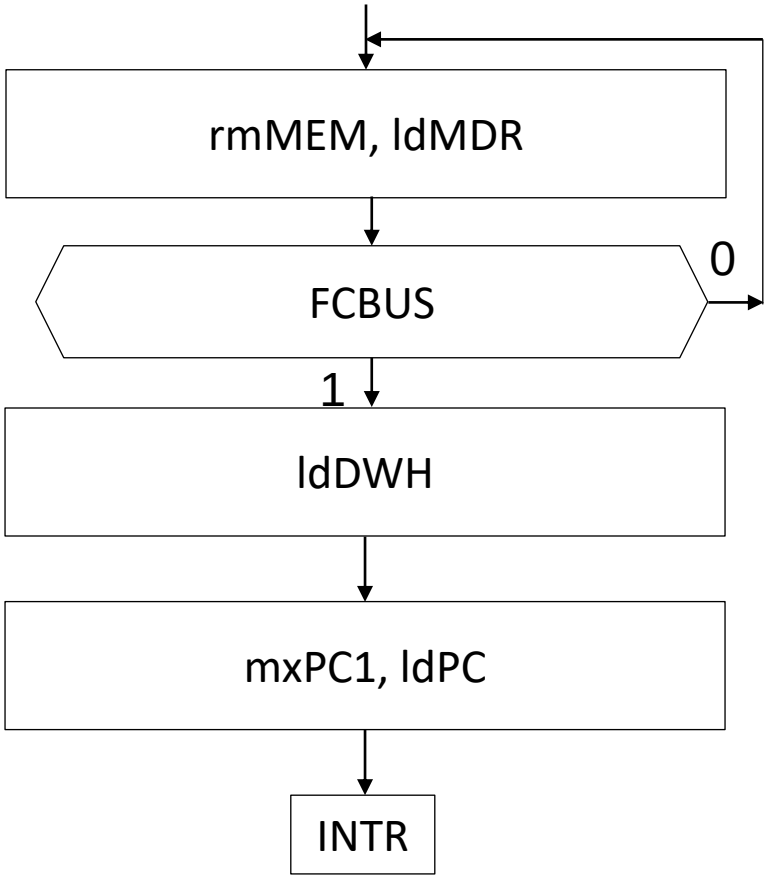

7
JMP
ldPC
INTR
8
JSR
mxMAR0, mxMAR1, ldMAR
mxMDR1, ldMDR, decSP
wrMEM
FCBUS
0
1

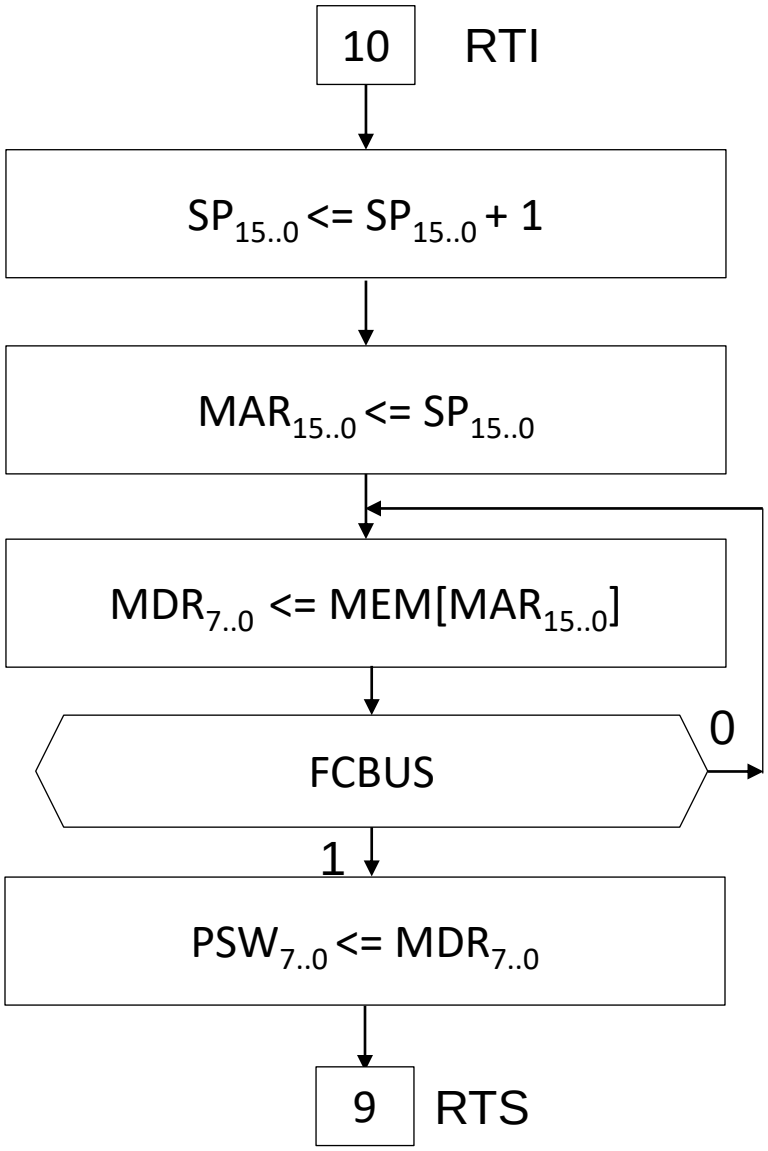

$MAR_{15..0} <= SP_{15..0}$
$MDR_{7..0} <= PC_{7..0}$
$SP_{15..0} <= SP_{15..0} - 1$
$MEM[MAR_{15..0}] <= MDR_{7..0}$
FCBUS
0
1
$PC_{15..0} <= IR_7..IR_0IR_{15..8}$
INTR
mxMAR0, mxMAR1, ldMAR,
mxMDR0, mxMDR1, ldMDR,
decSP
wrMEM
FCBUS
0
1
ldPC
INTR

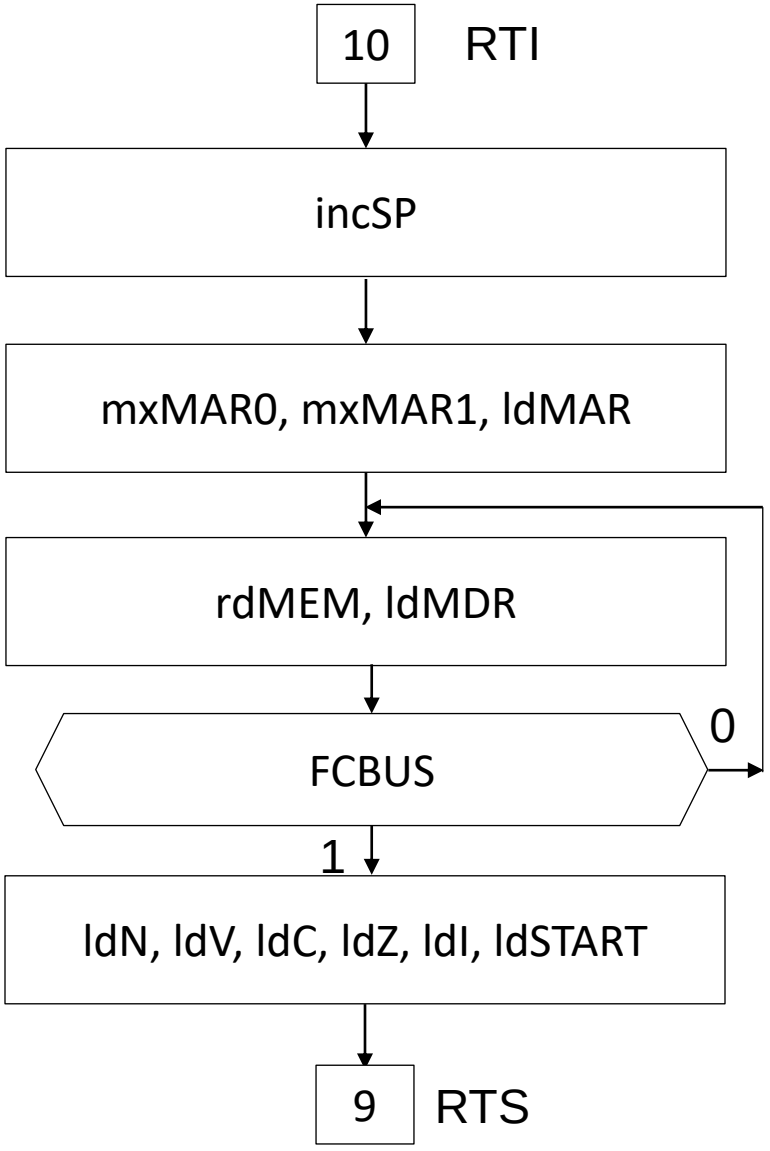

9
RTS
SP15..0 <= SP15..0 + 1
MAR15..0 <= SP15..0,
SP15..0 <= SP15..0 + 1
MDR7..0 <= MEM[MAR15..0]
FCBUS
0
1
DWL <= MDR7..0,
MAR15..0 <= SP15..0

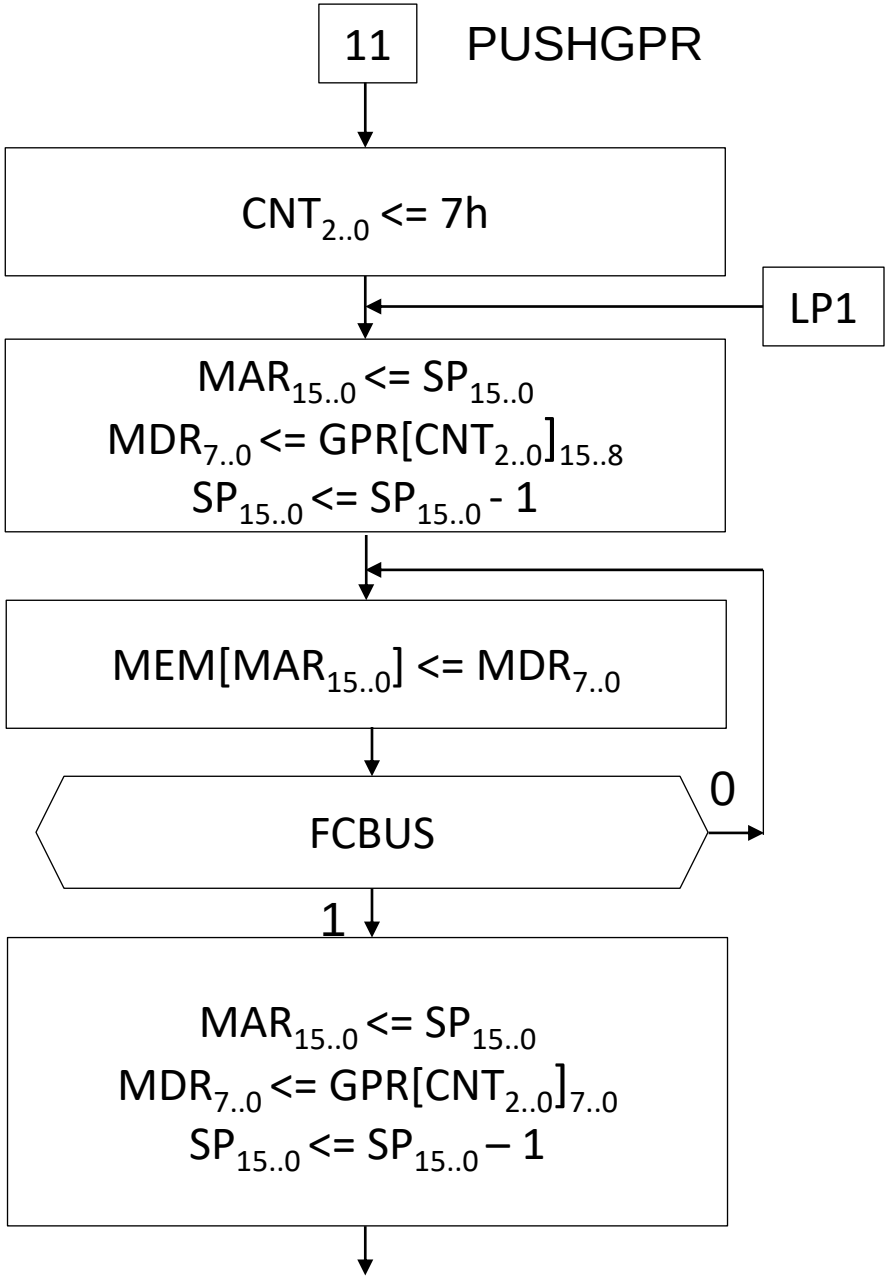

9
RTS
incSP
mxMAR0, mxMAR1, ldMAR, incSP
rmMEM, ldMDR
FCBUS
0
1
ldDWL, mxMAR0, mxMAR1,
ldMAR

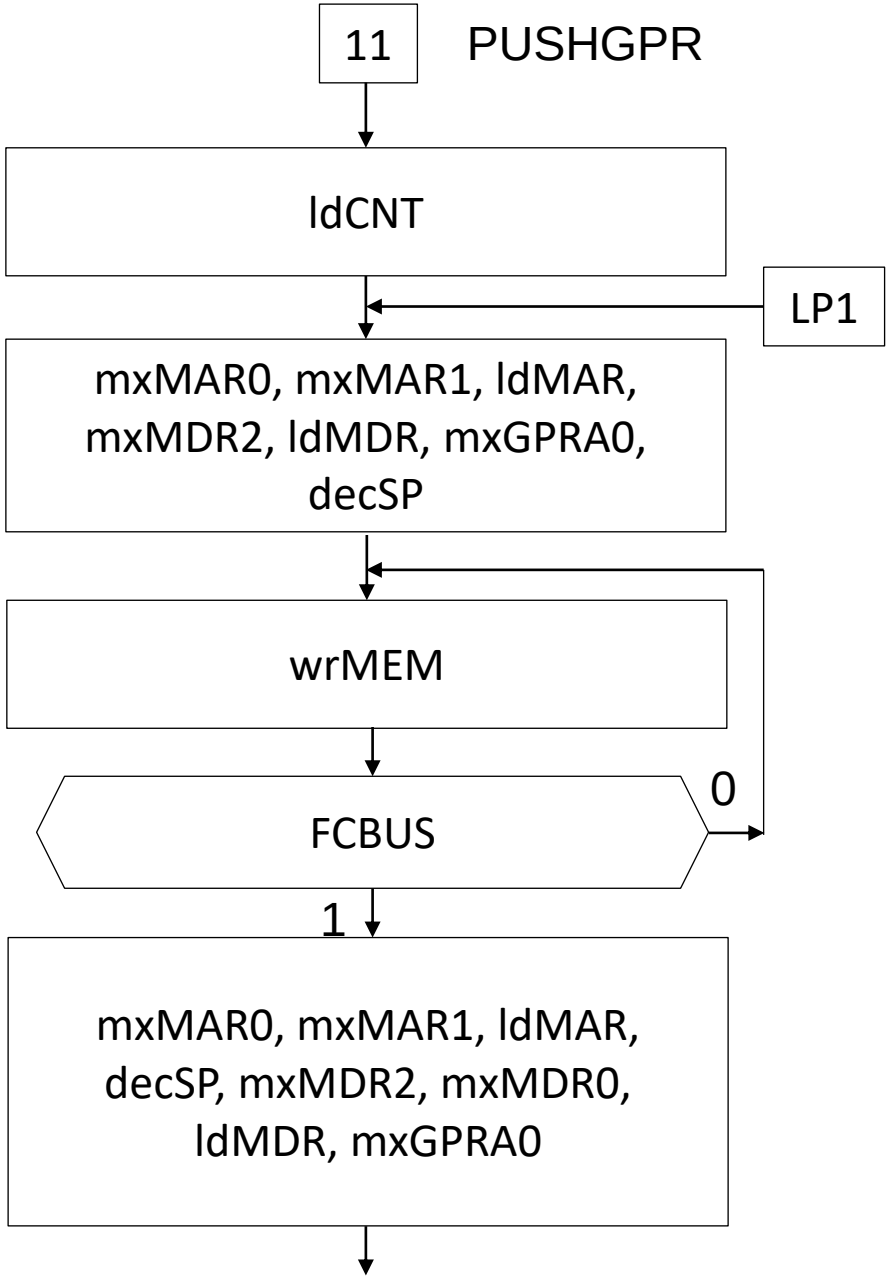

MDR7..0 <= MEM[MAR15..0]
FCBUS
0
1
DWH <= MDR7..0
PC15..0 <= DW15..0
INTR

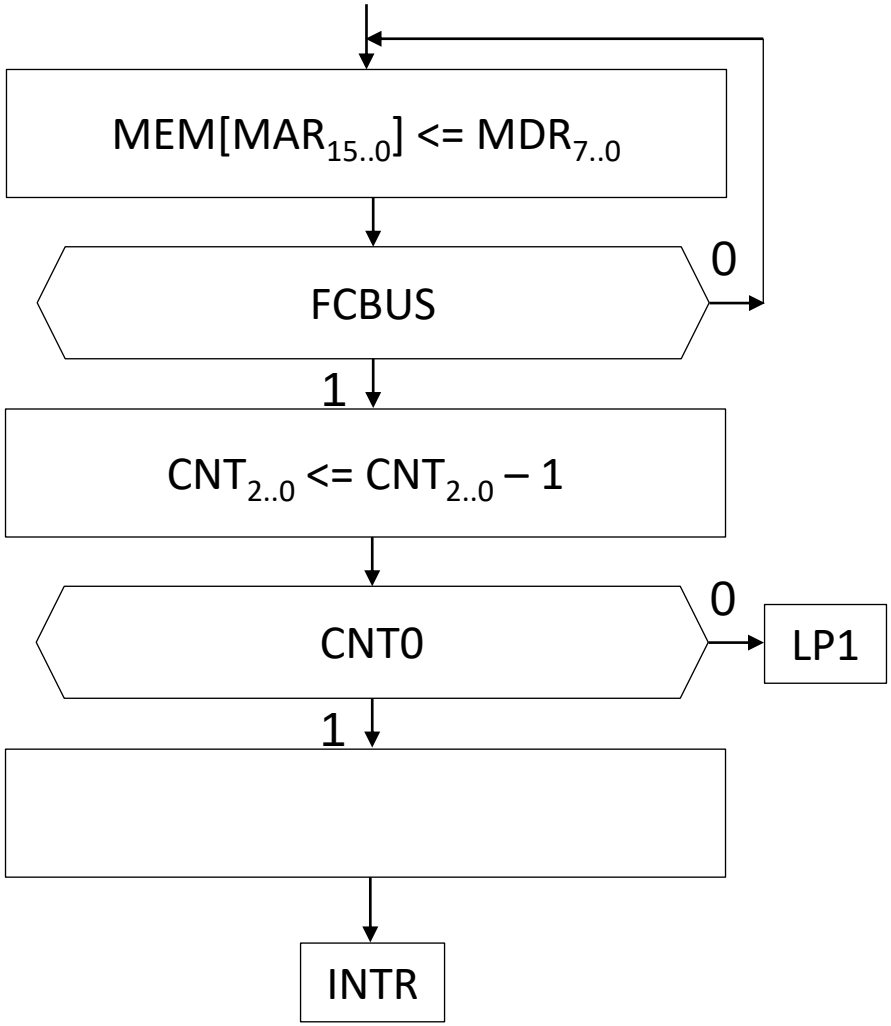

rmMEM, ldMDR
FCBUS
0
1
ldDWH
mxPC1, ldPC
INTR

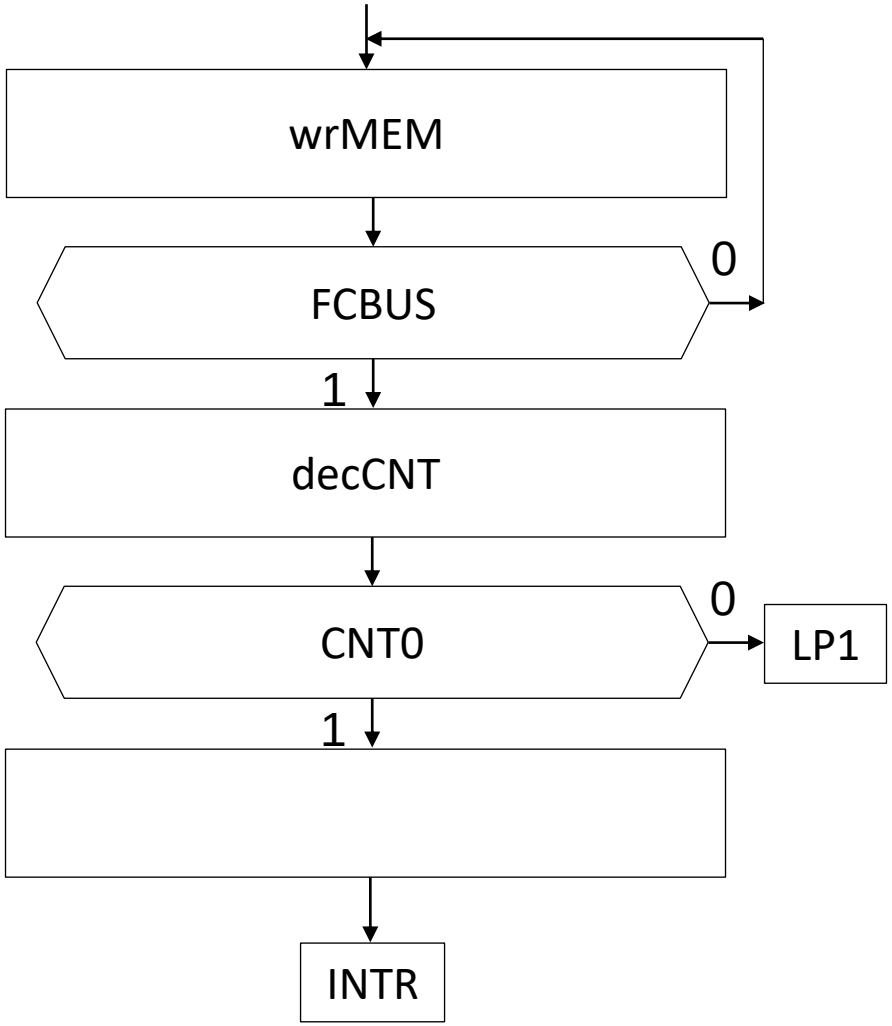

10
RTI
SP15..0 <= SP15..0 + 1
MAR15..0 <= SP15..0
MDR7..0 <= MEM[MAR15..0]
FCBUS
0
1
PSW7..0 <= MDR7..0
9
RTS

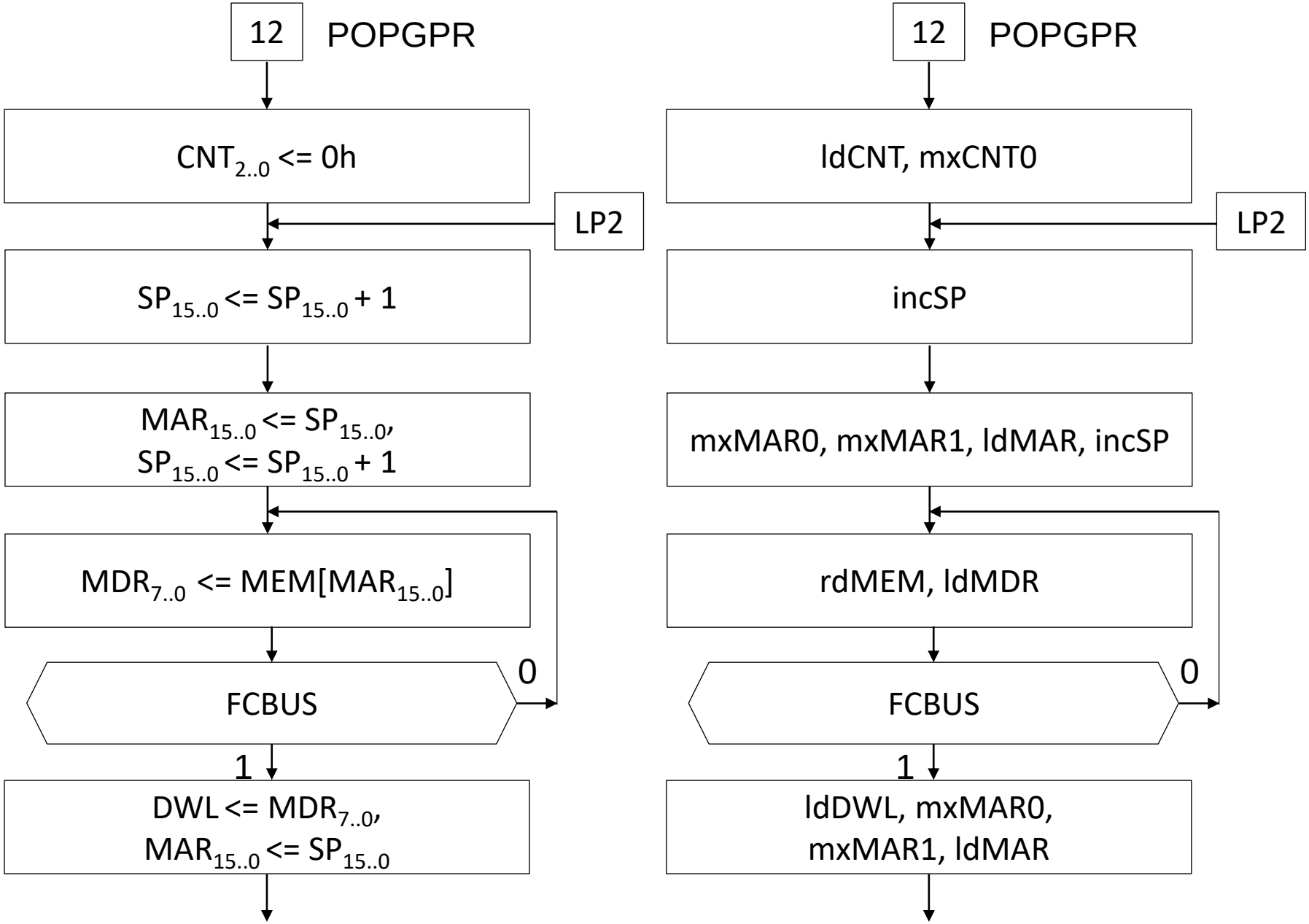

10
RTI
incSP
mxMAR0, mxMAR1, ldMAR
rdMEM, ldMDR
FCBUS
0
1
ldN, ldV, ldC, ldZ, ldI, ldSTART
9
RTS

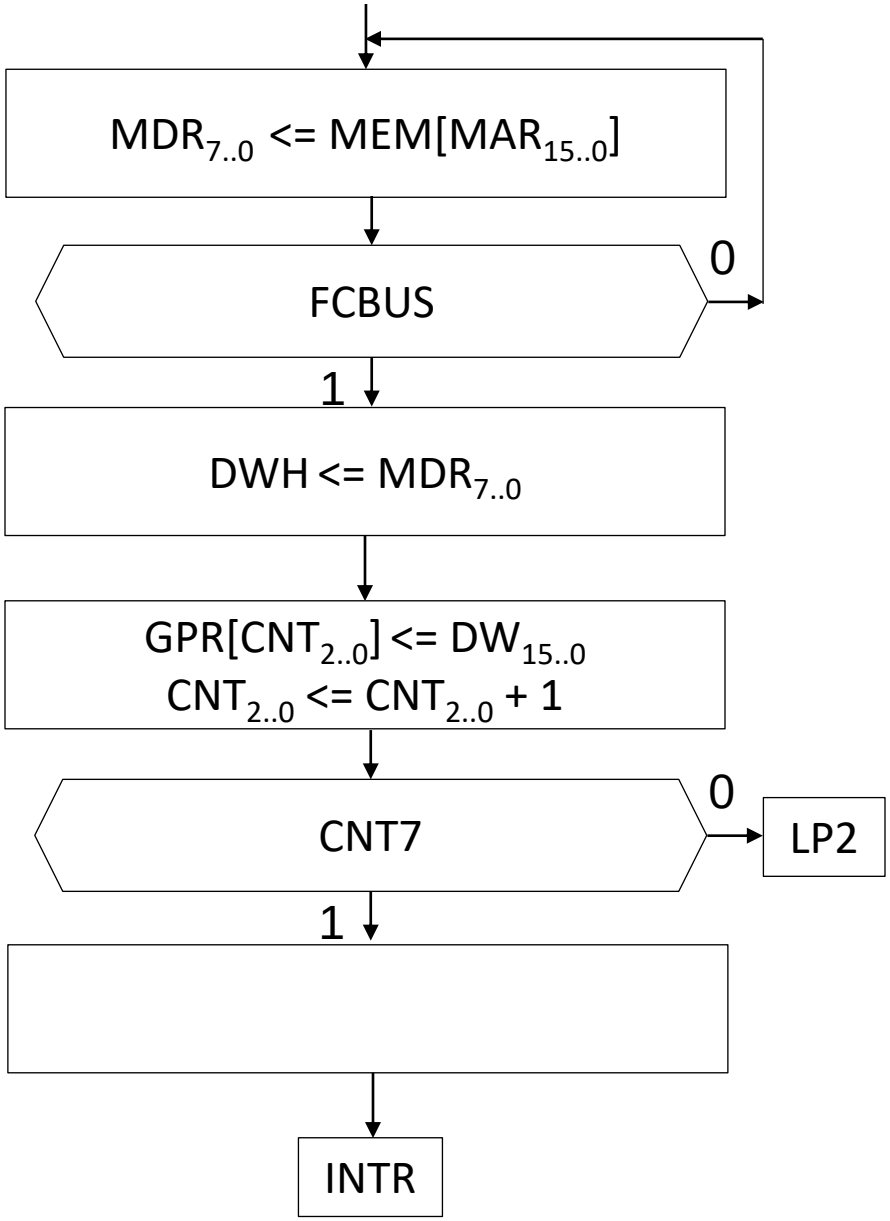

11
PUSHGPR
CNT2..0 <= 7h
LP1
MAR15..0 <= SP15..0
MDR7..0 <= GPR[CNT2..0]15..8
SP15..0 <= SP15..0 - 1
MEM[MAR15..0] <= MDR7..0
FCBUS
0
1
MAR15..0 <= SP15..0
MDR7..0 <= GPR[CNT2..0]7..0
SP15..0 <= SP15..0 – 1

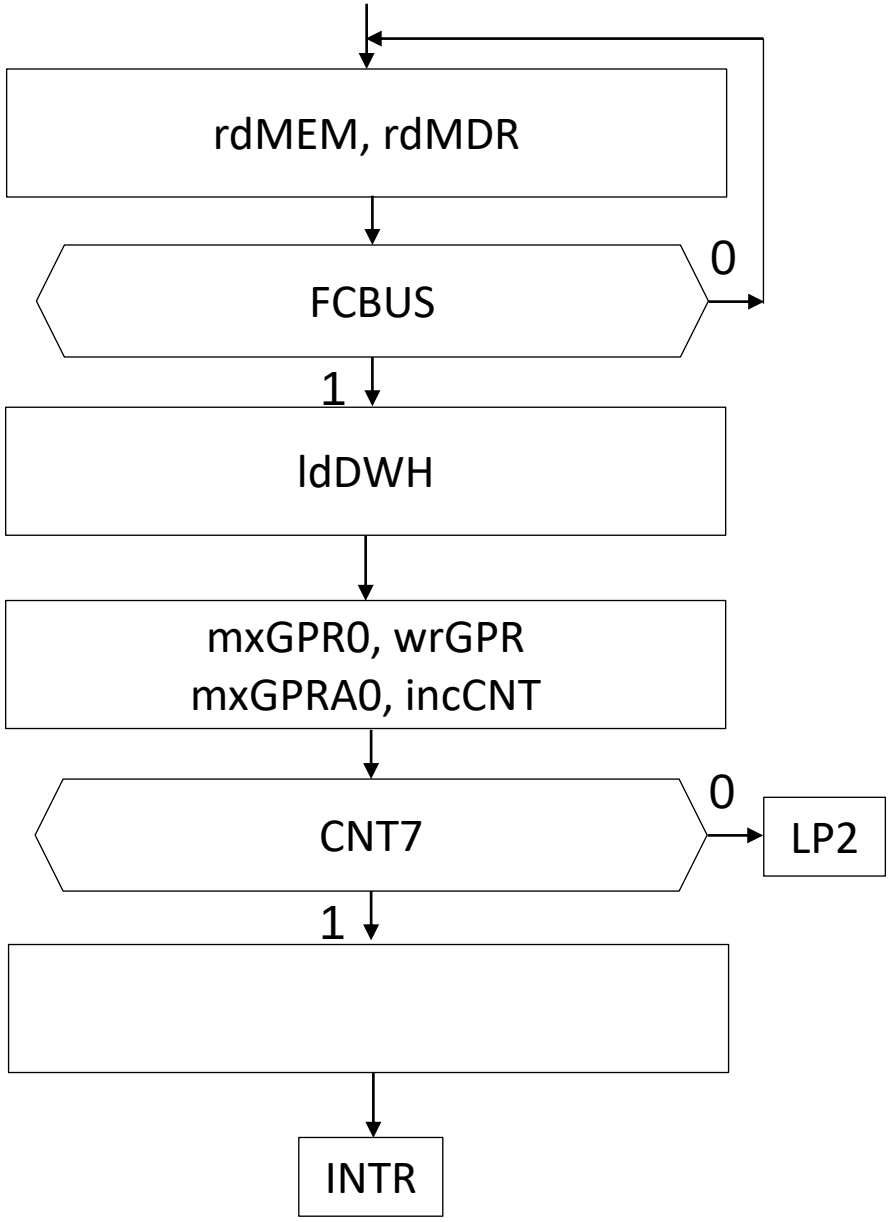

11
PUSHGPR
ldCNT
LP1
mxMAR0, mxMAR1, ldMAR,
mxMDR2, ldMDR, mxGPRA0,
decSP
wrMEM
FCBUS
0
1
mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR2, mxMDR0,
ldMDR, mxGPRA0

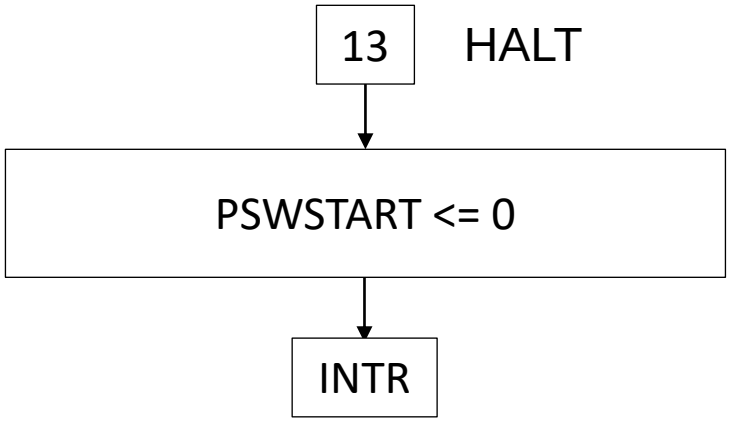

MEM[MAR15..0] <= MDR7..0
FCBUS
0
1
CNT2..0 <= CNT2..0 – 1
CNT0
0
LP1
1
INTR

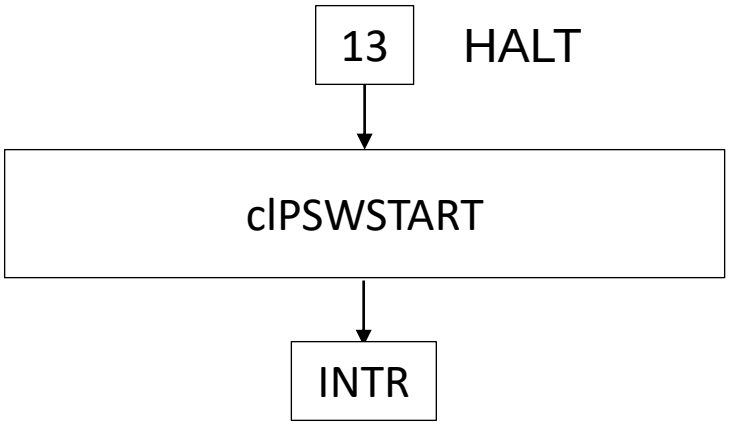

wrMEM
FCBUS
0
1
decCNT
CNT0
0
LP1
1
INTR

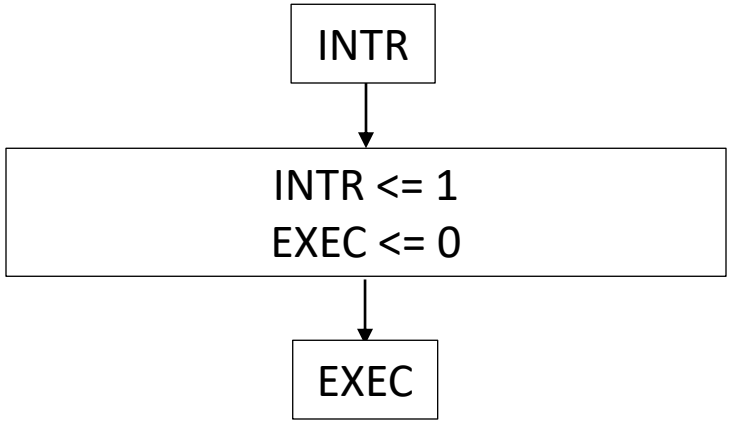

12
POPGPR
CNT2..0 <= 0h
LP2
SP15..0 <= SP15..0 + 1
MAR15..0 <= SP15..0,
SP15..0 <= SP15..0 + 1
MDR7..0 <= MEM[MAR15..0]
FCBUS
0
1
DWL <= MDR7..0,
MAR15..0 <= SP15..0
12
POPGPR
ldCNT, mxCNT0
LP2
incSP
mxMAR0, mxMAR1, ldMAR, incSP
rdMEM, ldMDR
FCBUS
0
1
ldDWL, mxMAR0,
mxMAR1, ldMAR

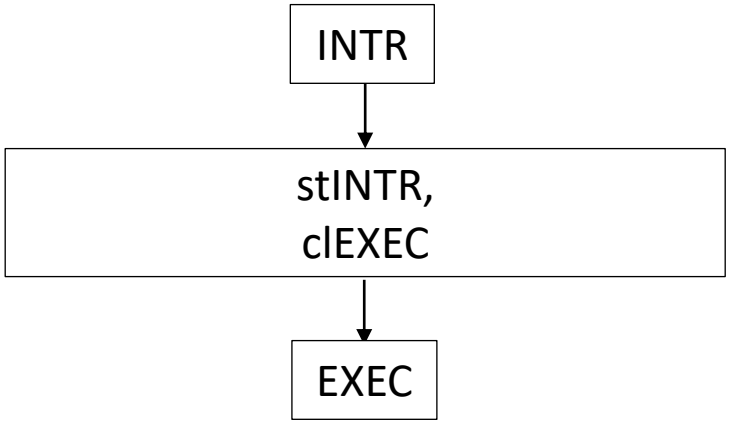

MDR7..0 <= MEM[MAR15..0]
FCBUS
0
1
DWH <= MDR7..0
GPR[CNT2..0] <= DW15..0
CNT2..0 <= CNT2..0 + 1
CNT7
0
LP2
1
INTR


rdMEM, rdMDR
FCBUS
0
1
ldDWH
mxGPR0, wrGPR
mxGPRA0, incCNT
CNT7
0
LP2
1
INTR

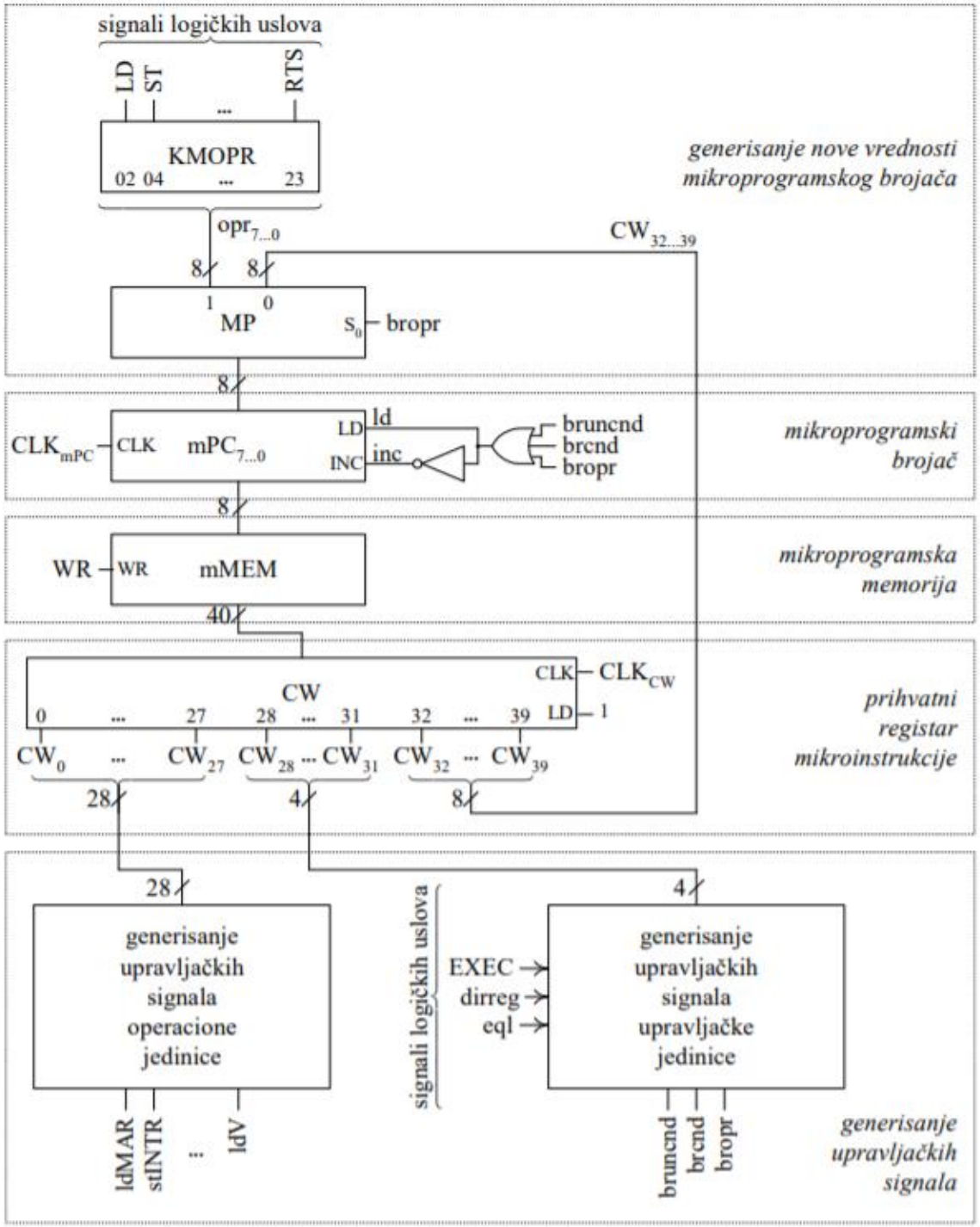

13
HALT
PSWSTART <= 0
INTR


13
HALT
clPSWSTART
INTR


INTR
INTR <= 1
EXEC <= 0
EXEC

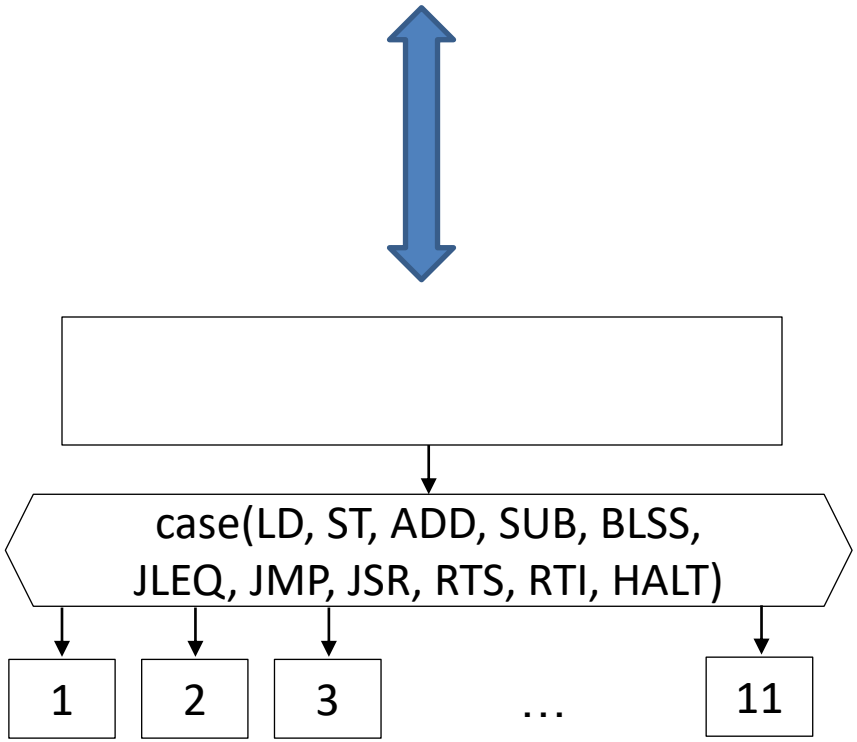

INTR
stINTR,
clEXEC
EXEC

Управљачка јединица



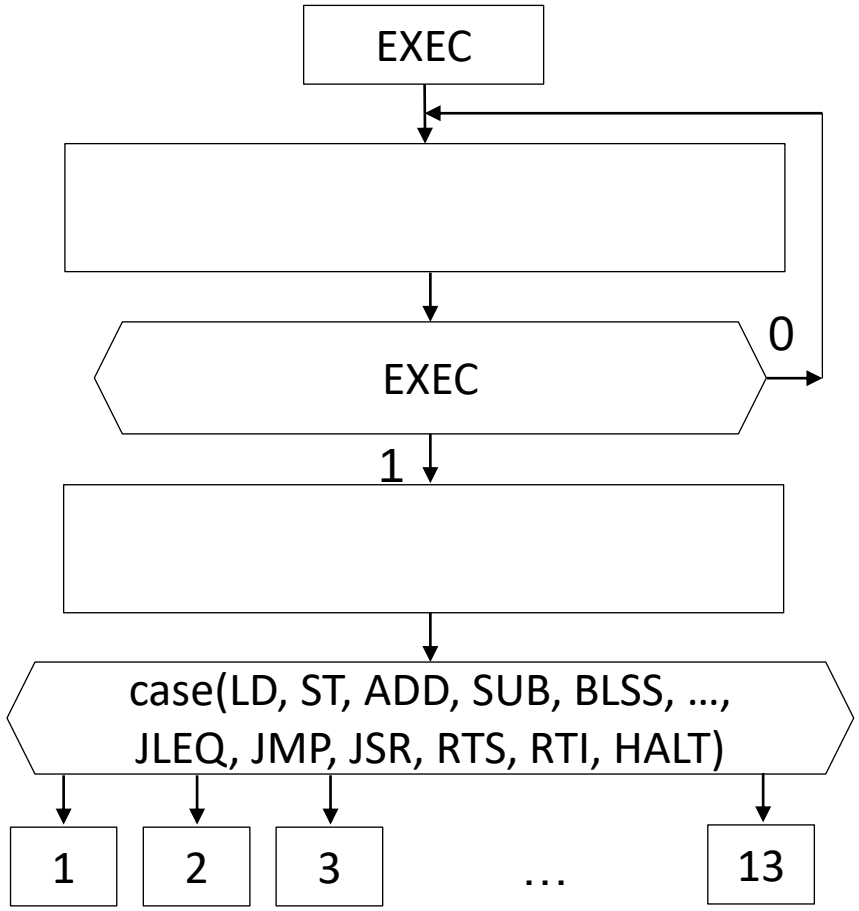
Секвенца управљачких сигнала

$step_{XX}$ br(case(LD, ST, …, RTI, HALT)then(LD, **step**), (ST, **step**)…,(RTI, **step**),(HALT, **step**))



step00 br(if notEXEC then step00)

step01 br(case(LD, ST,..., POPGPR, HALT) then(LD, **step02**), (ST, **step**),... ,(POPGPR, **step**),(HALT, **step**))



step00 br(if notEXEC then step00)

step01 br(case(LD, ST,..., POPGPR, HALT) then(LD, **step02**), (ST, **step04**),... ,(POPGPR, **step**),(HALT, **step**))

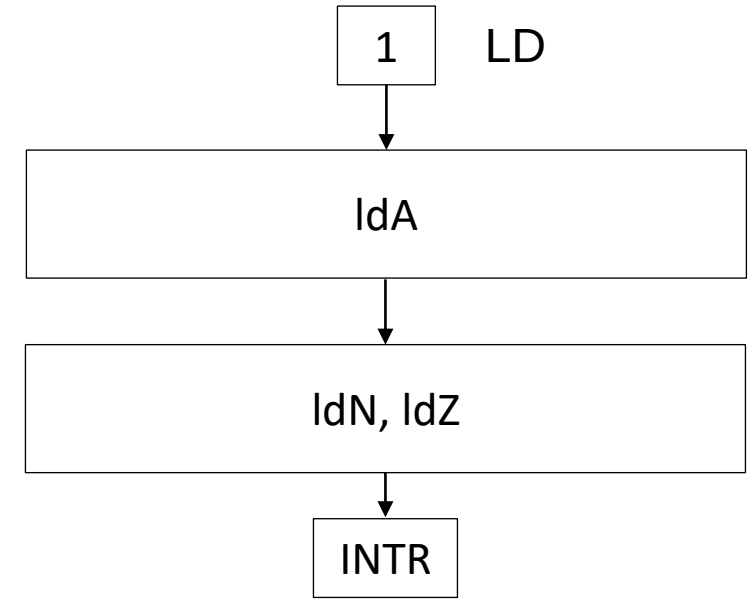
//----------LD----------

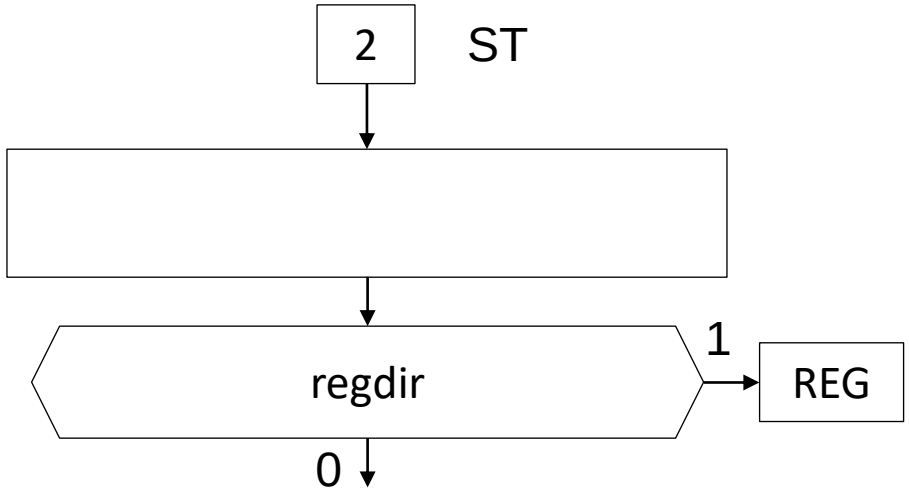
step02 ldA

step03 ldN, ldZ, br **step**

//----------ST----------

step04 br(if regdir then **step**)





step00 br(if notEXEC then step00)

step01 br(case(LD, ST,..., POPGPR, HALT) then(LD, **step02**), (ST, **step04**),... ,(POPGPR, **step**),(HALT, **step**))

//----------LD----------

step02 ldA

step03 ldN, ldZ, br **step**

//----------ST----------

step04 br(if regdir then **step08**)

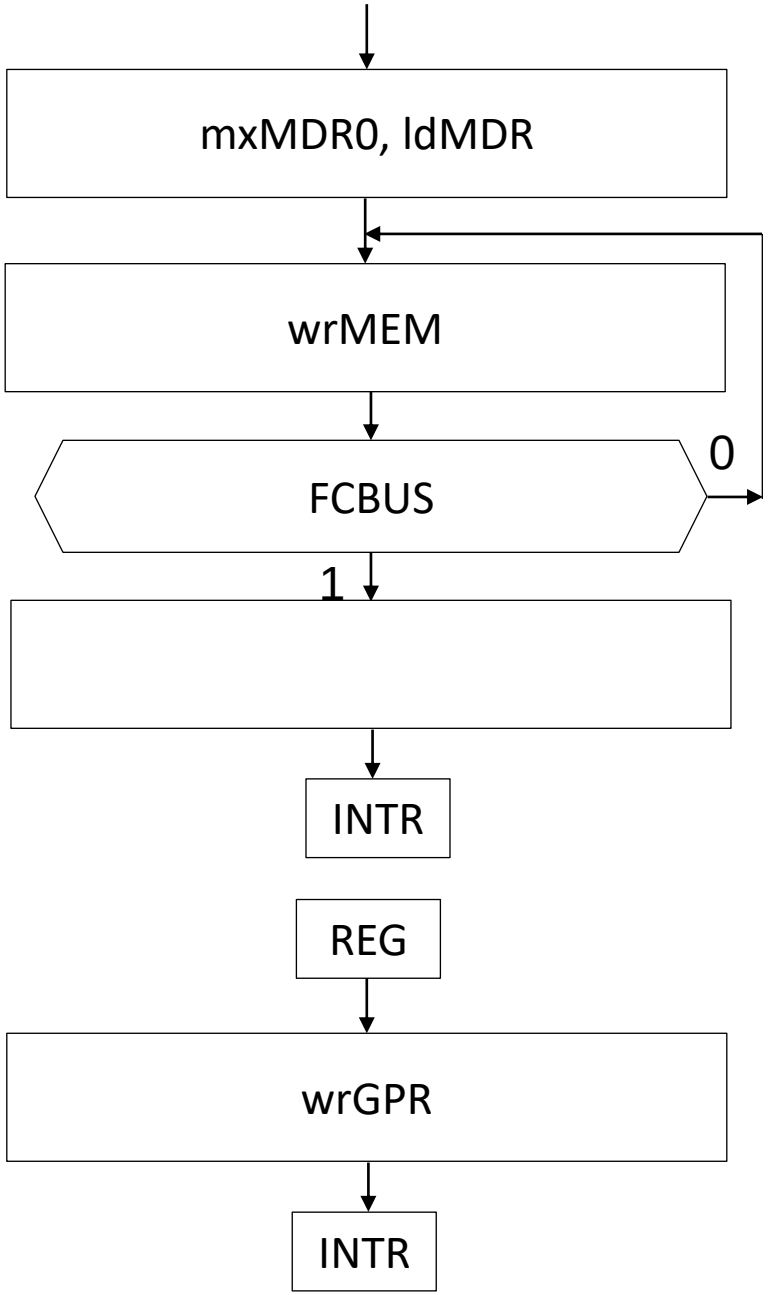
step05 mxMDR0, ldMDR

step06 wrMEM,

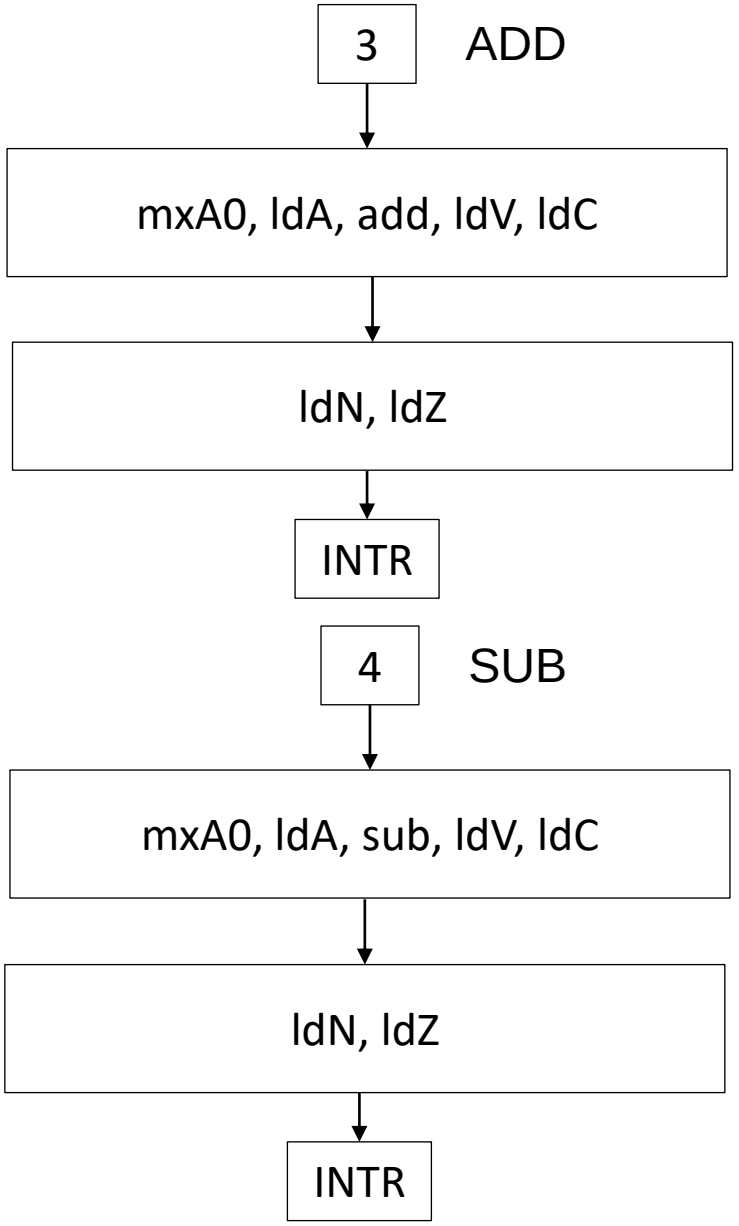
br(if notFCBUS then step06)

step07 br **step**

step08 wrGPR, br **step**



```
//----------------------ADD--------------------
step09 mxA0, ldA, add, ldV, ldC
step0A ldN, ldZ, br step
//----------------------SUB--------------------
step0B mxA0, ldA, sub, ldV, ldC
step0C ldN, ldZ, br step
```



//----------ADD----------

step09 mxA0, ldA, add, ldV, ldC

step0A ldN, ldZ, br **step**

//----------SUB----------

step0B mxA0, ldA, sub, ldV, ldC

step0C ldN, ldZ, br **step**

//----------BLSS,BGREU----------

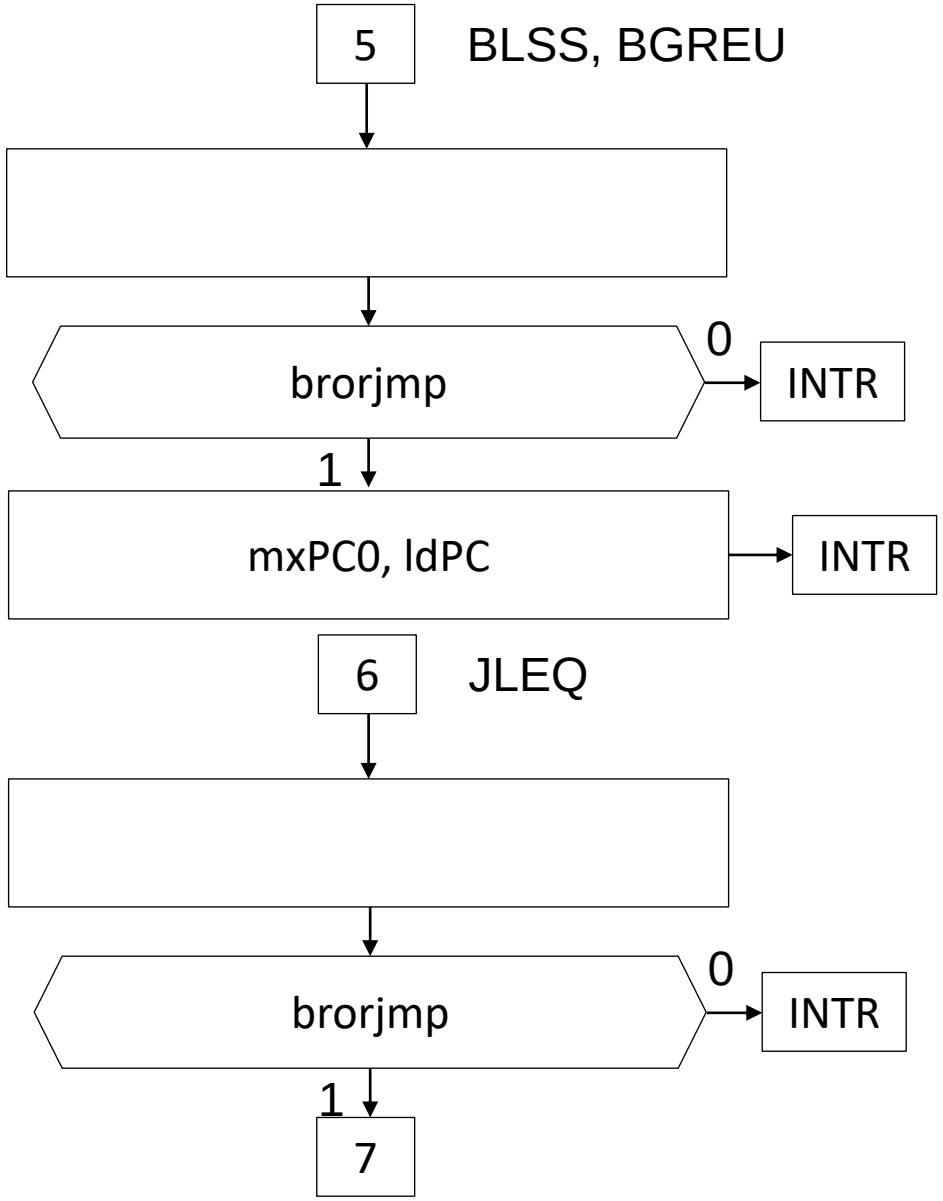
step0D br(if **not**brorjmp then **step**)

step0E mxPC0, ldPC, br **step**

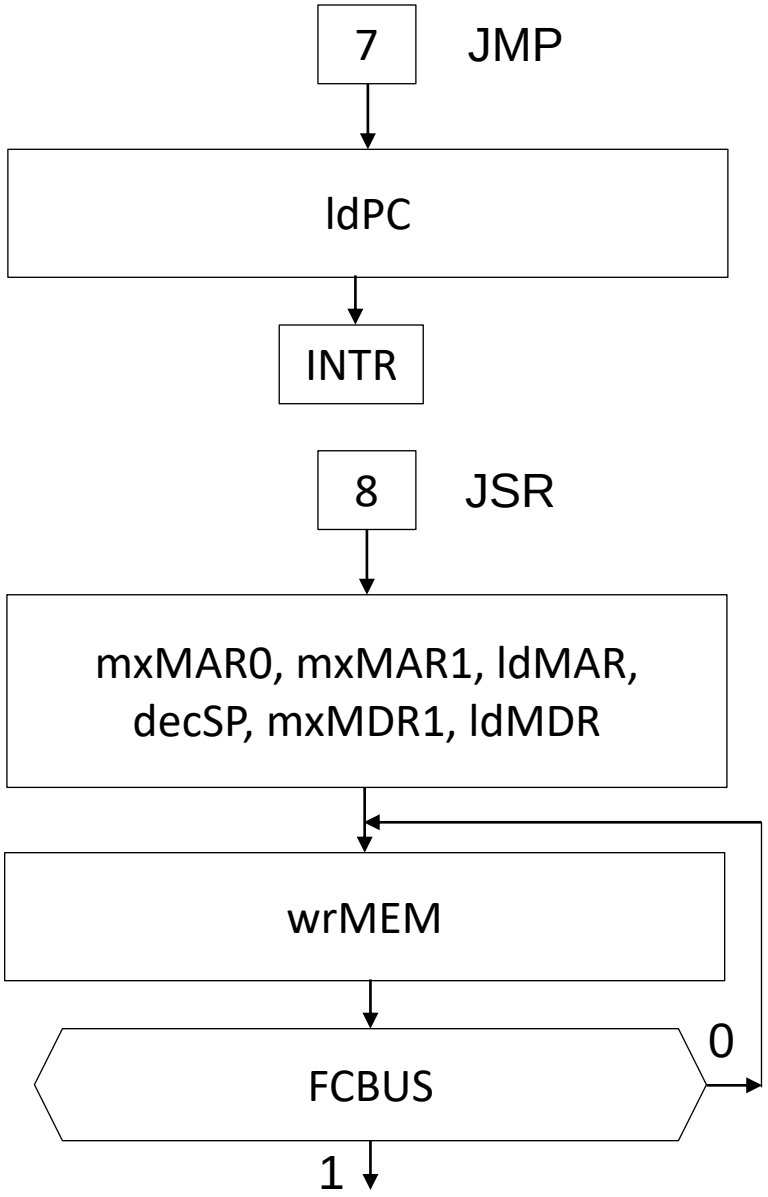
//----------JLEQ----------

step0F br(if **not**brorjmp then **step**)

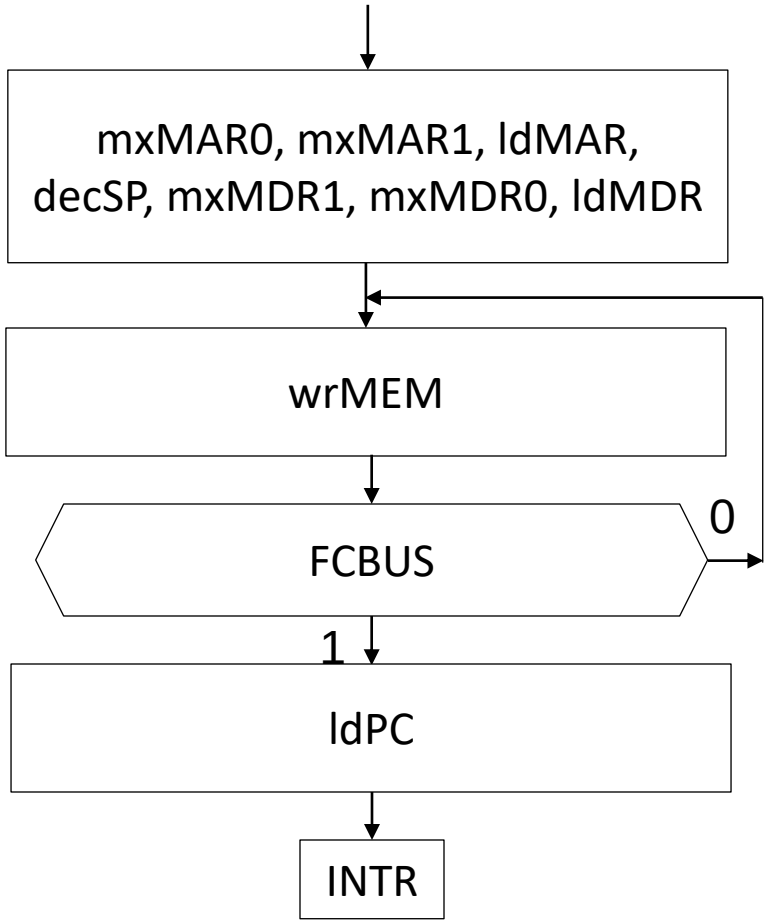
//----------JMP----------



//----------ADD----------
step09 mxA0, ldA, add, ldV, ldC
step0A ldN, ldZ, br **step**
//----------SUB----------
step0B mxA0, ldA, sub, ldV, ldC
step0C ldN, ldZ, br **step**
//----------BLSS,BGREU----------
step0D br(if **not**brorjmp then **step**)
step0E mxPC0, ldPC, br **step**
//----------JLEQ----------
step0F br(if **not**brorjmp then **step**)
//----------JMP----------
step10 ldPC, br **step**
//----------JSR----------
step11 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, ldMDR
step12 wrMEM,
br(if notFCBUS then step12)



```
//----------------------JSR--------------------
step11 mxMAR0, mxMAR1, ldMAR,
          decSP,mxMDR1, ldMDR
step12 wrMEM,
          br(if notFCBUS then step12)
step13 mxMAR0, mxMAR1, ldMAR,
       decSP, mxMDR1, mxMDR0, ldMDR
step14 wrMEM,
          br(if notFCBUS then step14)
step15 ldPC, br step
```



//----------JSR----------

step11 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, ldMDR

step12 wrMEM,
br(if notFCBUS then step12)

step13 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, mxMDR0, ldMDR

step14 wrMEM,
br(if notFCBUS then step14)

step15 ldPC, br **step**

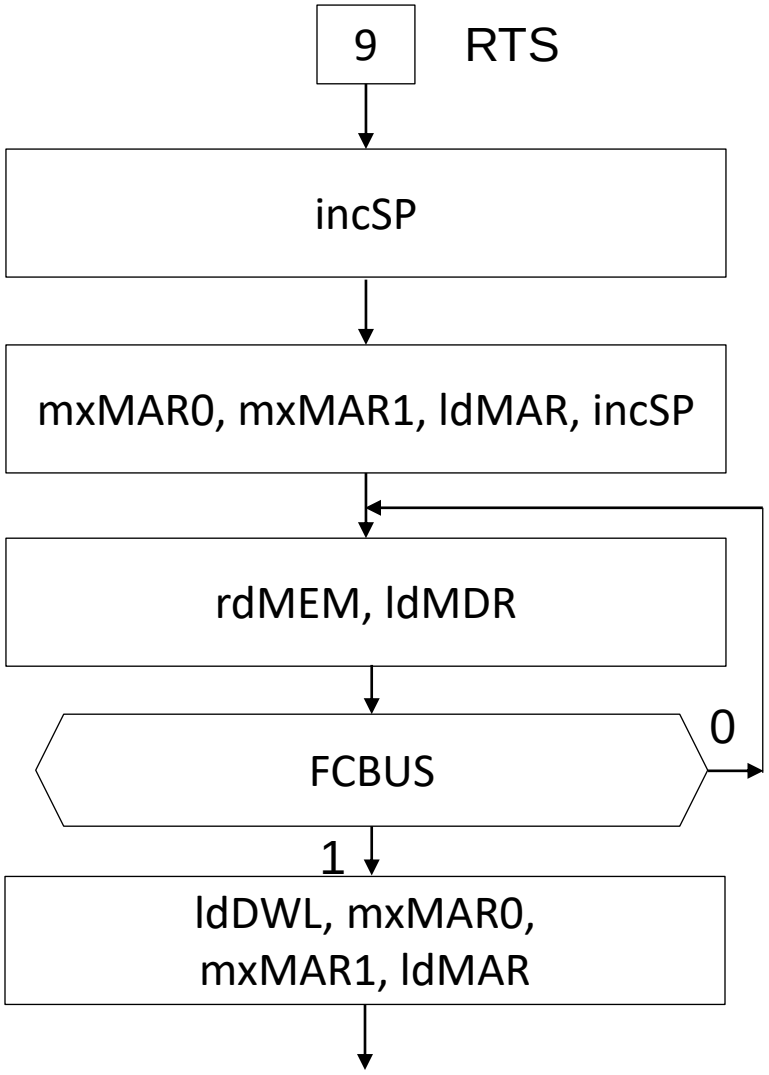
//----------RTS----------

step16 incSP

step17 mxMAR0, mxMAR1, ldMAR, incSP

step18 rdMEM, ldMDR,
br(if notFCBUS then step18)

step19 ldDWL, mxMAR0, mxMAR1, ldMAR



//----------RTS----------

step16 incSP

step17 mxMAR0, mxMAR1, ldMAR, incSP

step18 rdMEM, ldMDR,

br(if notFCBUS then step18)

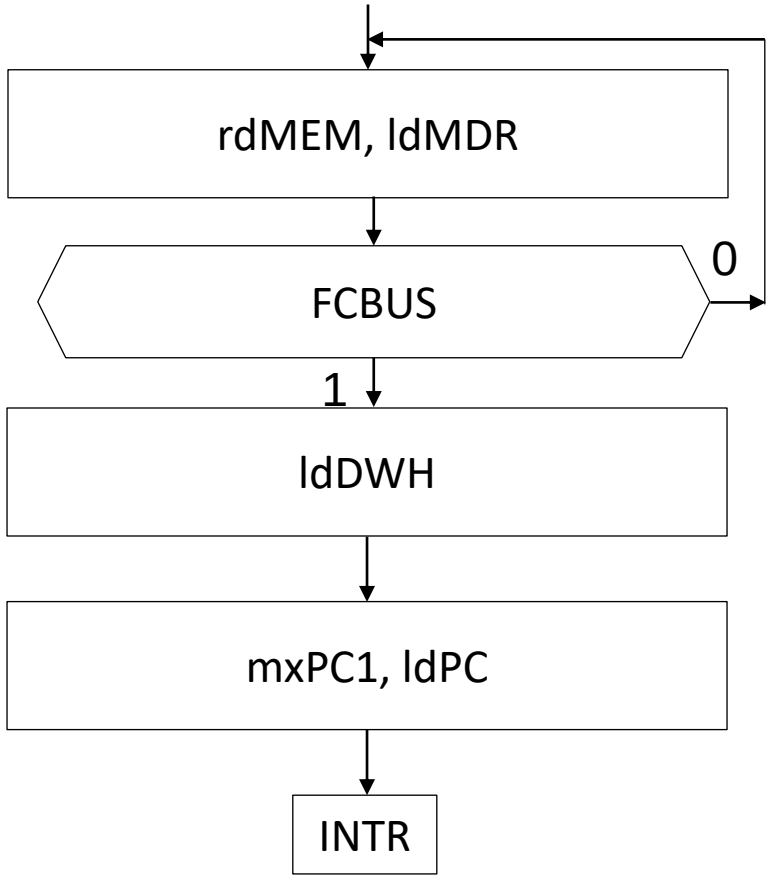
step19 ldDWL, mxMAR0, mxMAR1, ldMAR

step1A rdMEM, ldMDR,

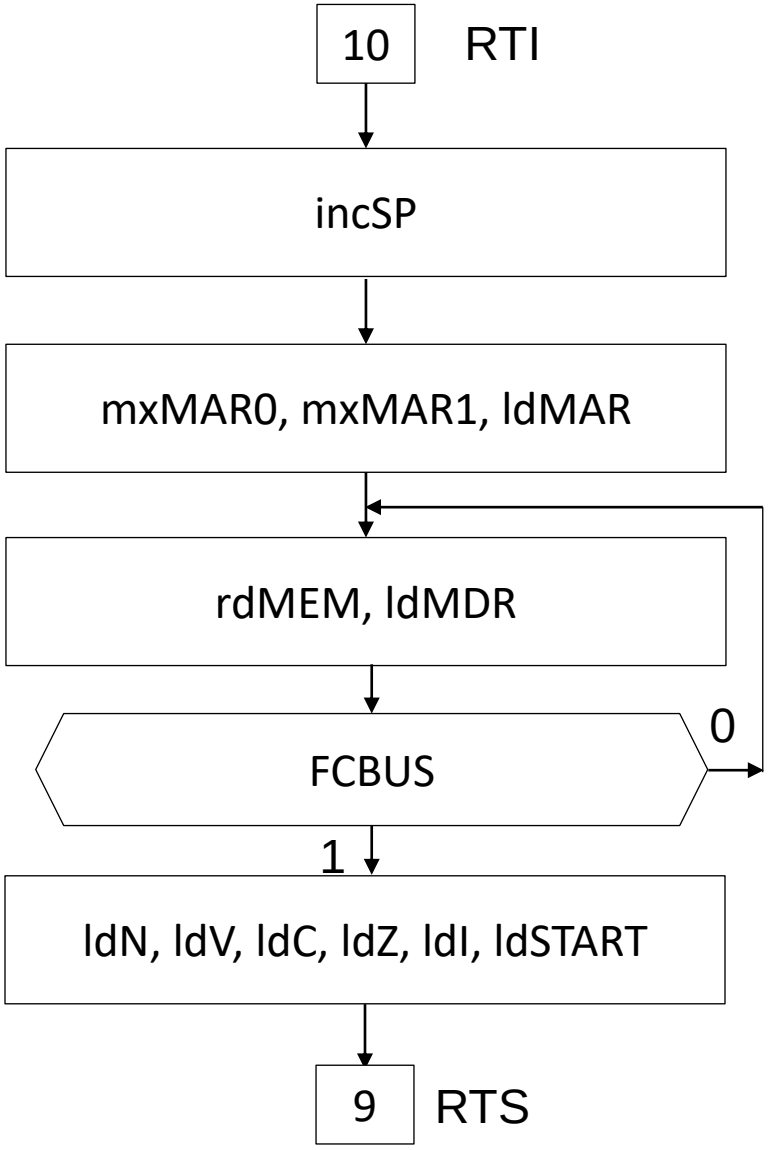
br(if notFCBUS then step1A)

step1B ldDWH

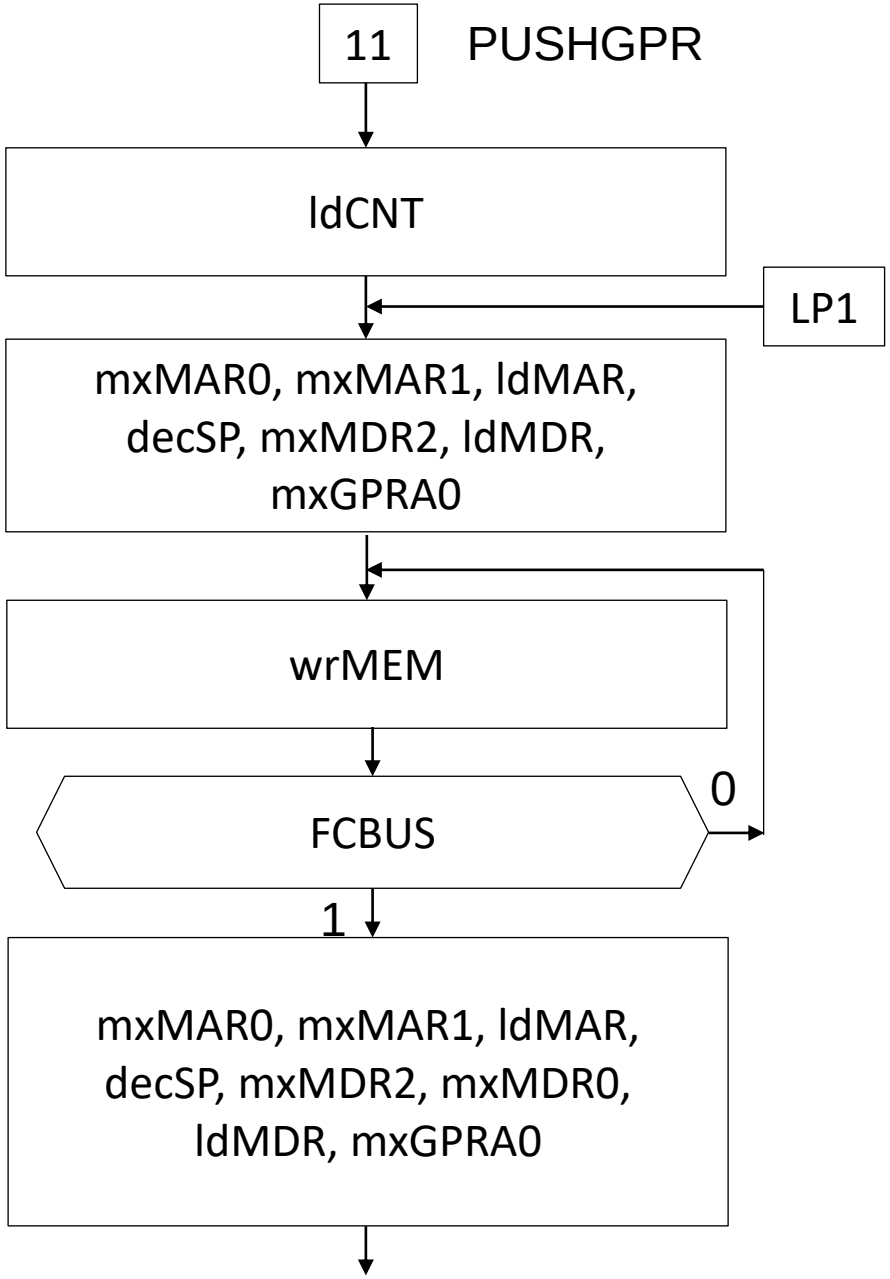
step1C mxPC1, ldPC, br **step**



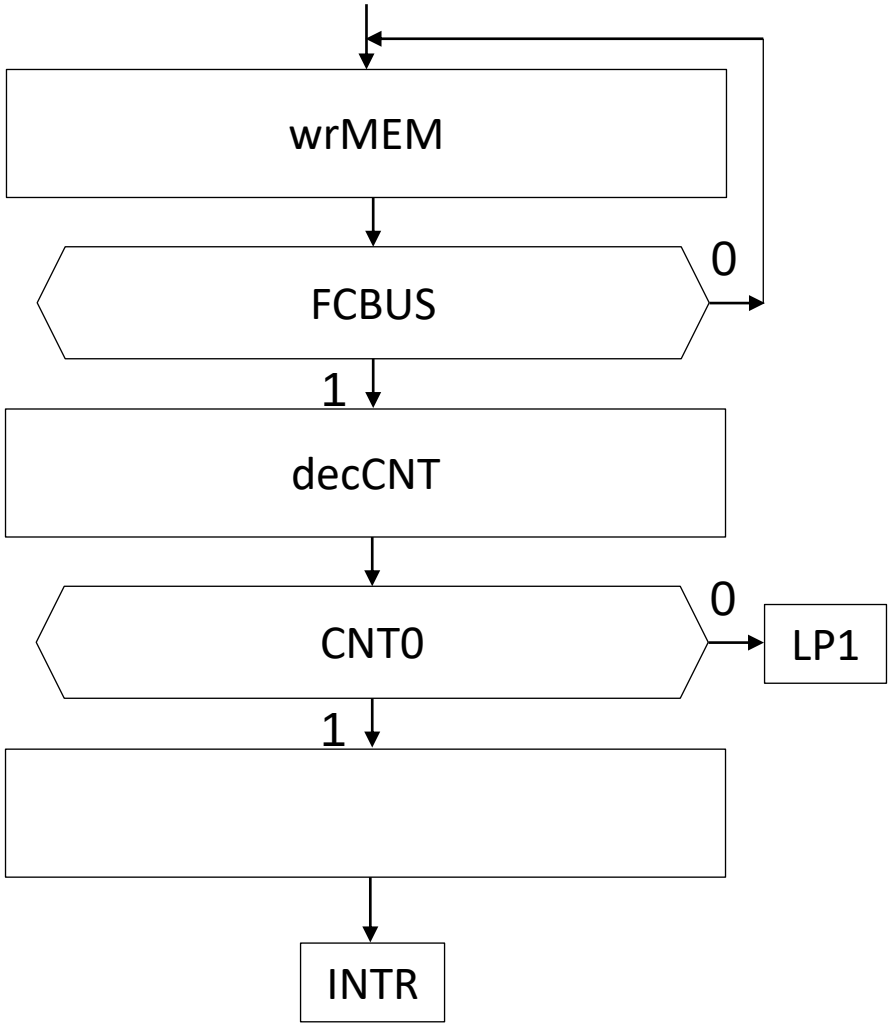
```
//----------------------RTS---------------------
step16 incSP
step17 mxMAR0, mxMAR1, ldMAR, incSP
step18 rdMEM, ldMDR,
       br(if notFCBUS then step18)
step19 ldDWL, mxMAR0, mxMAR,ldMAR
step1A rdMEM, ldMDR,
       br(if notFCBUS then step1A)
step1B ldDWH
step1C mxPC1, ldPC, br step
//----------------------RTI---------------------
step1D incSP
step1E mxMAR0, mxMAR1, ldMAR
step1F rdMEM, ldMDR,
       br(if notFCBUS then step1F)
step20 ldN, ldV, ldC, ldZ, ldI, ldSTART,
       br step16
```



```
//-------------------PUSHGPR------------------
step21 ldCNT
step22 mxMAR0, mxMAR1, ldMAR,
        decSP,  mxMDR2,  ldMDR,
          mxGPRA0
step23 wrMEM,
        br(if notFCBUS then step23)
step24 mxMAR0, mxMAR1, ldMAR,
          decSP,  mxMDR2,  mxMDR0,
          ldMDR, mxGPRA0
```



```
//-------------------PUSHGPR------------------
step21 ldCNT
step22 mxMAR0, mxMAR1, ldMAR,
       decSP,  mxMDR2,  ldMDR,
         mxGPRA0
step23 wrMEM,
       br(if notFCBUS then step23)
step24 mxMAR0, mxMAR1, ldMAR,
         decSP,  mxMDR2,  mxMDR0,
         ldMDR, mxGPRA0, decCNT
step25 wrMEM,
       br(if notFCBUS then step25)
step26 decCNT
       br(if notCNT0 then step22)
step27 br step
```



//--------------------POPGPR--------------------

step28 ldCNT, mxCNT0

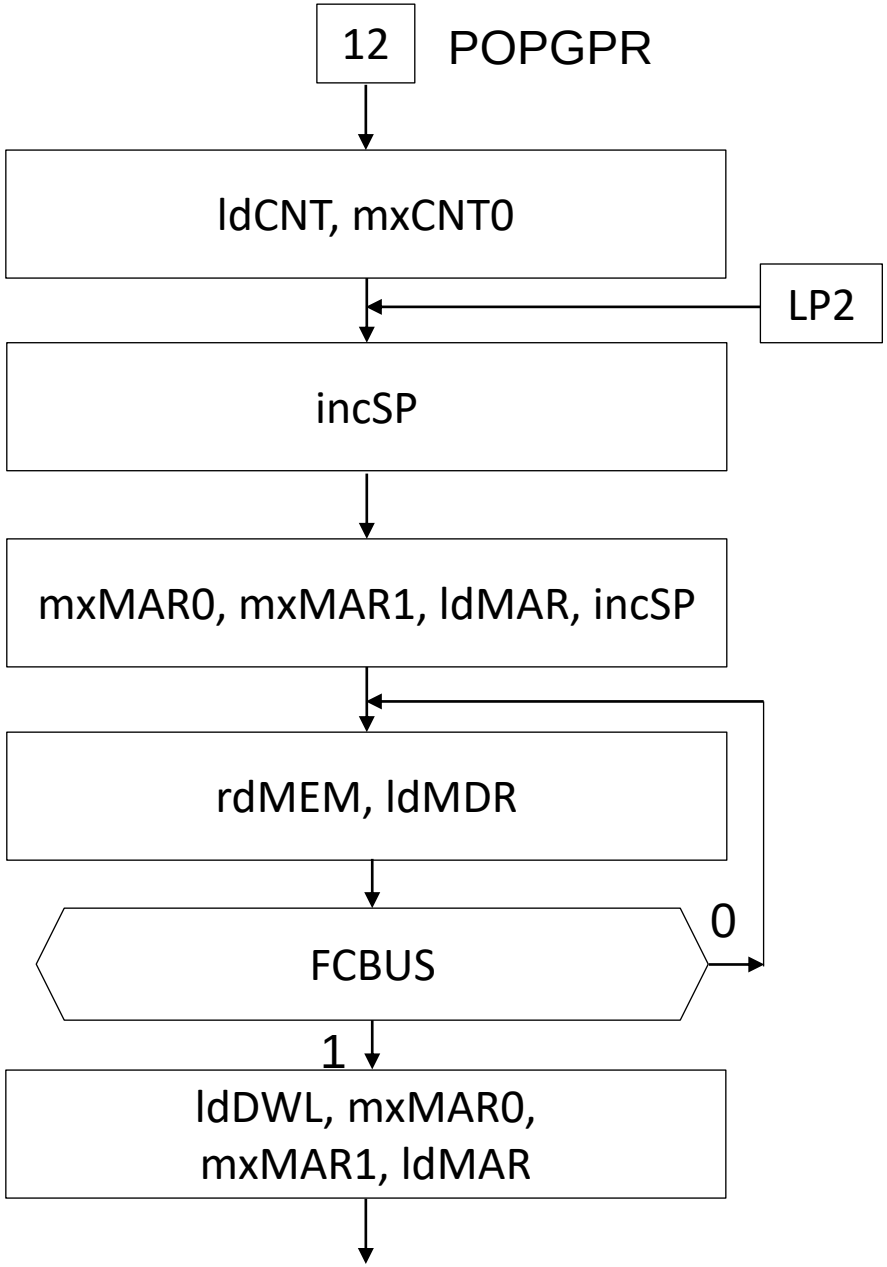
step29 incSP

step2A mxMAR0, mxMAR1, ldMAR, incSP

step2B rdMEM, ldMDR

br(if notFCBUS then step2B)

step2C ldDWL, mxMAR0, mxMAR1, ldMAR



//--------------------POPGPR--------------------

step28 ldCNT, mxCNT0

step29 incSP

step2A mxMAR0, mxMAR1, ldMAR, incSP

step2B rdMEM, ldMDR

br(if notFCBUS then step2B)

step2C ldDWL, mxMAR0, mxMAR1, ldMAR

step2D rdMEM, ldMDR

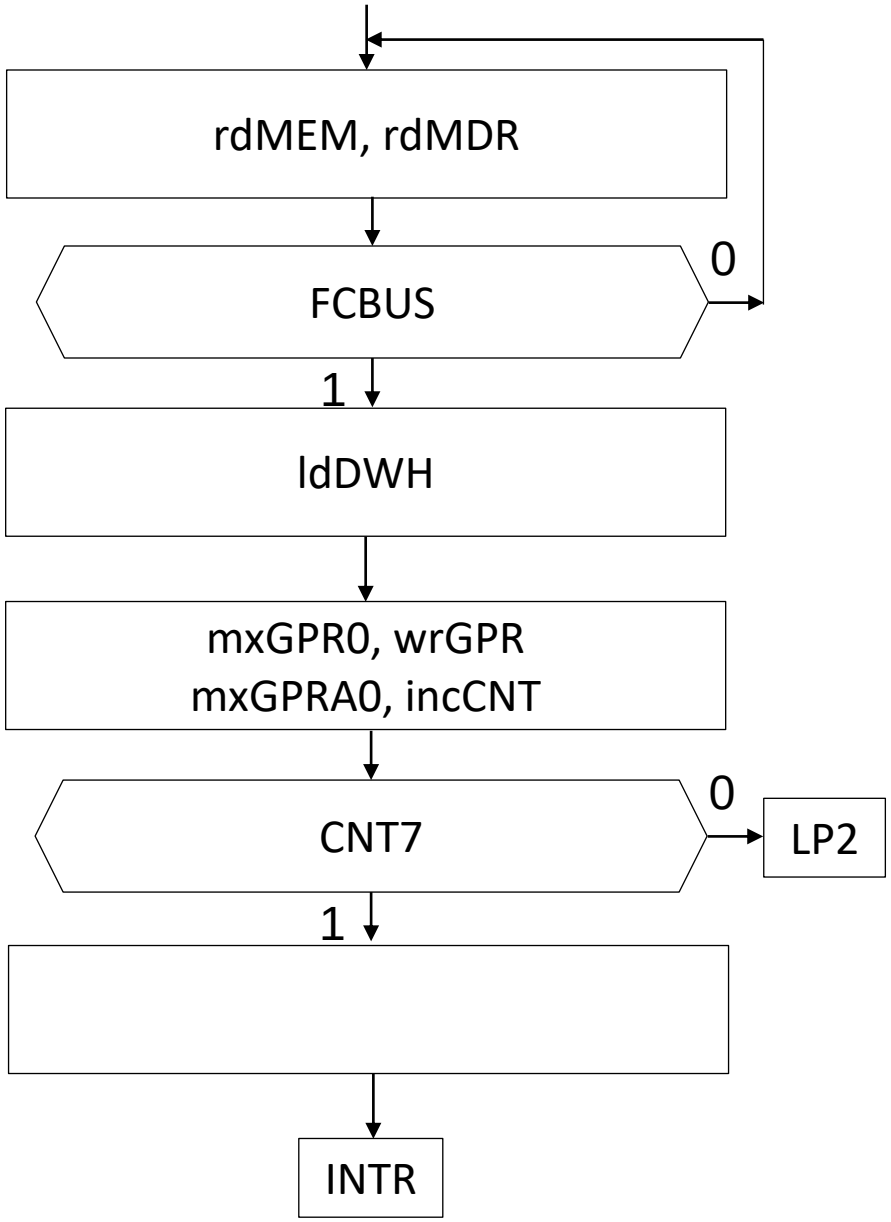
br(if notFCBUS then step2D)

step2E ldDWH

step2F mxGPR0, wrGPR, mxGPRA0, incCNT

br(if notCNT7 then step29)

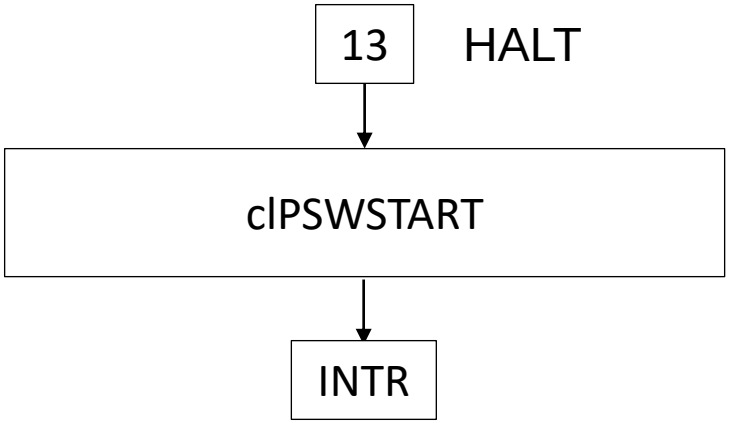
step30 br **step**

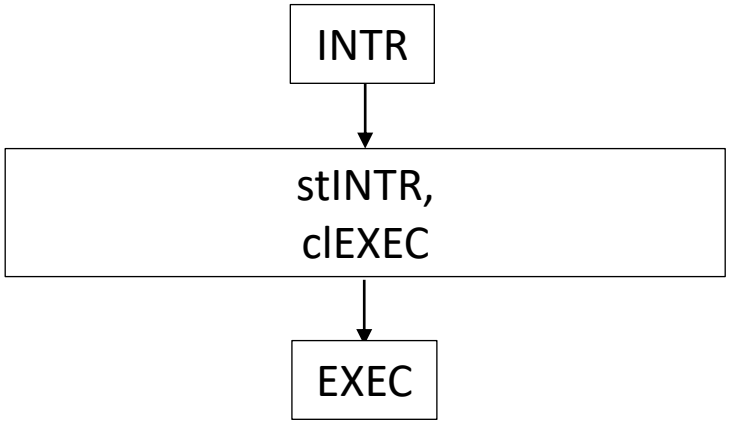


//-------------------HALT-------------------

step31 clPSWSTART

step32 stINTR, clEXEC, br step00





step00 br(if notEXEC then step00)

step01 br(case(LD, ST,..., POPGPR, HALT) then(LD, **step02**), (ST, **step04**),... ,(POPGPR, **step**),(HALT, **step**))

//----------LD----------

step02 ldA

step03 ldN, ldZ, br **step32**

//----------ST----------

step04 br(if regdir then **step08**)

step05 mxMDR0, ldMDR

step06 wrMEM,

br(if notFCBUS then step06)

step07 br **step32**

step08 wrGPR, br **step32**

//----------ADD----------

step09 mxA0, ldA, add, ldV, ldC

step0A ldN, ldZ, br **step32**

0	1	2	3
ldA	ldN	ldZ	mxMDR0

4	5	6	7
ldMDR	wrMEM	wrGPR	mxA0

8	9	10	11
add	ldV	ldC	

12	13	14	15

16	17	18	19

20	21	22	23

//----------SUB----------

step0B mxA0, ldA, sub, ldV, ldC

step0C ldN, ldZ, br **step32**

//----------BLSS,BGREU----------

step0D br(if **not**brorjmp then **step32**)

step0E mxPC0, ldPC, br **step32**

//----------JLEQ----------

step0F br(if **not**brorjmp then **step32**)

//----------JMP----------

step10 ldPC, br **step32**

//----------JSR----------

step11 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, ldMDR

step12 wrMEM,
br(if notFCBUS then step12)

0	1	2	3
ldA	ldN	ldZ	mxMDR0

4	5	6	7
ldMDR	wrMEM	wrGPR	mxA0

8	9	10	11
add	ldV	ldC	sub

12	13	14	15
mxPC0	ldPC	mxMAR0	mxMAR1

16	17	18	19
ldMAR	decSP	mxMDR1	

20	21	22	23

step13 mxMAR0, mxMAR1, ldMAR,
decSP, mxMDR1, mxMDR0, ldMDR
step14 wrMEM,
br(if notFCBUS then step14)
step15 ldPC, br **step32**
//----------RTS----------
step16 incSP
step17mxMAR0, mxMAR1, ldMAR, incSP
step18 rdMEM, ldMDR,
br(if notFCBUS then step18)
step19 ldDWL, mxMAR0, mxMAR1, ldMAR
step1A rdMEM, ldMDR,
br(if notFCBUS then step1A)
step1B ldDWH
step1C mxPC1, ldPC, br **step32**

0	1	2	3
ldA	ldN	ldZ	mxMDR0

4	5	6	7
ldMDR	wrMEM	wrGPR	mxA0

8	9	10	11
add	ldV	ldC	sub

12	13	14	15
mxPC0	ldPC	mxMAR0	mxMAR1

16	17	18	19
ldMAR	decSP	mxMDR1	incSP

20	21	22	23
rdMEM	ldDWL	ldDWH	mxPC1

```
//----------------------RTI---------------------
step1D incSP
step1E mxMAR0, mxMAR1, ldMAR
step1F rdMEM, ldMDR,
       br(if notFCBUS then step1F)
step20 ldN, ldV, ldC, ldZ, ldI, ldSTART,
       br step16
//-------------------PUSHGPR-------------------
step21 ldCNT
step22 mxMAR0, mxMAR1, ldMAR,
       decSP, mxMDR2, ldMDR,
         mxGPRA0
```

24	25	26	27
ldSTART	ldCNT	mxMDR2	mxGPRA0

28	29	30	31

32	33	34	35

36	37	38	39

40	41	42	43

44	45	46	47

step23 wrMEM,

br(if notFCBUS then step23)

step24 mxMAR0, mxMAR1, ldMAR,

decSP, mxMDR2, mxMDR0, ldMDR, mxGPRA0

step25 wrMEM,

br(if notFCBUS then step25)

step26 decCNT,

br(if notCNT0 then step22)

step27 br **step32**

//----------POPGPR----------

step28 ldCNT, mxCNT0

step29 incSP

step2A mxMAR0, mxMAR1, ldMAR, incSP

step2B rdMEM, ldMDR

br(if notFCBUS then step2B)

step2C ldDWL, mxMAR0, mxMAR1, ldMAR

24	25	26	27
ldSTART	ldCNT	mxMDR2	mxGPRA0

28	29	30	31
decCNT	mxCNT0		

32	33	34	35

36	37	38	39

40	41	42	43

44	45	46	47

step2D rdMEM, ldMDR
br(if notFCBUS then step2D)
step2E ldDWH
step2F mxGPR0, wrGPR, mxGPRA0,
incCNT
br(if notCNT7 then step29)
step30 br **step32**
//----------HALT----------
step31 clPSWSTART
step32 stINTR, clEXEC, br step00

24	25	26	27
ldSTART	ldCNT	mxMDR2	mxGPRA0

28	29	30	31
decCNT	mxCNT0	incCNT	mxGPR0

32	33	34	35
clPSWSTART	ldI	stINTR	clEXEC

36	37	38	39
/	/	/	/

40	41	42	43
/	/	/	/

44	45	46	47

Сигнал безусловног скока	CC
bruncnd	1

Сигнал условног скока	CC	Сигнал услова
brnotEXEX	2	$\overline{\text{EXEC}}$
brregdir	3	regdir
brbrorjmp	4	brorjmp
brnotCNT0	5	$\overline{\text{CNT0}}$
brnotCNT7	6	$\overline{\text{CNT7}}$
brnotFCBUS	7	$\overline{\text{FCBUS}}$

Сигнал вишеструког условног скока	CC
bropr	8

Услов	Корак
LD	2
ST	4
…	…
HALT	31

0	1	2	3
ldA	ldN	ldZ	mxMDR0

4	5	6	7
ldMDR	wrMEM	wrGPR	mxA0

8	9	10	…
add	ldV	ldC	…

40	41	42	43
/	/	/	/

44	45	46	47
cc			

48	49…	…54	55
ba			