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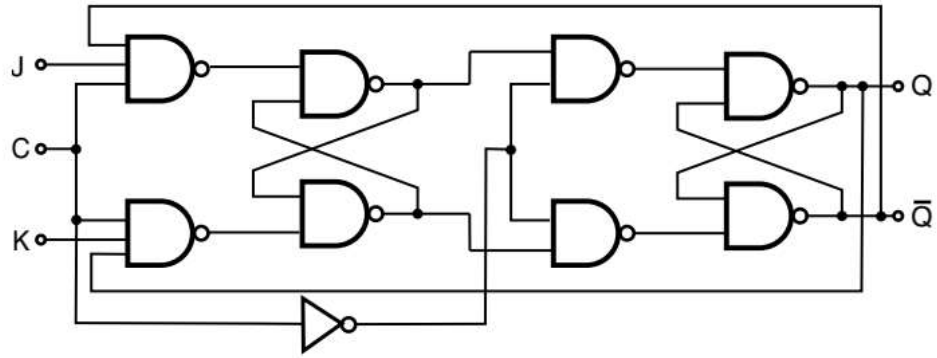
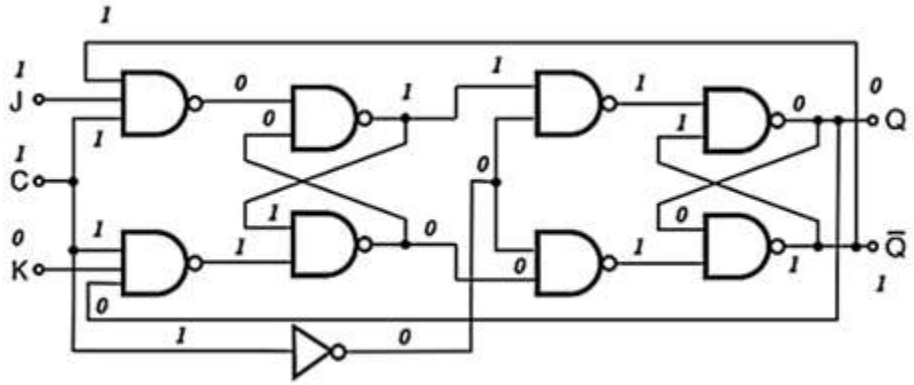
Homework - ICS 2020 Problem Sheet #9

Problem 9.1

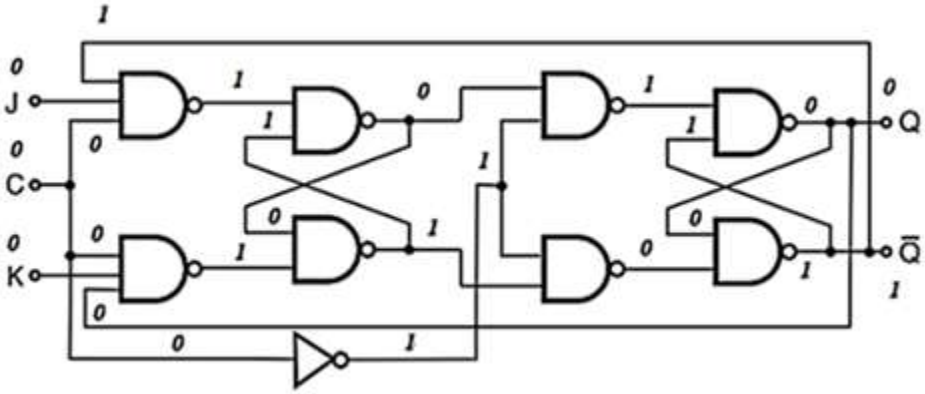
The sequential digital circuit shown below shows the design of a JK flip-flop based on two SR NAND latches. Assume the circuit's output is Q = 0 and that the inputs are J = 0 and K = 0, and that the clock input is C = 0. (You can make use of the fact that we already know how an SR NAND latch behaves.)



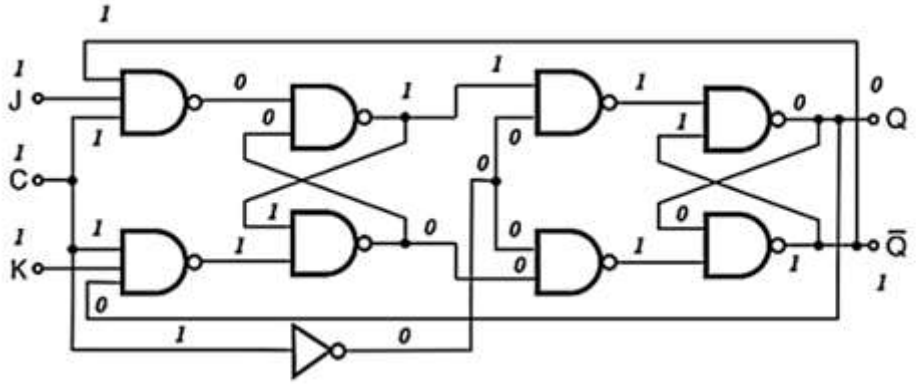
a) Suppose J transitions to 1 and C transitions to 1 soon after. Create a copy of the drawing and indicate for each line whether it carries a 0 or a 1.



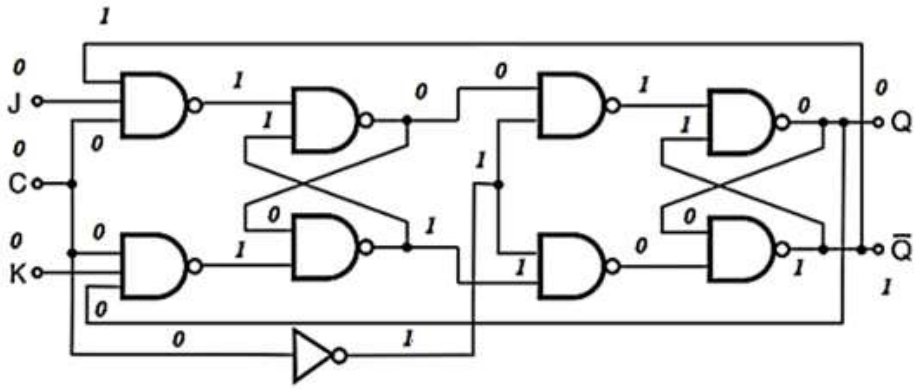
b) Some time later, C transitions back to 0 and soon after J transitions to 0 as well. Create another copy of the drawing and indicate for each line whether it carries a 0 or a 1.



c) Some time later, J and K both transition to 1 and C transitions to 1 soon after. Create another copy of the drawing and indicate for each line whether it carries a 0 or a 1.

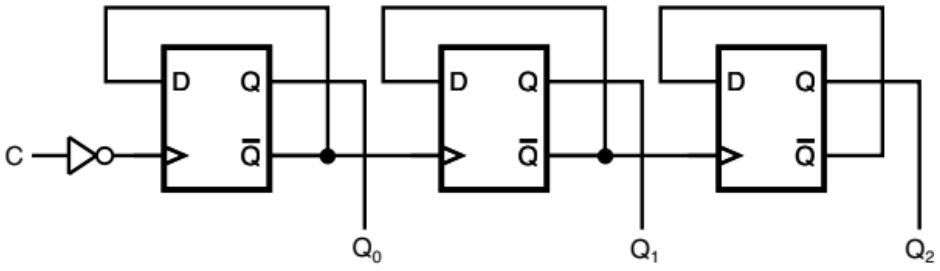


d) Finally, C transitions back to 0 and soon after J and K both transition to 0 as well. Create another copy of the drawing and indicate for each line whether it carries a 0 or a 1.

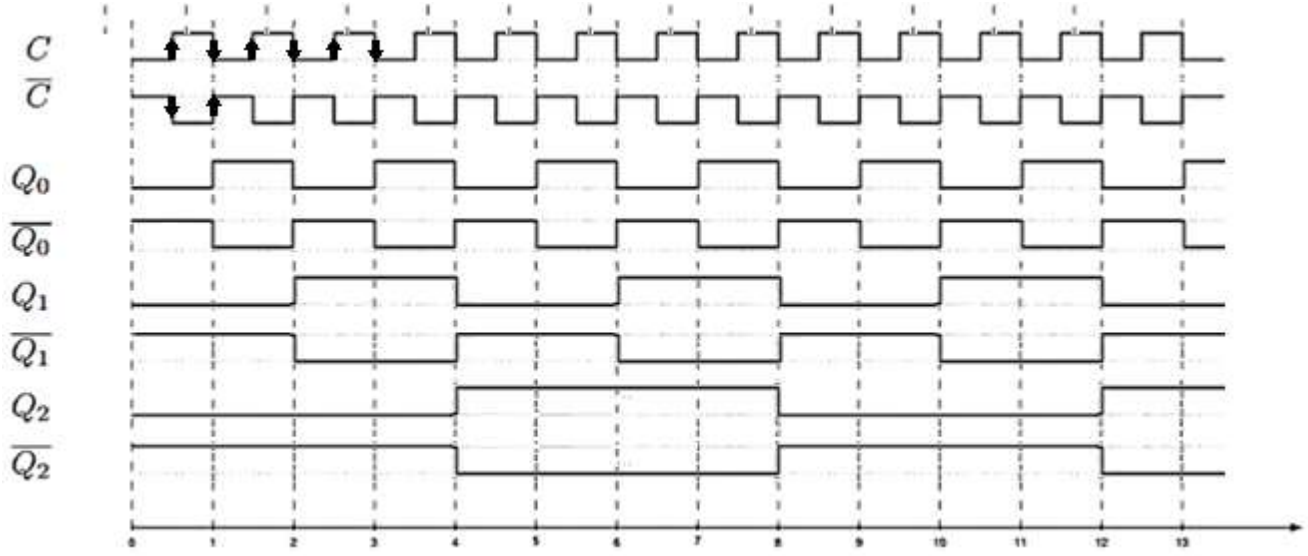


Problem 9.2

The following circuit shows a 3-bit ripple counter consisting of three positive edge triggered D flip-flops and a negation gate on the clock input C.



a) Complete the following timing diagram. Assume that gate delays are very short compared to the speed of the clock signal (i.e., you can ignore the impact of gate delays).



b) Can you make ripple counters arbitrary "long" or is there a limit on the number of D flip flops that can be chained? Explain.
   - No, you can not make the ripple-counters arbitrary long. There must be a limit, taking into consideration that the gate delays would add up and we would not get the result we needed as the gates will get mixed with one another.