# Jonah Foley | CV

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## About Me

I'm a graduate Electronic Engineer eager to leverage my digital design skill set in the realm of hardware engineering. I am deeply interested in digital systems and hardware computation, cultivated by pursing a degree path focused on RTL design, design-oriented internship experience and various personal projects spanning CPU design to high-level synthesis. I've worked with FPGAs for both HFT and DSP applications equipping me with a versatile skill set conducive to effective problem-solving. Outside of work, I am an avid film photographer and I'm currently learning Portuguese.

## Experience & Placements

### Jump Trading International Limited – Hardware Engineer Intern – Summer 2023 (10 Weeks)

During my 10 weeks at Jump I worked on designing network ingress components for FPGA devices. This involved developing an in-depth understanding of the existing codebase and designing new modules to strict timing constraints, requiring knowledge of the UDP network stack and consideration for the wider system architecture. In this process I gained experience deploying code into a production environment, developing an appreciation for continuous integration techniques, and learning new approaches to hardware simulation in Python. With supplemental training on financial fundamentals, this internship gave me an appreciation for the high intensity demands of HFT, from which I have developed a results-oriented mindset.

### Plextek Ltd. – FPGA Engineer Intern – Summer 2022 (12 weeks)

During my second internship at Plextek I was tasked with carrying out a proof-of-concept study into a component-based FPGA framework called OpenCPI and using it to implement a radio jammer. Using the framework, I successfully implemented a proof-of-concept design targeting the ADRV9361 platform, which utilised the FFT core I had built in my first internship here and demonstrated it performing jamming of PMR handsets (walkie-talkies). The FPGA operated in parallel to an embedded ARM processor which communicated to a PC over UDP to control configuration of the on-board DAC for synthesis of tones at the target frequency, utilising a custom JSON-based message parsing system atop a Qt GUI.

### Plextek Ltd. – FPGA Engineer Intern – Summer 2021 (10 Weeks)

This 10-week internship was my first step into commercial engineering. I was tasked with, and successfully achieved, the development of an FPGA-based (MAX-10) digital system which could compute the real-time Fourier transform of audio signals and transmit the result to a PC. UART was used as a serial interface to a PC where I built a multi-threaded spectrum analyser application in OpenGL that plotted the real-time power spectrum of the FFT. This project required understanding and selecting an appropriate FFT algorithm and then realising that using VHDL, drawing upon my digital design skillset.

## Education

| **University Degree \| MEng Electronic Engineering \| University of Southampton \| 2019-2023** | | |
|---|---|---|
| **Year** | **Grade achieved (Average)** | **Weighting** |
| Year 1 (19/20) | 78.5% | 0 |
| Year 2 (20/21) | 80.6% | 1 |
| Year 3 (21/22) | 81.7% | 2 |
| Year 4 (22/23) | 87.8% | 2 |
| | Final Weighted Average Grade: | 83.9% (1:1 Hons) |

| **A-Level \| Devonport High School for Boys, Plymouth \| 2017-2019** | |
|---|---|
| **Subject(s)** | **Grade achieved** |
| Mathematics, Physics, Chemistry | A* |

| **GCSE \| Plymouth College, Plymouth \| 2012-2017** | |
|---|---|
| **Subject(s)** | **Grade achieved** |
| English Language, English Literature, Mathematics, Physics, Biology, Chemistry, History, Business Studies | A* |
| Art | A |

| | |
|---|---|
| Spanish | B |

## Academic Awards

Zepler Prize (Oct. 2022) - Awarded for receiving the highest mark across combined BSc and MEng degrees in part III Electronic Engineering at the University of Southampton.

Chelton Prize (Oct. 2022) - Awarded for receiving the highest part III project (dissertation) mark in the area of 'radio, wireless or mobile communications' at the University of Southampton.

Harry Wright Chemistry Award (July 2019) - Awarded for receiving the highest A-Level chemistry grade at Devonport Highschool for Boys.

## Design Projects (University & Personal)

### Draw.IO to SystemVerilog FSM Generator (https://github.com/jonah766/FSM.io)

*Skills*: *C++20, SystemVerilog, Git, XML, Data Structures*

- Created a tool to convert Draw.IO state machine diagrams to SystemVerilog code in three steps: XML decoding, binary tree-like structure generation, and code generation.
- Leveraged modern features like `std::ranges` and `std::expected` for implementation.
- Aimed to simplify SystemVerilog FSM creation from graphical representations, inspired by high-level synthesis.

### Embedded Affine Transform CPU (https://github.com/jonah766/a_fine_CPU/)

*Skills: SystemVerilog, coco.tb, Processor Design, Fixed Point Computation*

- Created an embedded processor in SystemVerilog for affine transform computation, focusing on minimal design size for low-power applications.
- Designed a custom ALU for parallel computation and a custom instruction set to perform I/O operations.
- Conducted simulation using coco.tb, implementing functional models for core components like the ALU.
- Demonstrated the final design on an Altera DE1 SoC by running a pseudocode-described program.

### Adiabatic Low Power Logic (4th year group design project)

*Skills*: C*adence Virtuoso Schematic Capture, SKILL Scripting, Python, Analogue Circuits, Transistor Theory, Git*

- Collaborated with a semiconductor foundry on the design of adiabatic logic gates for a low-power cell library.
- Conducted schematic capture of adiabatic gates in Virtuoso and developed an automated simulation framework in Python to assess their energy consumption.
- Demonstrated the viability of adiabatic gates by implementing combinatorial and synchronous circuits using the custom cell library, developing scripts for automatic circuit generation.

### Index Modulated OFDM (3rd year individual project)

*Skills*: *MATLAB, Wireless Comms. Research, Report Writing, Monte-Carlo Simulation, Wireless Channel Modelling*

- Collaborated with Professor Sheng Chen on an investigation of 'index modulation' in OFDM wireless transmission.
- Conducted theoretical analysis covering wireless channel modelling, OFDM, multi-user MIMO systems, and various IM-OFDM families.
- Developed MATLAB simulation models for each analysis, assessing performance compared to other schemes and extending the study to 'dual-mode' IM-OFDM for increased throughput, earning the Chelton Prize.

## Relevant Technical Proficiencies

- SystemVerilog/VDHL (*Applied to: Networking, DSP, Numerical Processing, Processor Design, SystemC*)
- Python (*Automation, Hardware Simulation (coco.tb), Component Modelling, Numerical Methods, GUI design*)
- C/C++ (*STL*, *Hardware Modelling, OpenCV, OpenGL, GUI Design, CMake, Conan, Embedded (C)*)
- Quartus/Vivado/Vitis (*Static Timing Analysis, Synthesis, TCL scripting, Xilinx/Altera FPGAs*)
- ModelSim/Xcelium (*Hardware Verification, Coverage Analysis*)
- Git/Github/Gitlab (*Multi-user projects, Continuous Integration (Jenkins*), *Dependency Management*)
- Linux (*Proficiency working with: RHEL 8, CentOS, Ubuntu, in virtual environments*)
- RISC-V, MIPS, PicoMIPS architectures
- UDP Communication Protocol (*Network Header Processing, VLAN tagging, Packet Generation*)