Jonas Haglund

Education

2016-10 - 2023-06 KTH/EECS, Lindstedtsvägen 5, 114 28 Stockholm, Sweden.

PhD in computer science with focus on formal verification of memory isolation of DMA.

2012-08 - 2016-10 KTH/CSC, Lindstedtsvägen 5, 114 28 Stockholm, Sweden.

Master in computer engineering with focus on general problem solving, formal methods, systems software and hardware.

2010-08 - 2012-06 KTH/CSC, Lindstedtsvägen 5, 114 28 Stockholm, Sweden.

Continuation of bachelor in computer engineering with focus on computer science.

2007-08 - 2010-08 KTH/STH, Hälsovägen 11C, 141 57 Huddinge, Sweden.

Start of bachelor in computer engineering with focus on computer networks.

Professional Experience

2023-08 - present SSRG, ECE, Virginia Tech, 1991 Kraft Dr. SW, Suite 2001, Blacksburg, Virginia 24061, United States.

Work on formal verification of that device drivers configure I/O devices to respect memory isolation requirements, and synthesis of such drivers.

Teaching Experience

2023-08 - 2024-05 SSRG, ECE, Virginia Tech, 1991 Kraft Dr. SW, Suite 2001, Blacksburg, Virginia 24061, United States.

I supervised Aditya Gawali and Robbie Platt master's theses projects, about direct memory access (DMA) device driver modeling and verification:

- Modeling and Synthesis of Linux DMA Device Drivers using HOL4. Aditya Gawali. May 7, 2024.
- Verification of DMAC Device Driver Operations in HOL4. Robert D. Platt. May 7, 2024.

2016-10 - 2020-12 KTH/EECS, Lindstedtsvägen 5, 114 28 Stockholm, Sweden.

I was a teaching assistant during my PhD in the following courses (corresponding to one year of full time work): Computer Security; Logic in Computer Science; Formal Methods; and Algorithms, Data Structures and Complexity. I mainly: did tutorials; helped students with labs; and graded labs, assignments and exams. I have also developed lab assignments for the formal methods course involving C program verification and model checking.

Other Experience

2016-10 - 2023-06 KTH/EECS, Lindstedtsvägen 5, 114 28 Stockholm, Sweden.

I was a member of the PhD computer science program council. I helped with organizing retreats for the PhD students, participating in a PhD computer science program evaluation, documenting a description of the PhD computer science program, attending council meetings, and announcing PhD courses and PhD student requests for PhD courses. I have also reviwed three papers in the security and formal methods field.

Other Industry and Research Experience

2021-01 - 2021-03 Arm Ltd, 110 Fulbourn Road, Cambridge, CB1 9NJ, United Kingdom.

A seven week internship where I worked on modeling and formalizing security properties of an ARM architecture. This was during the COVID pandemic and I worked from home in Sweden.

2016-03 - 2016-09 RISE Research Institutes of Sweden, Isafjordsgatan 22, 164 40 Kista, Sweden.

Worked on a research project (PROSPER) where I programmed parts of a hypervisor and extended a port of Linux to run on top of the hypervisor.

Publications

Haglund, J., & Guanciale, R. (2022). Formally Verified Isolation of DMA. In A. Griggio & N. Rungta (Eds.), Proceedings of the 22nd Conference on Formal Methods in Computer-Aided Design – FMCAD 2022 (pp. 118–128). TU Wien Academic Press. DOI: https://doi.org/10.34727/2022/isbn.978-3-85448-053-2_18.

A general model of DMA controllers which is formalized and verified with respect to memory isolation.

Haglund, J., Guanciale, R. Trustworthy isolation of DMA devices. J BANK FINANC TECHNOL 4, 75–94 (2020). DOI: https://doi.org/10.1007/s42786-020-00018-x.

A journal article that is an extension of the following article. Describes a monitor that checks that a NIC is isolated, with the monitor being a part of a hypervisor with Linux on top.

Haglund, J., Guanciale, R. (2019). Trustworthy Isolation of DMA Enabled Devices. In: Garg, D., Kumar, N., Shyamasundar, R. (eds) Information Systems Security. ICISS 2019. DOI: https://doi.org/10.1007/978-3-030-36945-3_3.

A case study of formally verifying the conditions under which a network interface controller (NIC) can access only certain memory regions.

Professional Presentations

2022-10 Paper at FMCAD 2022.

2022-06 Research Group Retreat. Described a formal model of a USB DMA controller.

2022-06 Seminar at KTH/EECS. Described a formal analaysis tool of DMA controllers, including a USB DMA controller.

2021-11 Seminar at KTH/EECS. Presentation of 80% of my PhD studies.

2021-02 Seminar at ARM. Described a formal analysis of memory isolation of a NIC DMA controller, with a runtime monitor configuring the NIC to respect isolation.

2020-06 Seminar at KTH/EECS. Presentation of 50% of my PhD studies.

2019-12 Paper at Internal Conference in Information Systems Security (ICISS) 2019.

2019-11 Seminar at KTH/EECS. Presentation of 30% of my PhD studies.

2019-06 Poster presentation at Euro S&P. Described formal verification of memory isolation of a NIC DMA controller.

2019-05 Research Group Retreat. Described a formal model and a memory isolation proof of a NIC DMA controller.

Expertise

Formal Methods	Modeling hardware, formalization of properties, and formal proofs (interactive theorem proving; I have some experience with model checking, NuSMV, and deductive verification, Frama-C).
Hardware/Software Interface	Low-level programming in C and assembly, and configuration of peripherals.
Systems Software	Hypervisors and operating systems (mainly memory management and peripherals).