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# Power Electronics for Distributed Energy Systems

Practical Part 1  
Boost Converter for PV Applications

by

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# 1 Motivation

The general goal of the Practical Part of the "Power Electronics for Distributed Energy Systems" course is to design a solar inverter. This first part of the task is focused on designing a DC-DC converter to extract the maximum power from the solar panel by controlling the input voltage of the boost converter via the duty cycle.

The design steps are taken from the given task [1].

## 2 PV Characterization

The first part of the task deals with the characterization of the source of the dc-dc converter. Two solar string in parallel feed the circuit. Each string consists of 22 panels.

Since the PV panels are connected in series to form a string, voltage-related parameters scale with the number of modules, while current-related parameters remain unchanged. Therefore, the open-circuit voltage, series resistance, shunt resistance, and voltage temperature coefficient are multiplied by the number of modules per string.

The values are extracted from a datasheet of the "KC200GT" module by the manufacturer "Kyocera" [2].

This leads to the following values for a PV String:

Parameter	Single PV Module	PV String (22 Modules)
Open-circuit voltage $V_{OC}$ [V]	32.9	723.8
Equivalent series resistance $R_s$ [ $\Omega$ ]	0.221	4.862
Equivalent shunt resistance $R_p$ [ $\Omega$ ]	415.405	9138.91
Voltage temperature coefficient $K_V$ [V/K]	-0.123	-2.706

Table 1: PV module parameters dependent on the number of panels in a series string

To characterize the PV-System the Irradiance is set to 0.25 and 1.0 of the maximal value, which is  $1000 \frac{W}{m^2}$ . Two cycles are recorded in total, which adds up to a simulation length of one second. In the following the current and voltage dependency are discussed.

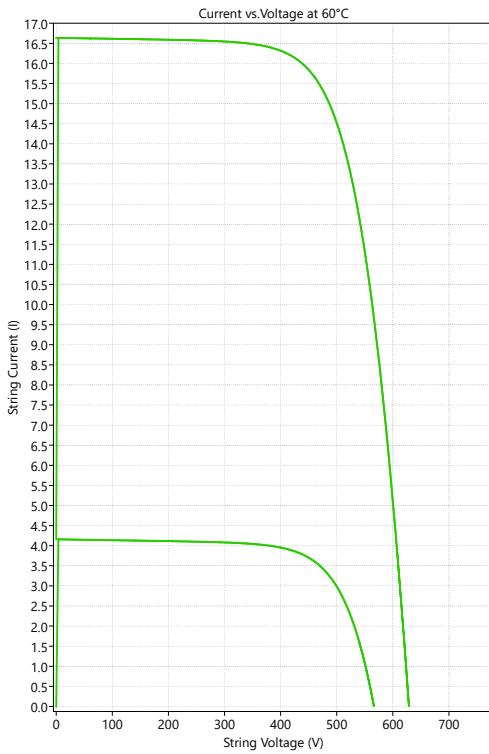


Figure 1: Current over voltage at 60 °C

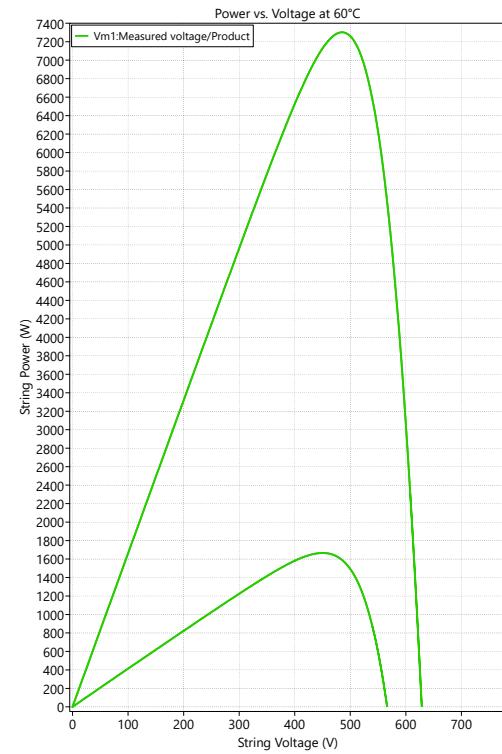


Figure 2: Power over voltage at 60 °C

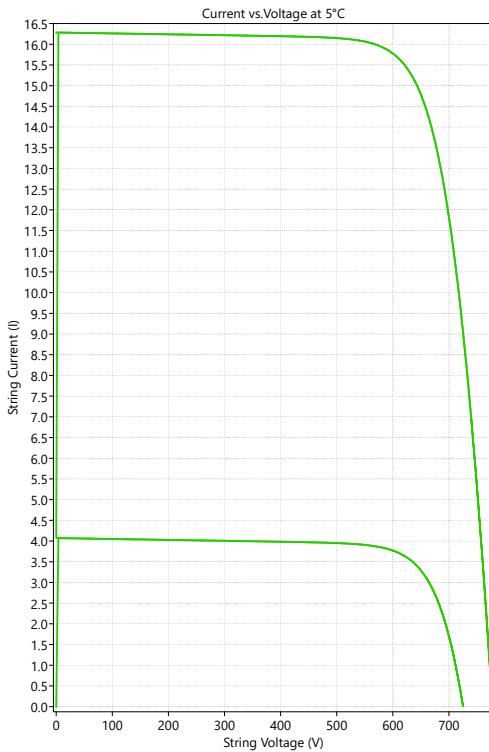


Figure 3: Current over voltage at 5 °C

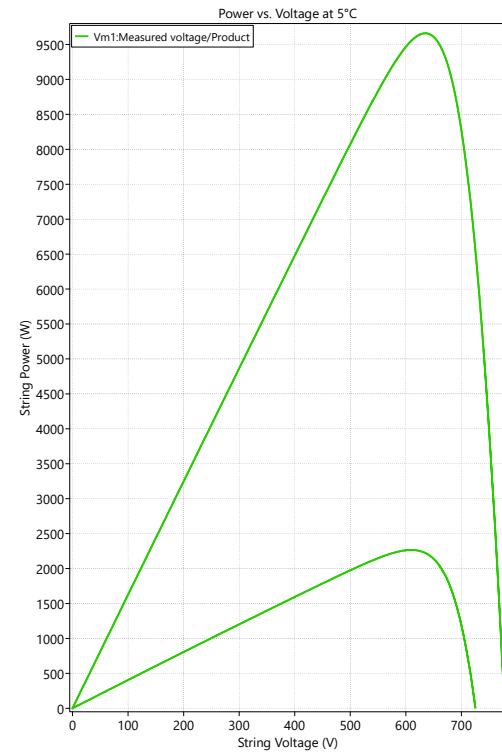


Figure 4: Power over voltage at 5 °C

Figure 1 to Figure 4 show the characteristic curves of the PV system. It becomes evident that the maximum power output is highly dependent on temperature. This variation in power is mainly caused by changes in the output voltage, while the current is only weakly affected.

With increasing temperature, the saturation current of the internal diode increases, which leads to a reduction of the terminal voltage and therefore a lower maximum power output.

Furthermore, a reduction in irradiance leads to a proportional decrease in the output power. The maximum power is approximately linear with irradiance, while the open-circuit voltage shows only a weak dependence on irradiance. Lower irradiance generates less photocurrent, which is linked to the open-circuit voltage.

Temperature	$P_{MPP}$ [W]	$V_{MPP}$ [V]	$V_{OC}$ [V]
5 °C	9655	635	770
25 °C	8800	580	723
60 °C	7300	485	628

Table 2: Maximum power and voltage levels of the PV string at different cell temperatures at full irradiance

Temperature	$P_{MPP}$ [W]	$V_{MPP}$ [V]	$V_{OC}$ [V]
5 °C	2250	610	725
25 °C	2050	550	667
60 °C	1660	450	566

Table 3: Maximum power and voltage levels of the PV string at different cell temperatures at 25% irradiance

Lastly, the power output at a fixed voltage of 580 V, which is the Maximum Power Point (MPP) voltage for an irradiance of 1, was simulated for an irradiance of 0.2. The power at this point is 1530 W. The maximum possible power at an irradiance of 0.2 would be 1600 W, which can be obtained from Figure 5, so we lost 4.375% by not shifting the voltage. This behavior can be explained with Table 2 and Table 3, as the voltage of the MPP shifts with varying irradiance. Therefore, at the constant operating voltages the MPP is missed with changing levels of irradiance.

This work is the foundation of the DC-DC converter design and describes the intended operating points to harvest the maximum amount of available solar power. A control strategy needs to be formulated in the subsequent design to enable varying voltage levels.

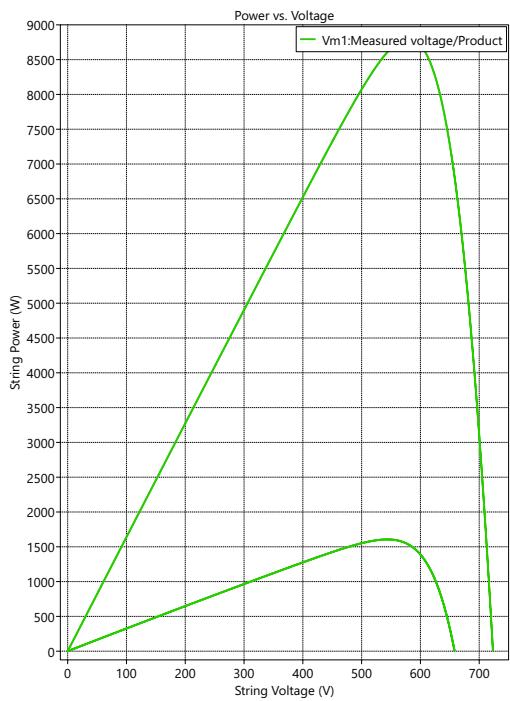


Figure 5: Power over voltage at 25°C with irradiances of 1 and 0.2

## 3 Boost Converter Design

### 3.1 DC-link voltage

The minimum DC-bus voltage is determined by the inverter connected to the DC link. A three-phase inverter rated at 400 V with a modulation index of  $m = 1$  requires a minimum DC-bus voltage of 654 V [3]. Including a safety margin of 10%, the minimum required DC-bus voltage increases to 719 V. Consequently, a nominal DC-bus voltage of 750 V is selected.

At the same time, unnecessarily increasing the DC-link voltage results in higher switching losses in the power semiconductors. Therefore, the DC-link voltage must represent a compromise between efficiency and robust maximum power point (MPP) operation. In this design, a DC-link voltage of 750 V is chosen as a reasonable trade-off. It also aligns with our safety margin of 25% of the maximum voltage of the switches, which would set the maximum possible voltage to 900 V.

### 3.2 Switch Driver and PWM Modulation

Next, the driver for switches  $S_1$  and  $S_2$  is designed. The duty cycle  $D$  is defined as the fraction of the switching period during which switch  $S_1$  is turned on. Since in this case  $S_2$  is the switch connected to the boost inductor,  $D$  represents  $1 - D$  of  $S_2$ .

The PWM modulation scheme is implemented as shown in Fig. 6. A triangular carrier signal is compared with the calculated duty cycle to generate the gate signals.

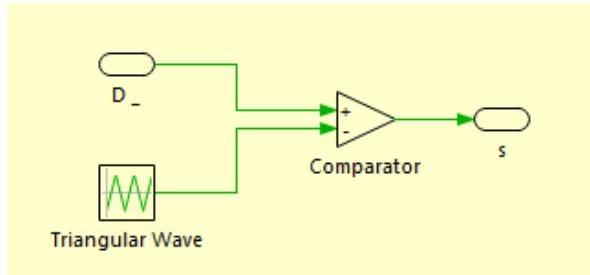


Figure 6: PWM generator

### 3.3 Inductor Design

The inductance is designed to ensure a sufficiently small current ripple. According to the exercise specifications, the peak-to-peak current ripple is limited to 30% of the average input current [4]. At the MPP, the average input current is  $I_{\text{MPP}} = 15.22\text{A}$  [2]. Thus, the maximum allowable current ripple at a switching frequency of 70 kHz is

$$\Delta I_{\text{max}} = 0.3I_{\text{MPP}} = 4.746\text{A}. \quad (1)$$

Using the inductor voltage-current relation

$$V_L = L \frac{di_L}{dt} \quad (2)$$

With  $V_{L_{MPP}} = 578.6 \text{ V}$ ,  $D = \frac{578.6}{750}$  and  $\Delta t = D * 1/70000 \text{ s}$  the required inductance is calculated to be

$$L = 0.4137 \text{ mH}. \quad (3)$$

The resulting current ripple is verified in Fig. 7. To ensure precise simulation the maximal step size is set to  $1\mu\text{s}$

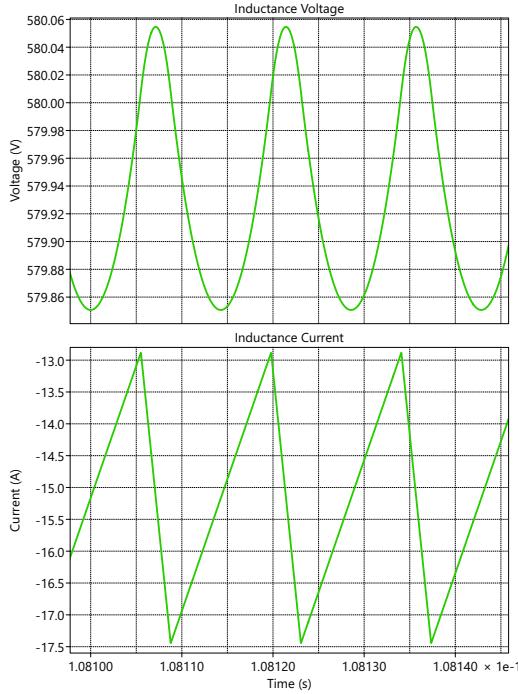


Figure 7: PV voltage  $V_{\text{pv}}$  and inductor current  $i_L$

### 3.4 Inductor Series Resistance

The inductor series resistance  $R_L$  is chosen such that only 0.1% of the MPP power is dissipated in the inductor. At the MPP, a power of  $P_{\text{MPP}} = 8800 \text{ W}$  is delivered at a current of  $I_{\text{MPP}} = 15.22 \text{ A}$ . The corresponding resistance is

$$R_L = \frac{0.001 P_{\text{MPP}}}{I_{\text{MPP}}^2} = \frac{0.001 * 8800 \text{ W}}{(15.22 \text{ A})^2} = 0.03799 \Omega. \quad (4)$$

### 3.5 Input Capacitor Design

The input capacitance is designed to limit the amplitude of the high-frequency voltage components to 5 mV at frequencies greater than 150 kHz. The worst-case voltage ripple occurs at a duty cycle of  $D = 0.5$ . The current function of the capacitor can be obtained by a Fourier series, as shown in the following equation:

$$I_C(t) = \sum_{k \in \mathbb{N}} \frac{11}{\pi^2 * k^2} * (\cos(k * \pi) - 1) * \cos\left(\frac{k * 2 * \pi}{T} * t\right) \quad (5)$$

With  $T = \frac{1}{70000}$  s, the largest amplitude of the high-frequency components occurs at  $k = 3$ , resulting in  $\hat{I}_C = 0.2477$  A. A value of  $\hat{I}_C = 0.3$  A is used to ensure a sufficient safety margin. Additionally, the third harmonic can be analyzed using a Fourier spectrum over 10 switching periods to validate the amplitude (Figure 8).

In this Fourier spectrum, we observe that the largest amplitude for frequencies greater than 150 kHz occurs at 210 kHz, confirming that this is the relevant frequency. Higher-frequency ripples are present but significantly smaller in amplitude. Since their contribution to the transferred charge is minimal, they can be neglected.

Under these conditions, the required capacitance is calculated using

$$\hat{I}_C = \omega C \hat{V}_C \quad (6)$$

In this equation,  $\hat{I}_C = 0.3$  A and  $\omega = 2\pi f$ .  $\hat{V}_C$  is equal to 5 mV

$$C = \frac{\hat{I}_C}{\omega \hat{V}_C} \quad (7)$$

This results in a required capacitance of

$$C = 45.472 \mu\text{F} \quad (8)$$

The voltage ripple is verified in Fig. 8. At the frequency of 210 kHz, we can see a voltage amplitude of 4.87 mV, which aligns with our requirements.

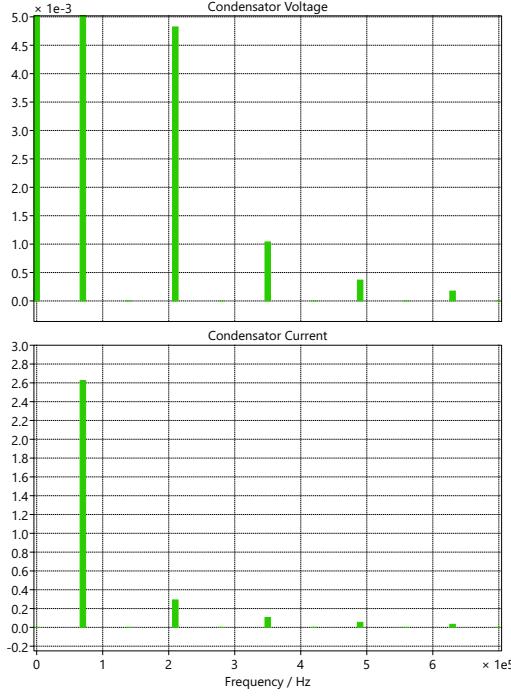


Figure 8: PV voltage ripple  $V_{pv}$

In order to ensure a safety margin, a capacitance of  $50 \mu\text{F}$  is used.

### 3.6 Duty Cycle Calculation

The duty cycle is calculated from the DC-link voltage and the input voltage. Due to easier implementation,  $1 - D$  of  $S_2$  is calculated and processed in the switch driver. This equals  $D$  of  $S_1$ , as requested in the task [1]. The corresponding implementation is shown in Figure 9.

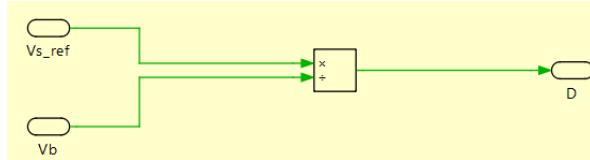


Figure 9: Duty-cycle calculation

### 3.7 Open-Loop Voltage Response

Finally, the open-loop response of the PV voltage  $V_{pv}$  is evaluated. For this purpose, the switch voltage  $V_s$  is stepped from 400 V to 410 V. The resulting transient response is shown in Figure 10.

The voltage of the PV is offset by 0.62 V because of the current flowing through the series resistance in the inductor. An overshoot of the PV voltage of 9.78 V (97.8%) can be observed, as shown in Figure 10.

The voltage value settles to less than 2% of the overshoot (0.1956 V) 0.073 s after the step at 0.5 s. This information can be obtained from Figure 11, as the voltage reaches the corridor of  $410.62 \text{ V} \pm 0.1956 \text{ V}$ .

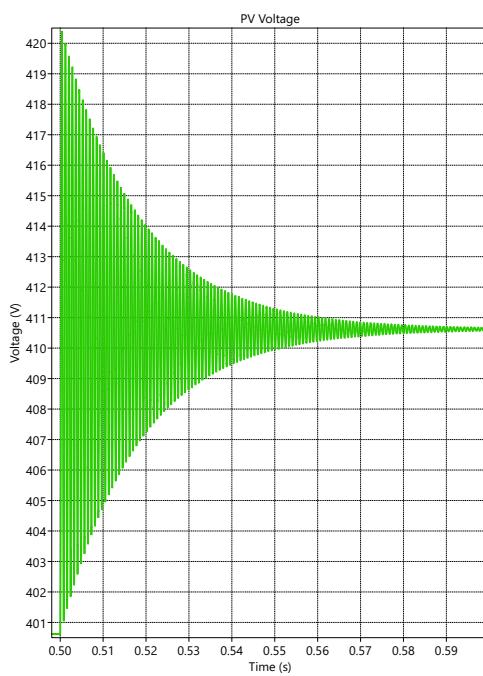


Figure 10: Step response PV voltage

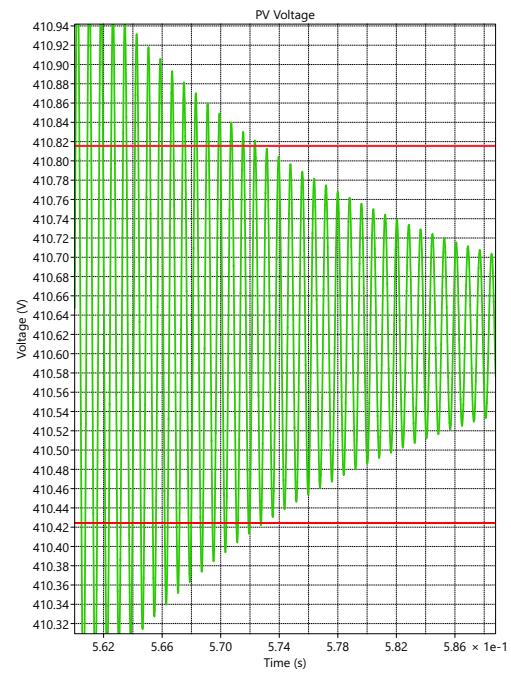


Figure 11: Step response PV voltage in 2% margin

## 4 Controller Design

Firstly to design the controller it is important to define the polarity of the currents and voltages. Therefore the circuit is displayed. For easier and consistent calculation the sign of  $i_L$  is flipped.

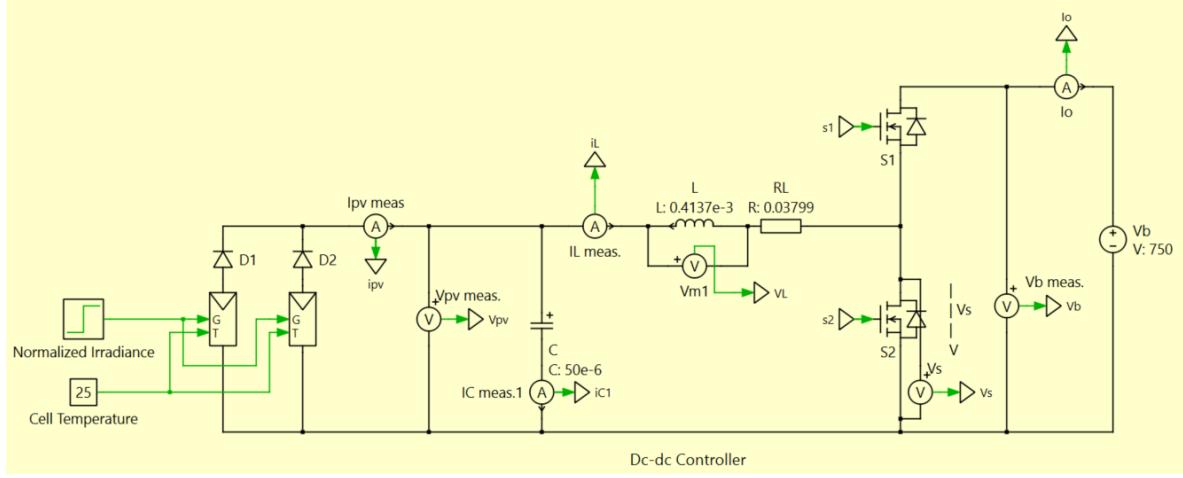


Figure 12: Circuit of the boost converter

### 4.1 Linearized model

The basis of the design are the inductor voltage and capacitor current equations. Since  $d$  represents the on time of  $s_1$  the voltage of  $v_b$  reaches the loop of the inductor voltage at  $D * T_s$

$$\text{Inductor voltage equation: } L \frac{di_L}{dt} = v_{pv} - d v_b - R_L i_L \quad (9)$$

$$\text{Capacitor current equation: } C \frac{dv_{pv}}{dt} = i_{pv} - i_L \quad (10)$$

To get the correlation between small deviations from the equilibrium we introduce the  $\tilde{x}$  operator, which represents a small deviation from the operating point.

Due to the inversion of the inductor current the following equations represent the derivative of the inductor current and capacitor voltage.

$$\frac{d\tilde{i}_L}{dt} = \frac{1}{L} \tilde{v}_{pv} - \frac{R_L}{L} \tilde{i}_L - \frac{V_b}{L} \tilde{d} - \frac{D}{L} \tilde{v}_b \quad (11)$$

$$\frac{d\tilde{v}_{pv}}{dt} = -\frac{1}{C} \tilde{i}_L \quad (12)$$

The inputs and outputs of the control system are given as:

$$x = \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{pv} \end{bmatrix}, \quad u = \begin{bmatrix} \tilde{d} \\ \tilde{v}_b \end{bmatrix} \quad (13)$$

This leads to the following system:

$$\dot{x} = Ax + Bu = \begin{bmatrix} -\frac{R_L}{L} & \frac{1}{L} \\ -\frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \tilde{i}_L \\ \tilde{v}_{pv} \end{bmatrix} + \begin{bmatrix} -\frac{V_b}{L} & -\frac{D}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{d} \\ \tilde{v}_b \end{bmatrix} \quad (14)$$

## 4.2 Transfer Functions & State Space Model

To get the Transfer Functions the same steps were used as in Tutorial 3 [5]. The transfer function translates the input deviation for the operating point into an output deviation:

$$G(s) = (sI - A)^{-1}B = \begin{bmatrix} G_{id}(s) & G_{ib}(s) \\ G_{vd}(s) & G_{vb}(s) \end{bmatrix} \quad (15)$$

The outputs are calculated based on the transfer function:

$$\begin{bmatrix} \tilde{i}_L(s) \\ \tilde{v}_{pv}(s) \end{bmatrix} = G(s) \begin{bmatrix} \tilde{d}(s) \\ \tilde{v}_b(s) \end{bmatrix} \quad (16)$$

Using linear algebra the transfer function can be calculated from A and B.

$$sI - A = \begin{bmatrix} s + \frac{R_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & s \end{bmatrix}$$

Using the determinant of the equation above the inverse is calculated to be:

$$(sI - A)^{-1} = \frac{1}{s^2 + \frac{R_L}{L}s + \frac{1}{LC}} \begin{bmatrix} s & \frac{1}{L} \\ -\frac{1}{C} & s + \frac{R_L}{L} \end{bmatrix} \quad (17)$$

Multiplication with B yields the transfer function:

$$G(s) = \frac{1}{s^2 + \frac{R_L}{L}s + \frac{1}{LC}} \begin{bmatrix} -\frac{V_b}{L}s & -\frac{D}{L}s \\ \frac{V_b}{LC} & \frac{D}{LC} \end{bmatrix} \quad (18)$$

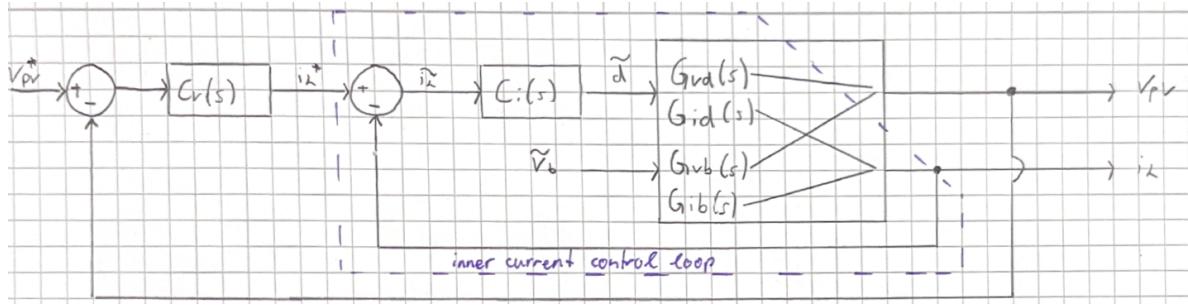


Figure 13: Block Diagram of the Boost Converter with Transfer Functions

Figure 13 shows the transfer functions of the system embedded in the Block Diagram of the boost converter with two inputs and two outputs. The transfer functions shown in Equation 18 are the basis of the controller design.

### 4.3 Current Controller Design - Transfer Functions

Since the duty cycle is the only input that is actively controllable its transfer function should be used to design the current controller.

That leaves:

$$G_{id}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = -\frac{s}{s^2 + \frac{R_L}{L}s + \frac{1}{LC}} * \frac{V_b}{L} \quad (19)$$

This transfer function is characterized by one root and two poles, whereas the simplified form is characterized by one pole.

$$G_{id,simp}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} \approx -\frac{V_b}{s * L + R_L} \quad (20)$$

In reality the LC-circuit forms a resonant system resulting in the two poles, the simplified transfer function assumes an RL-circuit. We choose low frequencies since then the reactance of the capacitor is really high and its current does not affect the inductor as much.

The real system features a resonance at  $f_{res} = \sqrt{\frac{2\pi}{LC}} = 1106.6 \text{ Hz}$ . This hugely influences the stability of the control system. As expected, the phase is  $+90^\circ$  at low frequencies. Below the LC resonance, the capacitor impedance is high, so changes in duty cycle mainly appear as voltage across the inductor. Since the inductor current responds to the rate of change of this voltage, the system behaves like a differentiator in this frequency range.

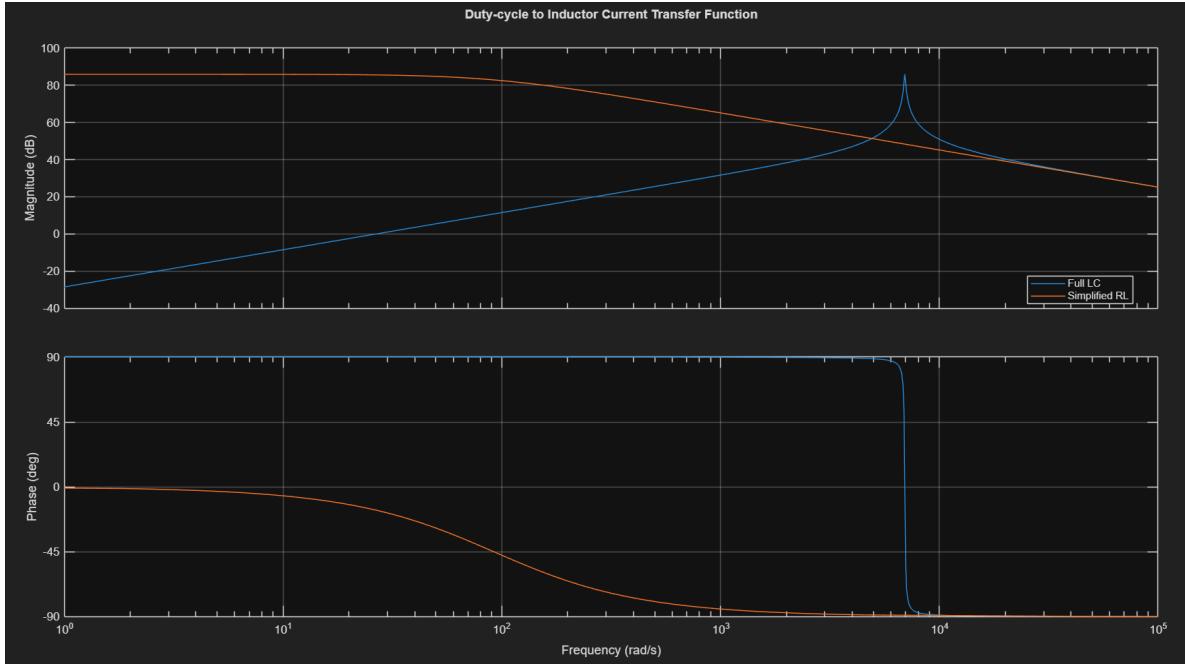


Figure 14: Gain and Phase of the Systems  $G_{id}(s)$  and  $G_{id,simp}(s)$

The MatLab export shows the positive transfer functions, which means that the Controller Parameters need to be negative, because of the  $i_L$  and  $d$  relationship.

#### **Gain and Phase of the Systems $G_{id}(s)$ and $G_{id,simp}(s)$**

The simplified version is missing the C behaviour, which results in a low-pass filter rather than the original band-pass filter. From the Bode plot (Figure 14) we can see that the behaviours align from 3 kHz onward, so the simplified version can also be used for transfer functions with a crossover frequency greater than 3 kHz. This is advantageous for the following tasks, as we aim to design our controller for frequencies above 7 kHz.

The stability analysis still needs to be performed on the full transfer function, since the resonance can have an effect on the stability and the phase drops rapidly by  $180^\circ$ .

#### **4.4 Current Controller Design - Controller Parameters**

First the simplified transfer function is analyzed by replacing the capacitor with a voltage source. The setup is shown in Figure 15, the subsequent switches and the DC-Link voltage stay the same as before. The voltage is stepped from 550 to 580 Volts to check if the controller is able to adapt the duty cycle. The current reference is also stepped from 12 to 15 Ampere to see whether the controller manages to regulate the current.

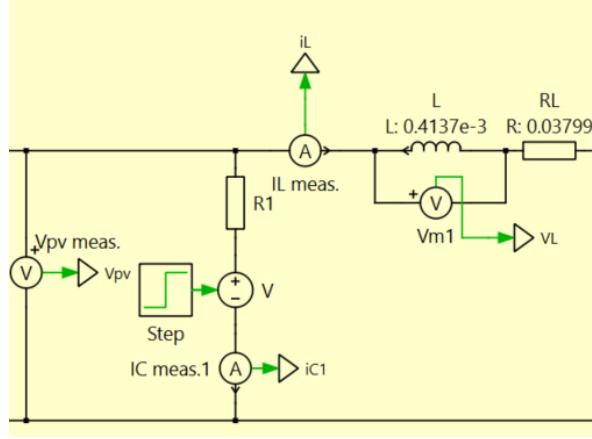


Figure 15: Simplified circuit to test the current controller

To design the controller the crossover-frequency specific  $K_p$  and  $K_I$  need to be calculated. The Open Loop Gain at the crossover frequency is given by:

$$|G_c(j\omega_c) G_p(j\omega_c)| = 1 \quad (21)$$

$$G_p(s) = G_{id}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_b}{L} \frac{s}{s^2 + \frac{R_L}{L}s + \frac{1}{LC}} \quad (22)$$

$$G_c(s) = C_i(s) = K_p + \frac{K_i}{s} \quad (23)$$

By evaluation the Open-Loop Gain at the crossover frequency  $K_p$  can be calculated. By setting  $\omega_i = \omega_c$  a phase margin of  $45^\circ$  is reached. For verification purposes this phase margin is accepted as close enough to  $50^\circ$ .  $K_p$  is calculated as follows.

$$K_p = \frac{\omega_c L}{\sqrt{2}V_b} \quad (24)$$

The MatLab files to calculate the values and analyze the open-loop behaviour are turned in with the report. To create comparable results all controllers are tested under the same conditions. Voltage step of 30 V after 0.1 seconds and current step by 3 A after 0.3 seconds. In the simplified loop they are all stable.

From this point on all controller parameters are negative, because the duty cycle represents the On-Time of the upper switch and the current through the inductor was chosen as positive from the input towards the output!

$f_c$	$K_p$	$K_i$	P Margin (real)	Stable (V step)	d Variation	Overfit Ripple
7 kHz	-0.0171549	-754.51	$45.7^\circ$	Yes	0.07	High
14 kHz	-0.0343097	-3018.04	$45.1^\circ$	Yes	0.17	Severe

Table 4: Comparison of PI current controllers for different crossover frequencies

True stability can only be decided after the voltage controller is implemented, since the transfer function with the voltage step equals the simplified one. The voltage controller and joint stability is addressed in the next part of the report.

## 4.5 Voltage Controller Design

The boost converter in this model is a two-input two-output system with the small-signal inputs being the duty-cycle perturbation  $\tilde{d}$  and the output voltage perturbation  $\tilde{v}_b$ , and the outputs being the inductor current  $\tilde{i}_L$  and the PV voltage  $\tilde{v}_{pv}$ . For voltage controller design, the disturbance  $\tilde{v}_b$  is neglected.

The duty-to-voltage dynamics can be decomposed into a cascade of a duty-to-current and a current-to-voltage transfer function,

$$\tilde{d}(s) \xrightarrow{G_{id}(s)} \tilde{i}_L(s) \xrightarrow{G_{vi}(s)} \tilde{v}_{pv}(s), \quad (25)$$

which implies

$$G_{vd}(s) \approx G_{id}(s) G_{vi}(s), \quad G_{vi}(s) = \frac{G_{vd}(s)}{G_{id}(s)}. \quad (26)$$

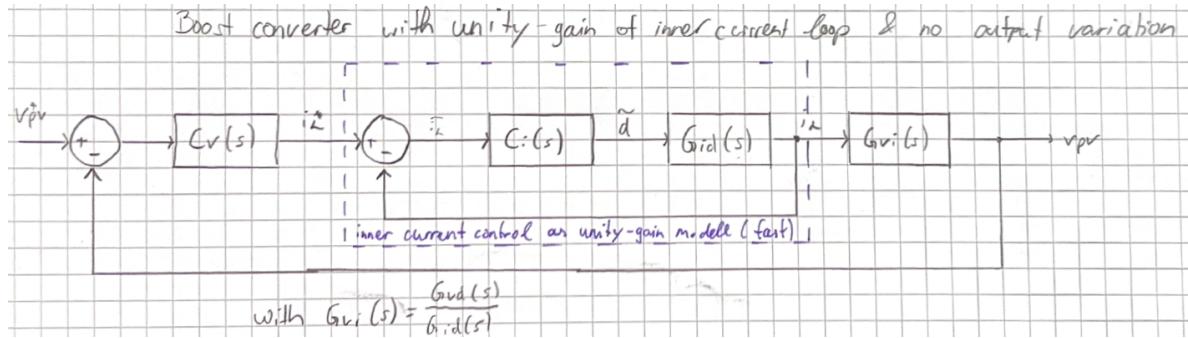


Figure 16: Block Diagram based on Current Control Loop Simplification

Using the diagram shown, and assuming that the inner current control loop is much faster than the voltage control loop, it can be approximated as a unity-gain, instantaneous current translation. This allows the voltage controller to be designed and tuned using only the voltage controller  $C_v(s)$  and the current-to-voltage transfer function  $G_{vi}(s)$ .

### Derivation of the voltage plant

The capacitor  $C$  is located at the input of the boost converter and stabilizes the PV voltage  $v_{pv}$ . The capacitor current is given by

$$i_C(t) = C \frac{dv_{pv}(t)}{dt}. \quad (27)$$

Applying Kirchhoff's current law at the PV-side capacitor node yields

$$\tilde{i}_{PV}(t) = \tilde{i}_C(t) + \tilde{i}_L(t). \quad (28)$$

Assuming that the small-signal perturbation of the PV source current is negligible,  $\tilde{i}_{PV} \approx 0$ , the capacitor current becomes

$$\tilde{i}_C(t) = -\tilde{i}_L(t). \quad (29)$$

Substituting into the capacitor equation gives

$$C \frac{d\tilde{v}_{pv}(t)}{dt} = -\tilde{i}_L(t), \quad (30)$$

and taking the Laplace transform yields

$$G_{vi}(s) = \frac{\tilde{v}_{pv}(s)}{\tilde{i}_L(s)} = -\frac{1}{Cs}. \quad (31)$$

The negative sign is absorbed in the feedback loop, such that the plant seen by the voltage controller is a pure integrator.

### Controller structure and tuning

A PI controller is used to regulate the PV voltage and generate the reference inductor current  $i_L^*$ ,

$$C_v(s) = K_P \left( 1 + \frac{\omega_i}{s} \right). \quad (32)$$

The inner current control loop has a crossover frequency of 7 kHz. To ensure sufficient bandwidth separation between the cascaded control loops, two voltage loop crossover frequencies are selected,

$$f_{cv} \in \{700 \text{ Hz}, 1750 \text{ Hz}\}, \quad (33)$$

both targeting a phase margin of approximately  $60^\circ$ .

For an integrator plant, the phase margin is determined by the location of the PI zero. The zero is therefore placed at

$$\omega_i = 0.5 \omega_c, \quad \omega_c = 2\pi f_{cv}. \quad (34)$$

0.5 was chosen as the "zero-frequency" of the PI controller through trial and error to increase the phase margin.

### Gain calculation

The controller gains are obtained from the magnitude condition at the crossover frequency,

$$|C_v(j\omega_c)G_{vi}(j\omega_c)| = 1. \quad (35)$$

Solving for the proportional and integral gains yields

$$K_P = \frac{C\omega_c}{\sqrt{1 + (\omega_i/\omega_c)^2}}, \quad K_I = K_P \omega_i. \quad (36)$$

## Numerical results

The resulting controller parameters and achieved phase margins are summarized in Table 5.

$f_{cv}$ [Hz]	$K_P$	$K_I$	Phase Margin [°]
700	-0.1967	-432.5545	63.43
1750	-0.4917	-2703.4655	63.43

Table 5: Voltage controller parameters and achieved phase margins

If these parameters result in a stable closed loop control will be analyzed in the next part. The phase margins are as targeted, but if the bandwidth separation from the inner current control loop is sufficient needs to be tested through simulation.

## Simulation results and Closed Loop Stability

Ultimately the two loops are connected to fully design the Boost controller. The following table will describe all the possible combinations and check stability.

	$f_{ci} = 7\text{ kHz}$	$f_{ci} = 14\text{ kHz}$
$f_{cv} = 700\text{ Hz}$	<b>Closed Loop Stability</b>	<b>Closed Loop Stability</b>
	Yes	No
$f_{cv} = 1750\text{ Hz}$	<b>Closed Loop Stability</b>	<b>Closed Loop Stability</b>
	No	No

Table 6: Assessment of cascaded control stability

As the table demonstrates, only one combination of control parameters guarantees stability of the whole system. The resonance of the LC circuit influences the stability. Since  $G_{vi}$  only models the capacitor dynamics and assumes unity gain of the inner current control loop, this assumption is only valid when a clear time-scale separation between the cascaded loops is maintained. Consequently, the current control loop can only be assumed a unity-gain system with  $f_{cv} \ll f_{ci}$ .

Figure 17 displays a 1 ms window of the reaction of the boost converter to a step in output voltage  $v_b$  from 750 to 800 V. It is clear, that the controller acts rapidly and precise. The input voltage  $v_{pv}$  only shifts marginally and stabilises very quickly.

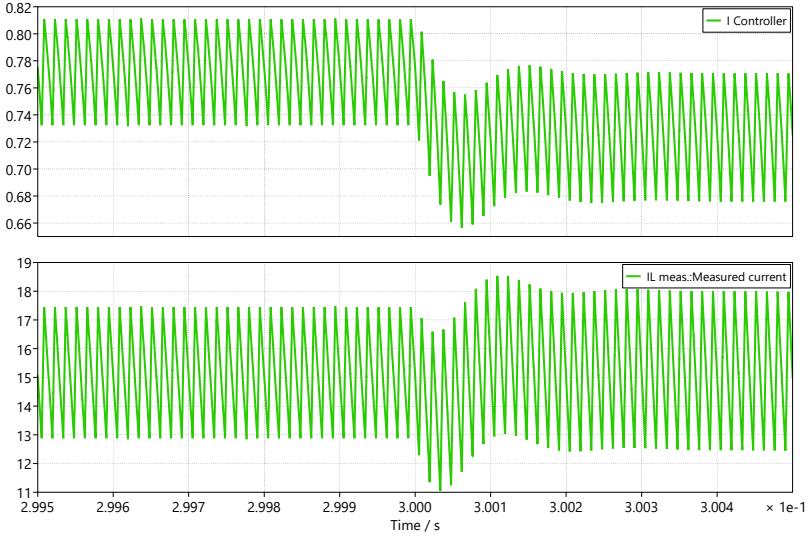


Figure 17: Reaction of the current controller and current to a Step in Output Voltage

The controllers are:

$$C_v(s) = -(0.1967 + \frac{432.6}{s}), \quad C_i(s) = -(0.017155 + \frac{754.51}{s}) \quad (37)$$

#### 4.6 Voluntary - Controller Optimization

The stability of the full closed-loop current controller can only be validated correctly after the Voltage controller has been implemented, since before the capacitor was replaced by a voltage source.

Now that the full loop is implemented some optimization is possible, by still keeping the same crossing frequency. Now the inner current loop is not assumed to be a unity gain system but also respected in the parameter evaluation for the voltage controller. The MatLab code is attached as `voluntary_optimal_cascaded_desing.m`

#### Problem with current design

The current problem of the controller comes from the improvable phase margin of the inner current control loop. At the moment the duty cycle varies quite a lot and follows the current ripple. Therefore an averaging of the current or low-pass filtering of the feed-back current would help reducing said ripple.

With the current parameters the controller becomes nstable as more phase lag is introduced by a filter.

## Treatment

Now both controllers are redesigned. The zero-frequency of the current loop is laid at the same frequency as the resonance. This improves the phase margin of the inner controller. This though makes the phase margins of the controllers deviate from the task; therefore for the discussions in further tasks the old parameters are used.

The new control parameters are:

$$C_v(s) = - \left( 0.21082 + \frac{463.625}{s} \right), \quad C_i(s) = - \left( 0.02336 + \frac{162.452}{s} \right) \quad (38)$$

Now a moving average filter over two periods of current ripple can be introduced. Figure 18 shows that the deviation of the duty cycle is greatly reduced, while still dealing with the deviation in DC-Link voltage.

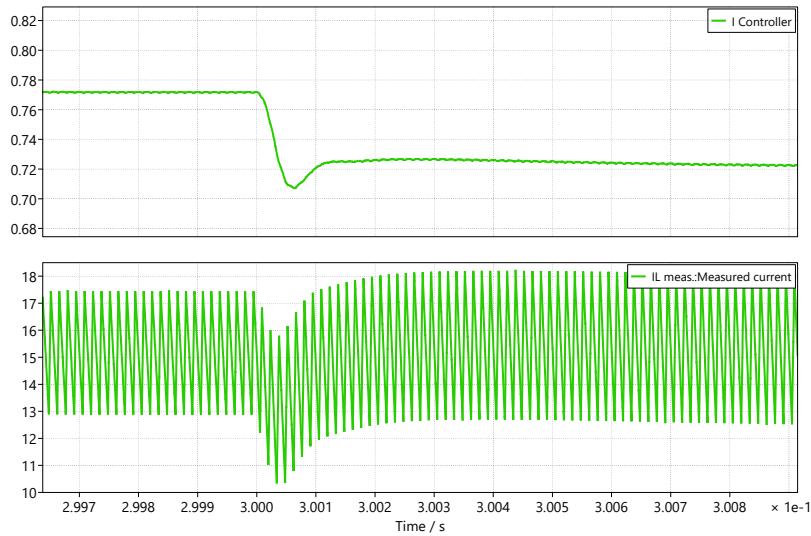


Figure 18: Duty cycle ripple with moving average filter of feedback

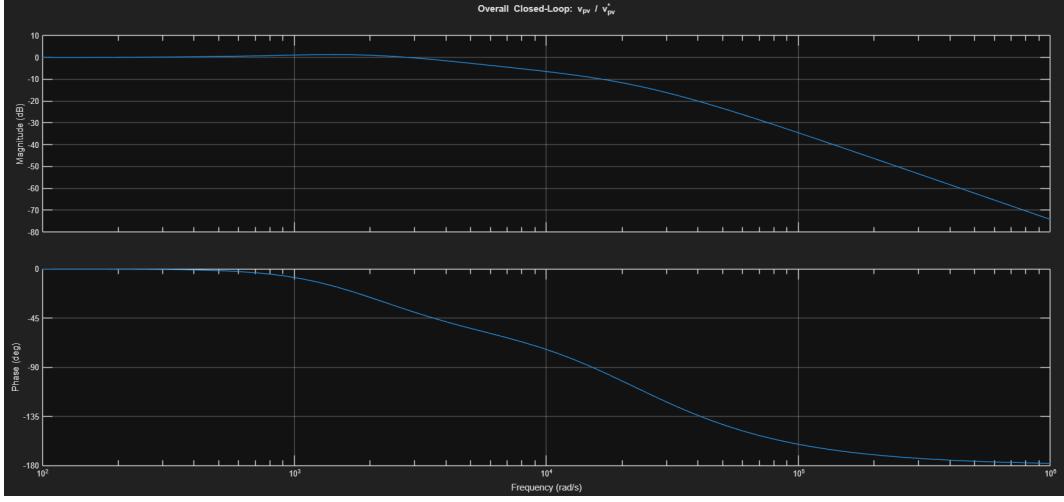


Figure 19: Closed Loop Bode Diagram of the full control system

Figure 19 shows the closed loop Bode Diagram. One can see, that for low frequencies the translation of desired voltage to actual expected voltage lies on the 0dB line. For higher frequencies it falls monotonic and also around the resonance frequency there are no severe peaks.

Therefore the controller is expected to work well.

## 4.7 Bonus Tasks

### 4.7.1 Redesign of the Voltage Controller Including Current Loop Dynamics

The voltage controller should take into account the dynamics of the inner current loop. The small-signal plant from inductor current to DC bus voltage is

$$G_{vi}(s) = \frac{\tilde{v}_{pv}(s)}{\tilde{i}_L(s)} = -\frac{1}{Cs}, \quad (39)$$

and the closed-loop current controller can be represented as

$$T(s) = \text{feedback}(G_c(j\omega_c) G_p(j\omega_c)), \quad (40)$$

$$G_p(s) = G_{id}(s) = \frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_b}{L} \frac{s}{s^2 + \frac{R_L}{L}s + \frac{1}{LC}} \quad (41)$$

$$G_c(s) = C_i(s) = K_p + \frac{K_i}{s} \quad (42)$$

which leads to the effective plant for voltage control:

$$G_{vi,\text{new}}(s) = T(s) G_{vi}(s). \quad (43)$$

The slower and faster voltage controller designs produce responses similar to those of the original controllers, demonstrating that even the simplified cascade architecture captures the system behavior

$f_{cv}$ [Hz]	$K_P$	$K_I$	Phase Margin [°]
700	-0.1939	-426.5086	63.43
1750	-0.4510	-2479.6236	62.09

Table 7: Voltage controller parameters and achieved phase margins

reasonably well. However, the degree of deviation differs between the two designs.

The 700 Hz controller operates effectively as a unity-gain element, meaning that changes in the ten times faster current controller have little influence on its behavior. As a result, its response closely matches that of the original controller.

In contrast, the 1750 Hz controller is only four times slower than the current controller. Because of this smaller separation in bandwidth, it begins to capture some of the faster dynamics within the current control loop. Consequently, it is more affected by the feedback interaction and deviates slightly more from the original controller. This is also reflected in the phase margin, which decreases from 63.43° to 62.09°.

#### 4.7.2 Short-Circuit Event between PV String and Boost Input

For a short circuit of  $0.05 \Omega$  between the PV array and the boost input to ground (Figure 20), the input voltage collapses nearly to zero.

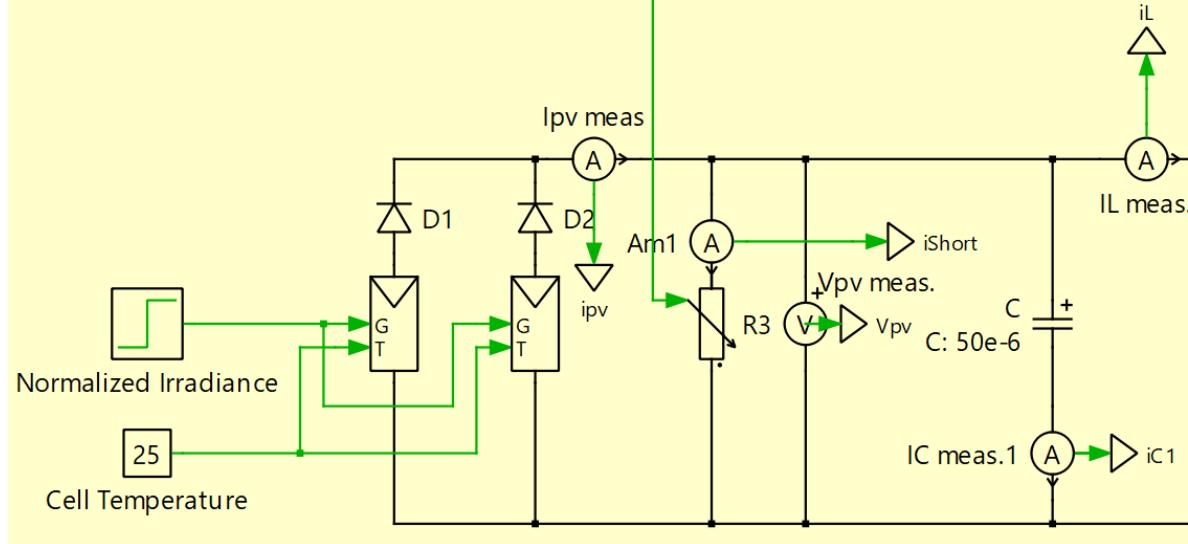


Figure 20: Short circuit across  $R_3$

To stabilize the voltage, the controller attempts to draw the maximum possible current from the PV string, which is limited to 16 A according to the datasheet. Since the short-circuit resistance is very low, the PV current is insufficient to prevent the voltage collapse. As a result, the controller increases the duty cycle, causing current to be drawn from the DC bus. This drives the inductor current into large negative values, which would damage the components.

The controller ramps the duty cycle of  $S_1$  up to 1, but due to  $R_L$ , a voltage divider forms, making it impossible to reach 580 V across the short. Consequently, the controller becomes unstable, and the voltage remains at the level corresponding to a fully opened Switch 2. All of these behaviors can be observed in Figure 21.

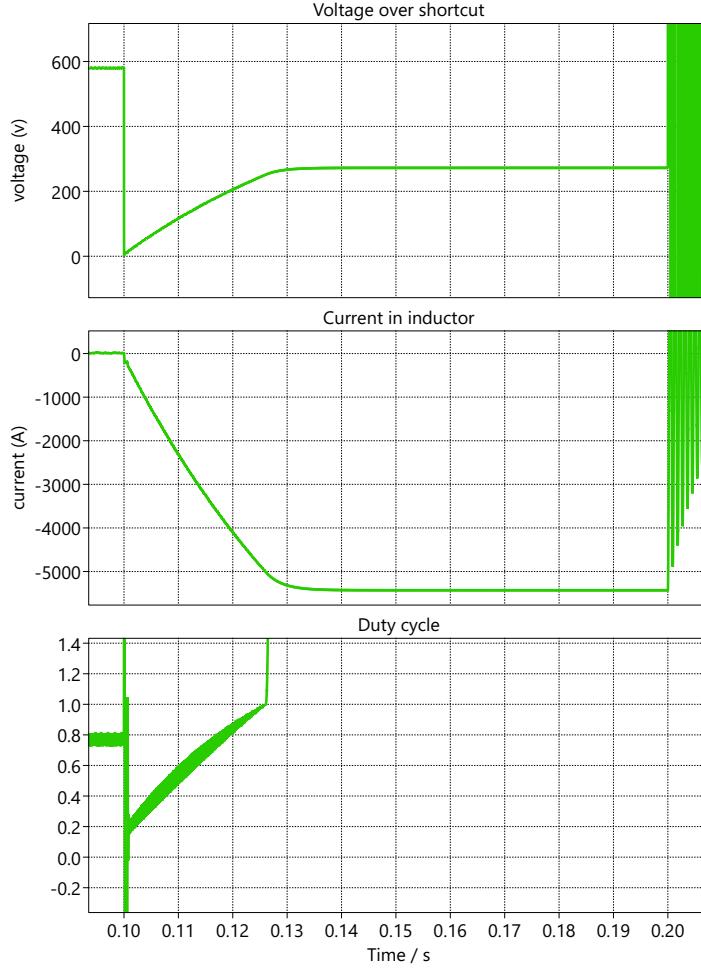


Figure 21: Voltage, current, and duty cycle during the short circuit

This behavior can be prevented by the following measures:

#### Prevention measures:

1. **Cycle-by-cycle current limiting:** Limit the inductor current and switch off immediately if the limit is exceeded.
2. **Voltage controller anti-windup:** Limit the output of the voltage controller to a safe current reference.
3. **Undervoltage or short-circuit detection:** Disable switching or enter a safe mode if the PV

voltage collapses.

4. **Soft ramping of voltage references:** Avoid large steps between  $V_{\text{ref}}$  and  $V_{PV}$  by applying rate limiting.
5. **Duty-cycle limits or forced minimum off-time:** Prevent excessive on-time and uncontrolled current rise.

A slower voltage controller reduces the aggressiveness of the response but cannot prevent the open-loop current rise, which is a physical phenomenon.

#### 4.7.3 Small-Signal Transfer Function and Bode Analysis

As shown in subsection 4.2 there is a transfer function that directly relates the DC-Link variance directly to input voltage variance.

The controller values from Bonus Task (g) in Table 7 at 700 Hz are used to describe the voltage controller. The inner current loop with crossover frequency of 7000 Hz is used.

$$G_{vb}(s) = \frac{\tilde{v}_{pv}(s)}{\tilde{v}_b(s)} = \frac{D}{LC} \frac{1}{s^2 + \frac{R_L}{L}s + \frac{1}{LC}}$$

As known from control theory basics the closed loop transfer function of a disturbance directly affecting the system is given as:

$$\frac{\tilde{v}_{pv}(s)}{\tilde{v}_b(s)} = \frac{G_{vb}(s)}{1 + L_v(s)}$$

where  $L_v(s) = C_v(s) G_{vi}(s) T_i(s)$  is the open-loop transfer function of the outer voltage control loop.

For frequencies well below the voltage-loop crossover frequency of 700 Hz, the magnitude of the open-loop transfer function satisfies  $|L_v(j\omega)| \gg 1$ . Consequently, the disturbance-to-output transfer function can be approximated as

$$\left| \frac{\tilde{v}_{pv}(j\omega)}{\tilde{v}_b(j\omega)} \right| \approx \frac{|G_{vb}(j\omega)|}{|L_v(j\omega)|} \ll 1, \quad (44)$$

which implies a strong rejection of low-frequency dc-link voltage ripple by the voltage controller.

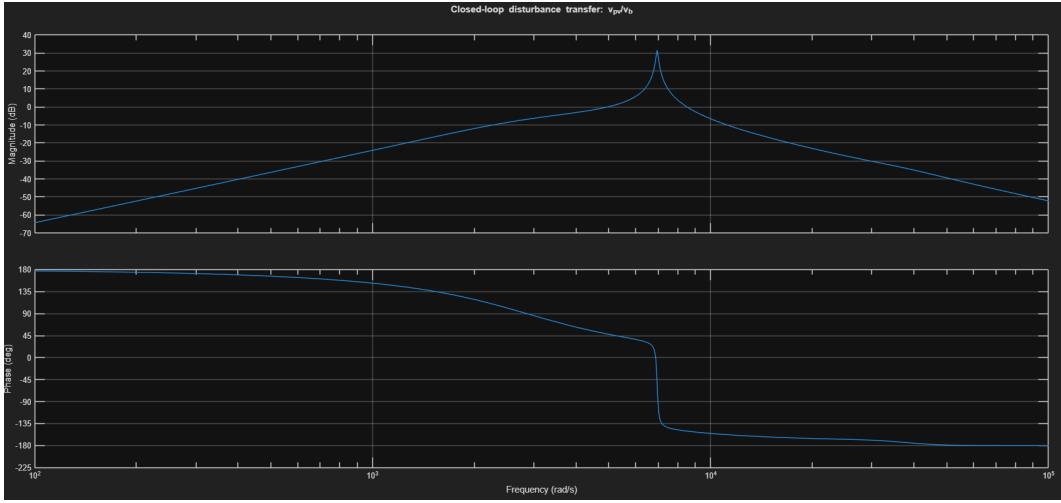


Figure 22: Closed Loop Disturbance Transfer Function of the DC-Link deviation to input voltage

Figure 22 shows that for low frequencies disturbances are highly suppressed whereas disturbances around the resonance frequencies could lead to instability.

Disturbances of 100 Hz show an amplitude of  $-32.3\text{ dB}$ . Therefore the 10 V ripple requested in task (j) should have an amplitude of 0.234 V at the input. This is tested through simulation.

#### 4.7.4 Simulation with 100 Hz Sinusoidal Ripple

By adding a 100 Hz, 10 V amplitude sinusoid to the DC bus voltage in simulation, the input ripple can be checked using FFT.

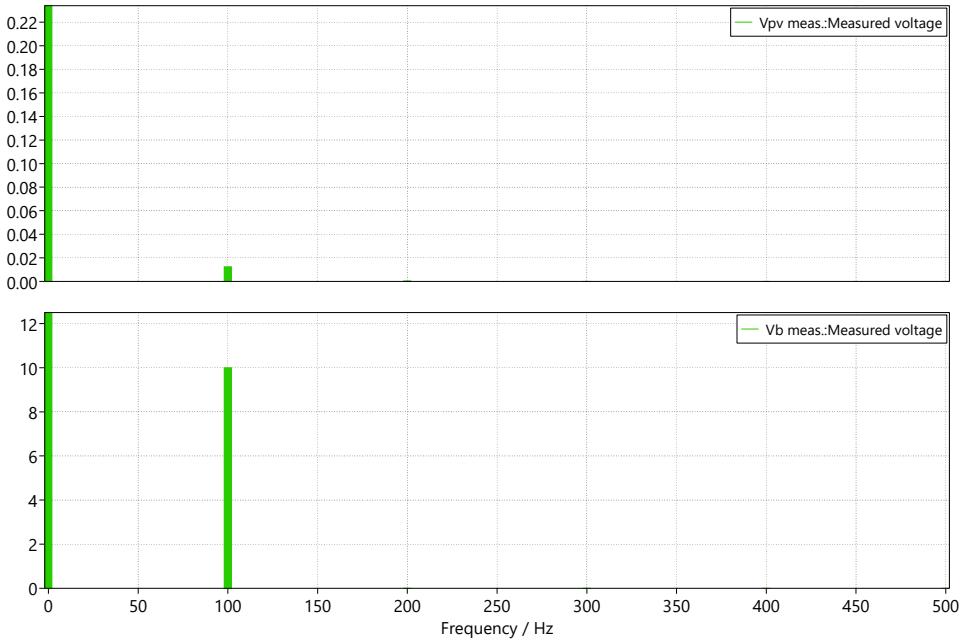


Figure 23: FFT of the PV Voltage and the DC Link Voltage with a 10V ripple

For the amplitude of the PV Voltage in Figure 23 the before expected 0.234 Volts are used as the maximum value for reference. The amplitude at 100 Hz is barely visible, showing that the MatLab solution does not fit the simulation. In reality the ripple that reaches the PV Module Voltage is way smaller than simulated.

The main reason is, that the controllers act faster than the 100 Hz ripple and manage to adjust the duty cycle dynamically resulting in a lower ripple than anticipated. Therefore the input voltage can be kept more or less constant.

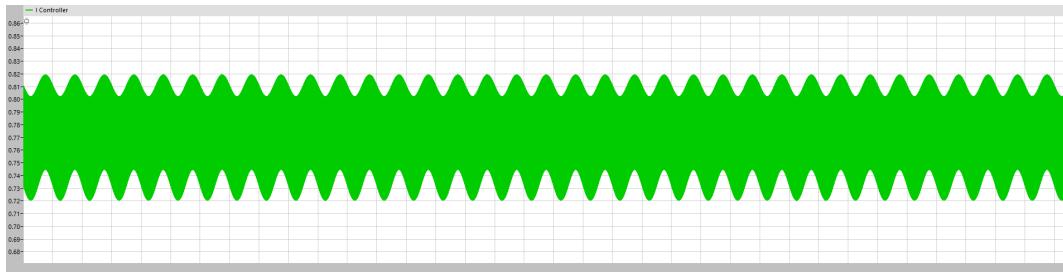


Figure 24: Duty cycle modulation as a result of the DC-Link ripple

One can see that the controller dynamically adjusts the duty cycle, which the MatLab small-signal-simulation does not respect, therefore the real effect of the disturbance is lower than assumed.

Just as a note here, also disturbances around the resonance frequency do not lead to a

#### 4.7.5 Duty-Cycle Compensation for Improved Disturbance Rejection

Now that it is shown that the feedback control already greatly reduces the impact of the DC-Link voltage variation and stabilizes it quite well feedforward control straight into the output is added to further diminish the impact.

To diminish the impact of the variation in the DC-Link voltage the following relationship should come close to 0 by adjusting the duty cycle:

$$D_0 \tilde{v}_b + V_{b0} \tilde{D}_{ff} \approx 0 \quad (45)$$

This leads to an feedforward duty cycle addition of  $\tilde{D}_{ff} = -\frac{D_0}{V_{b0}} \tilde{v}_b$ , which is added to the regular duty cycle given by the controller.

In Plecs the averaging of  $D_0$  and  $V_{b0}$  is done by moving average filters. For the duty cycle they are 2 periods of the current ripple whereas for the DC-Link Voltage they averaging happens over 2 sine waves or 0.02 s.

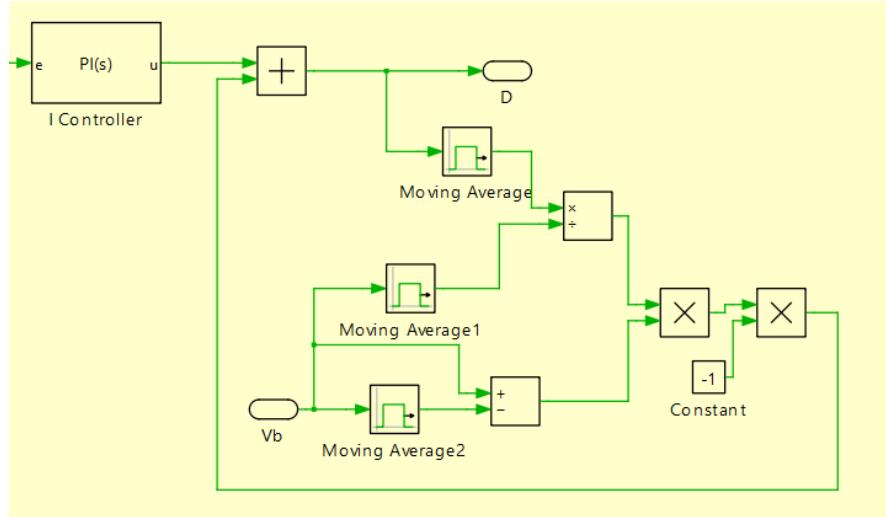


Figure 25: Setup of the feedforward compensation of DC-Link Voltage deviation

Figure 25 shows how the compensation is realized in Plecs. The following graphic shows the FFT of the PV-Voltage and the DC-Link voltage as in task (j).

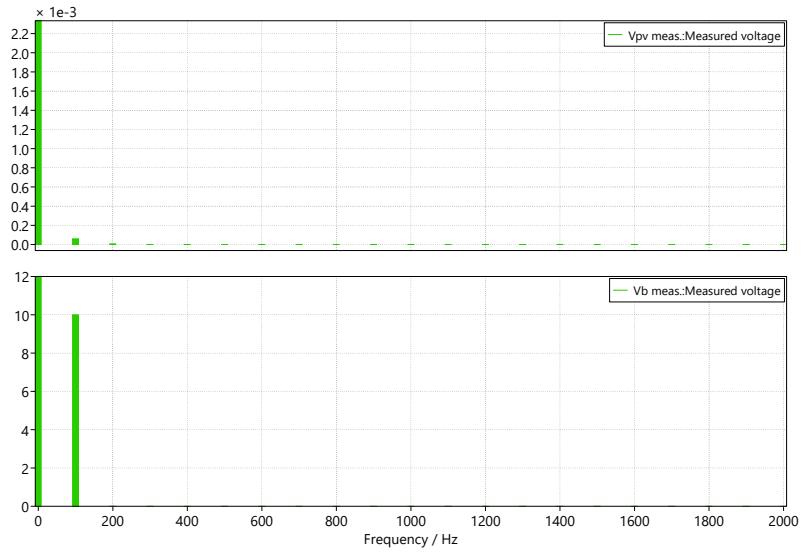


Figure 26: FFT of PV -and DC-Link voltage as in Figure 23

Now the deviation of the PV-Voltage is negligible. To compare without the feedforward compensation it is by two magnitudes smaller than the uncompensated circuit.

One has to note, that it is very sensitive to the parametrization of the filter.

## 5 Maximum Power Point Tracker

### 5.1 Perturb and Observe

A Maximum Power Point Tracker (MPPT) is designed to continuously adjust the reference voltage of the PV system to the optimal operating point for maximum power extraction under varying irradiance conditions. The Perturb and Observe algorithm operates as shown in Figure 27.

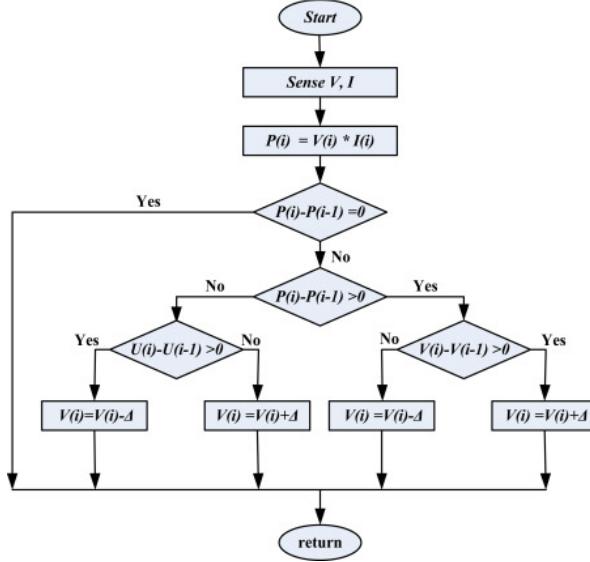


Figure 27: Perturb-and-Observe Technique[6]

### 5.2 MPPT Implementation

To implement this algorithm, the discrete states must first be initialized. These states include voltage, current, and power from the simulation, as well as the previous reference voltage. Additionally, the limits for the reference voltage are defined in the following code:

---

```

#define PREV_Voltage DiscState(0)
#define PREV_Current DiscState(1)
#define PREV_Power DiscState(2)
#define PREV_Vref DiscState(3)
#define VREF_MIN 0.0
#define VREF_MAX 740.0

```

---

Next, the initial reference voltage is set. In order to reduce ringing the start voltage is set to 0 V.

---

```
PREV_Vref = 0;
```

---

In the calculation, the algorithm compares the previous voltage and power values with the current ones. Based on this comparison, the reference voltage is adjusted and the output is updated. It is important to check whether a major timestep has occurred to ensure that all states are correctly updated.

---

```

if (IsMajorStep)
{
    double dP = Input(0) * Input(1) - PREV_Power;
    double dV = Input(0) - PREV_Voltage;
    double VSTEP = 2;
    double Vref = PREV_Vref;

    if (dP > 0) {
        if (dV > 0)
            Vref += VSTEP;
        else
            Vref -= VSTEP;
    } else {
        if (dV > 0)
            Vref -= VSTEP;
        else
            Vref += VSTEP;
    }

    if (Vref > VREF_MAX) Vref = VREF_MAX;
    if (Vref < VREF_MIN) Vref = VREF_MIN;

    Output(0) = Vref;
}

```

---

After the calculation, the states are updated manually:

---

```

PREV_Voltage = Input(0);
PREV_Current = Input(1);
PREV_Vref   = Output(0);
PREV_Power  = PREV_Voltage * PREV_Current;

```

---

### 5.3 Sampling time of the MPPT algorithm

As the voltage control operates at a frequency of 700 Hz, the MPPT algorithm must run more slowly to allow the system sufficient time to react. If the MPPT were to run faster, the system would never reach the reference voltage before a new one is applied. Therefore, we choose a sample time of 3 ms, which is half the rate of the voltage controller. In Figure 28, we can see the measured voltage compared to the reference voltage. With a sample time of 3 ms for the MPPT, we ensure that the system has enough time to settle before a new reference voltage is set.

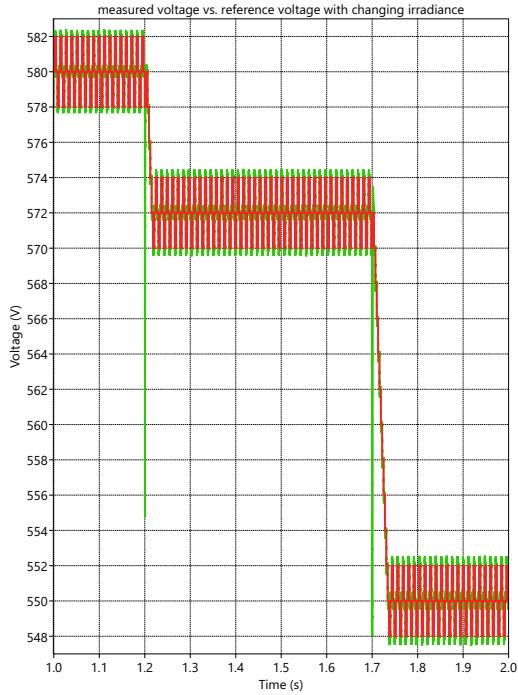


Figure 28: Measured Voltage vs. Reference Voltage

#### 5.4 Transients and Steady-State Changes

During operation, changes in irradiance and temperature can occur, requiring the MPPT algorithm to react accordingly. Therefore, selecting an appropriate voltage step size is crucial.

In Figure 29, a step size of 1 V is used for the reference voltage adjustment. During transient changes, the algorithm takes longer to reach the final reference voltage. Despite this slower response, the advantage is a highly precise adjustment with only minimal ripple. To mitigate the slower response, a good initial value such as 500 V should be chosen.

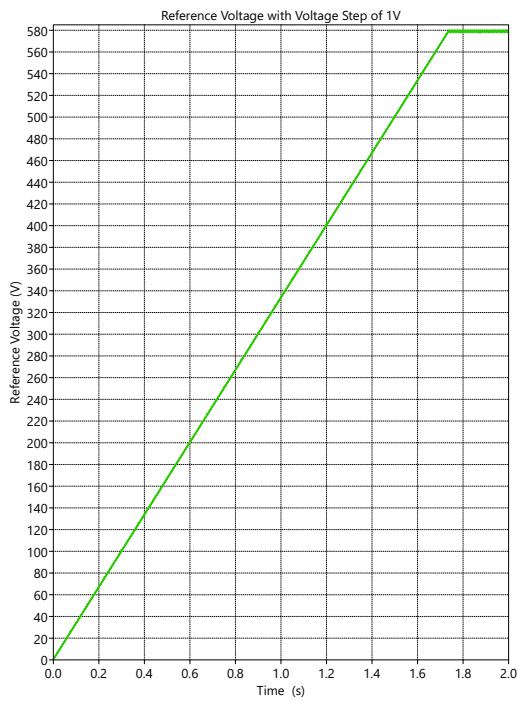


Figure 29: Reference Voltage with Voltage Step of 1V

Alternatively, a larger step size such as 10 V can be used, which results in much faster convergence to the correct reference voltage, as shown in Figure 30. However, this comes with the disadvantage of significantly higher voltage ripple.

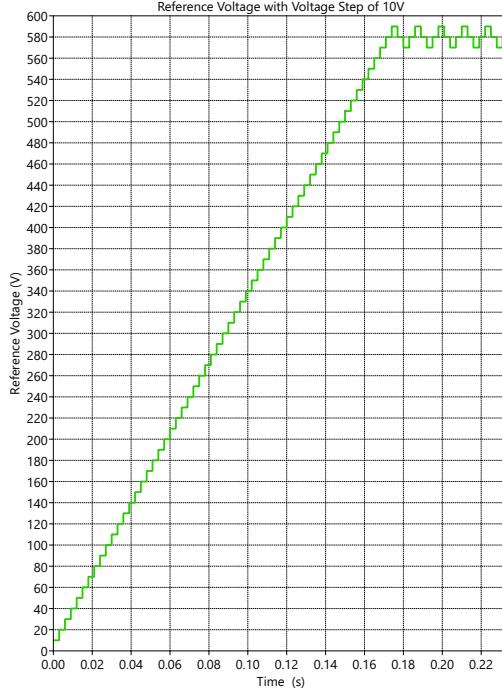


Figure 30: Reference Voltage with Voltage Step of 10V

In comparison, a smaller step size of 2 V is selected to ensure good precision while still providing sufficiently fast behavior. The initial idea of using an initial value of 500 V is not used, as it leads to significant ringing in the current controller. Since the PV system is relatively slow, rise times of approximately 0.9 s are acceptable.

## 5.5 Behavior for changing Irradiances

Finally, the dynamic behavior under changing irradiance conditions is examined. To test this, the irradiance is varied twice within one second, as shown in Figure 31. The MPPT reacts quickly to the changes and promptly approaches the new reference voltage. Overall, the algorithm is validated.

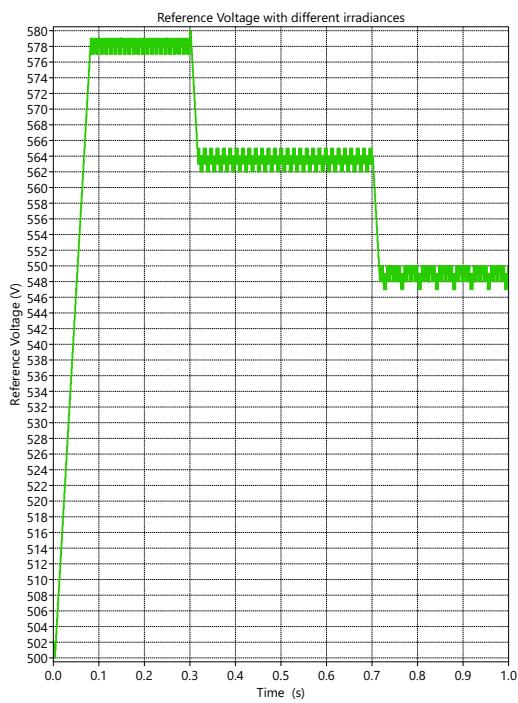


Figure 31: Reference Voltage with changing irradiance

## 6 Conclusion

In this project, a complete boost converter stage for a PV application was designed, modeled, and validated through simulation. The system was designed to interface a PV array consisting of two parallel strings of 22 Kyocera KC200GT modules with a grid-connected inverter.

The key technical achievements of this work include:

- **PV Characterization:** Detailed analysis of the KC200GT modules confirmed the non-linear dependency of the Maximum Power Point (MPP) on irradiance and temperature. These findings informed the voltage and current limits required for the power stage design.
- **Hardware Design:** A boost converter was dimensioned with a 0.4137 mH inductor and a 50  $\mu\text{F}$  input capacitor to maintain strict ripple requirements. A 750 V DC-link voltage was selected to ensure sufficient headroom for subsequent three-phase inverter structure was successfully implemented. By utilizing a linearized small-signal model, an inner current loop ( $f_{c,i} = 7 \text{ kHz}$ ) and an outer voltage loop ( $f_{c,v} = 700 \text{ Hz}$ ) were tuned to provide high stability and adequate disturbance rejection.
- **MPPT Performance:** The Perturb and Observe (P&O) algorithm was implemented and optimized. Using a sampling time of 3 ms and a step size of 2 V, the tracker demonstrated excellent efficiency and stability, even under rapidly changing irradiance conditions.
- **Optimization:** Voluntary improvements, such as the implementation of a moving average filter and the alignment of the current loop zero-frequency with the LC resonance, further enhanced the robustness of the system against high-frequency switching noise.

Overall, the project successfully demonstrates the integration of hardware dimensioning, control theory, and algorithmic optimization required for modern distributed energy systems. The simulation results confirm that the system is capable of high-performance energy harvesting while maintaining electrical stability across a wide range of operating points.

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