

CPU BYTE	DMA/USB/LCD			
ADDRESS <sup>(A)</sup>	BYTE ADDRESS <sup>(A)</sup>	MEMORY BLOCKS		BLOCK SIZE
000000h	0001 0000h	MMR (Reserved) <sup>(B)</sup>		64K Minus 192 Bytes
0000C0h	0001 00C0h	DARAM <sup>(D)</sup>		
010000h	0009 0000h	SARAM		256K Bytes
050000h	0100 0000h	External-CS0 Space <sup>(C)(E)</sup>		8M Minus 320K Bytes SDRAM/mSDRAM
800000h	0200 0000h	External-CS2 Space <sup>(C)</sup>		4M Bytes Asynchronous
C00000h	0300 0000h	External-CS3 Space <sup>(C)</sup>		2M Bytes Asynchronous
E00000h	0400 0000h	External-CS4 Space <sup>(C)</sup>		1M Bytes Asynchronous
F00000h	0500 0000h	External-CS5 Space <sup>(C)</sup>		1M Minus 128K Bytes Asynchronous
FE0000h	050E 0000h	ROM (if MPNMC=0)	Reserved (if MPNMC=1)	Unmapped (if MPNMC=1) 128K Bytes ROM (if MPNMC=0)
FFFFFFh	050F FFFFh			

- A. Address shown represents the first byte address in each block.
- B. The first 192 bytes are reserved for memory-mapped registers (MMRs).
- C. Reading/Writing to/from unmapped returns zeros.
- D. The USB and LCD controllers do not have access to DARAM.
- E. The CS0 space can be accessed by CS0 *only* or by CS0 *and* CS1.