

October 1987 Revised January 1999

### CD4093BC

# **Quad 2-Input NAND Schmitt Trigger**

#### **General Description**

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive  $(V_T^+)$  and the negative voltage  $(V_T^-)$  is defined as hysteresis voltage  $(V_H)$ .

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

#### **Features**

- Wide supply voltage range: 3.0V to 15V
- Schmitt-trigger on each input with no external components
- Noise immunity greater than 50%

- Equal source and sink currents
- No limit on input rise and fall time
- Standard B-series output drive
- Hysteresis voltage (any input)  $T_A = 25^{\circ}C$

Typical	$V_{DD} = 5.0V$	$V_{H} = 1.5V$
	$V_{DD} = 10V$	$V_H = 2.2V$
	$V_{DD} = 15V$	$V_H = 2.7V$
Guaranteed		$V_{H} = 0.1 \ V_{DD}$

#### **Applications**

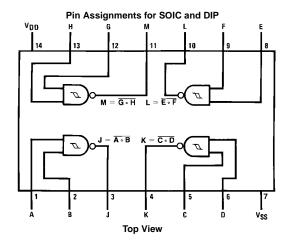
- · Wave and pulse shapers
- · High-noise-environment systems
- Monostable multivibrators
- · Astable multivibrators
- NAND logic

#### **Ordering Code:**

Order Number	Package Number	Package Description
CD4093BCM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
CD4093BCN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Connection Diagram**



#### Absolute Maximum Ratings(Note 1)

(Note 2)

-0.5 to +18 V<sub>DC</sub>

 $\label{eq:local_problem} \begin{array}{ll} \mbox{Input Voltage (V_{IN})} & -0.5 \mbox{ to V}_{DD} \mbox{ +0.5 V}_{DC} \\ \mbox{Storage Temperature Range (T_S)} & -65^{\circ}\mbox{C to +150}^{\circ}\mbox{C} \end{array}$ 

Power Dissipation (P<sub>D</sub>)

Dual-In-Line 700 mW Small Outline 500 mW

Lead Temperature (T<sub>L</sub>)

DC Supply Voltage (V<sub>DD</sub>)

(Soldering, 10 seconds) 260°C

# Recommended Operating Conditions (Note 2)

DC Supply Voltage (V<sub>DD</sub>)  $3 \text{ to 15 V}_{DC}$  Input Voltage (V<sub>IN</sub>)  $0 \text{ to V}_{DD} \text{ V}_{DC}$ 

Operating Temperature Range ( $T_A$ )  $-40^{\circ}C$  to  $+85^{\circ}C$ 

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2:  $V_{SS} = 0V$  unless otherwise specified.

#### DC Electrical Characteristics (Note 2)

Symbol	Parameter	0 1111	-40	-40°C		+25°C			+85°C	
		Conditions	Min	Max	Min	Тур	Max	Min	Max	Units
I <sub>DD</sub>	Quiescent Device	$V_{DD} = 5V$		1.0			1.0		7.5	μА
	Current	$V_{DD} = 10V$		2.0			2.0		15.0	μΑ
		$V_{DD} = 15V$		4.0			4.0		30.0	μΑ
V <sub>OL</sub>	LOW Level	$V_{IN} = V_{DD,}  I_O  < 1 \mu A$								
	Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V <sub>OH</sub>	HIGH Level	$V_{IN} = V_{SS},  I_O  < 1 \mu A$								
	Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		V <sub>DD</sub> = 15V	14.95		14.95	15		14.95		V
V <sub>T</sub> -	Negative-Going Threshold	I <sub>O</sub>   < 1 μA								
	Voltage (Any Input)	$V_{DD} = 5V, V_{O} = 4.5V$	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		$V_{DD} = 10V, V_{O} = 9V$	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		$V_{DD} = 15V, V_{O} = 13.5V$	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V <sub>T</sub> +	Positive-Going Threshold	I <sub>O</sub>   < 1 μA								
	Voltage (Any Input)	$V_{DD} = 5V, V_{O} = 0.5V$	2.75	3.6	2.75	3.3	3.5	2.65	3.5	V
		$V_{DD} = 10V, V_{O} = 1V$	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		$V_{DD} = 15V, V_{O} = 1.5V$	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V <sub>H</sub>	Hysteresis (V <sub>T</sub> + – V <sub>T</sub> –)	$V_{DD} = 5V$	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	$V_{DD} = 10V$	1.0	4.3	1.0	2.2	4.0	0.70	4.0	V
		$V_{DD} = 15V$	1.5	6.3	1.5	2.7	6.0	1.20	6.0	V
l <sub>OL</sub>	LOW Level Output	$V_{IN} = V_{DD}$								
	Current (Note 3)	$V_{DD} = 5V, V_{O} = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_{O} = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_{O} = 1.5V$	3.6		3.0	8.8		2.4		mA
l <sub>OH</sub>	HIGH Level Output	$V_{IN} = V_{SS}$								
	Current (Note 3)	$V_{DD} = 5V, V_{O} = 4.6V$	-0.52		0.44	-0.88		-0.36		mA
		$V_{DD} = 10V, V_{O} = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
		$V_{DD} = 15V, V_{O} = 13.5V$	-3.6		-3.0	-8.8		-2.4		mA
I <sub>IN</sub>	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.3		-10 <sup>-5</sup>	-0.3		-1.0	μА
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10 <sup>-5</sup>	0.3		1.0	μΑ

Note 3:  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

#### AC Electrical Characteristics (Note 4)

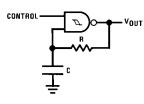
 $\rm T_A = 25^{\circ}C,\, C_L = 50$  pF,  $\rm R_L = 200k,\, Input\, t_f,\, t_f = 20$  ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Тур	Max	Units
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time	$V_{DD} = 5V$		300	450	ns
		$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		120	210	ns
		V <sub>DD</sub> = 15V		80	160	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time	$V_{DD} = 5V$		90	145	ns
		$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$		50	75	ns
		V <sub>DD</sub> = 15V		40	60	ns
C <sub>IN</sub>	Input Capacitance	(Any Input)		5.0	7.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance	(Per Gate)		24		pF

Note 4: AC Parameters are guaranteed by DC correlated testing.

# **Typical Applications**

#### **Gated Oscillator**



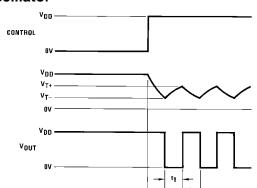
Assume  $t_1 + t_2 >> t_{PHL} + t_{PLH}$  then:

 $t_0 = RC \ \ell n \ [V_{DD}/V_T -]$ 

 $t_1 = RC \ \ell n \ [(V_{DD} - V_{T} \!\!\!-) \! / \! (V_{DD} - V_{T} \!\!\!\!+)]$ 

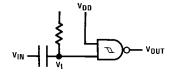
 $t_2 = RC \ \ell n \ [V_T^{+/V}T^{-]}$ 

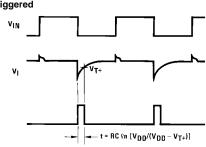
$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC \ln \frac{(V_T^+)(V_{DD} - V_T^-)}{(V_T^-)(V_{DD} - V_T^+)}}$$



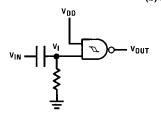
#### **Gated One-Shot**

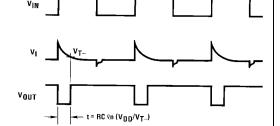
#### (a) Negative-Edge Triggered



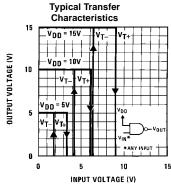


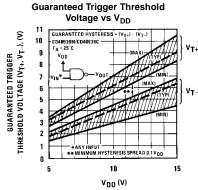
#### (b) Positive-Edge Triggered

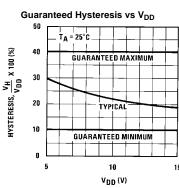


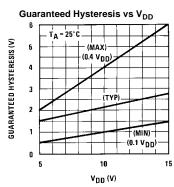


#### **Typical Performance Characteristics**

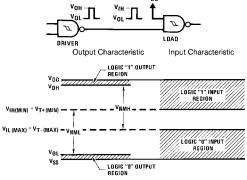






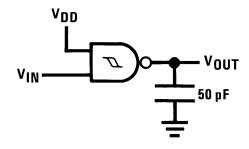


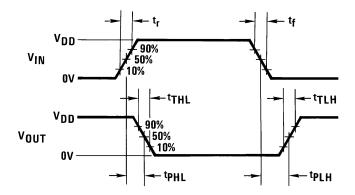
#### **Input and Output Characteristics**



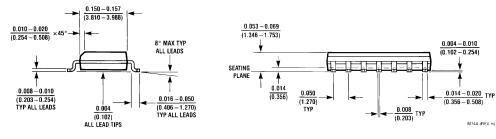
$$\begin{split} &V_{NML} = V_{IH(MIN)} - V_{OL} \cong V_{IH(MIN)} = V_{T} +_{(MIN)} \\ &V_{NMH} = V_{OH} - V_{IL(MAX)} \cong V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T} -_{(MAX)} \end{split}$$

# **AC Test Circuits and Switching Time Waveforms**



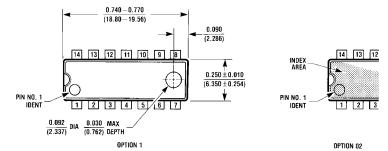


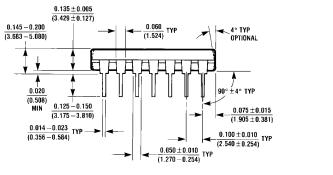
# 

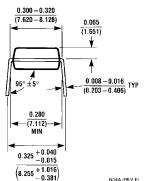


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body Package Number M14A

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com