Senior Design
ENG EC 463

To: Professor Pisano

From: Smart Grid ECE Senior Design Team

Team: Power Pooches: Team 14

Date: 11/21/2014

Subject: First Deliverable Test Report

1.0 Project Objective

1.1 The overall objective of this Smart Grid Test Facility project is to make an educational tool for engineering students, allowing them to test circuitry (such as loads and generators) on a small-scale emulation of the power grid.

1.2 This test facility will also allow for integration of Smart Grid components into the grid, in addition to clean energy generation stations.

2.0 Test Objective and Significance

2.1 The test setup is presented in Figure 1. The test procedure will focus on the Data Acquisition (DAQ), transmission lines, and variable load circuit. A signal generator will supply power to a transmission line, which passes the power onto the resistive load. Meanwhile, the DAQ measures the AC sine wave at various points along the circuit. Although this setup is implemented in a simple form, this test will confirm whether our basic arrangement is successful and prove the concepts that will be employed in the final design.

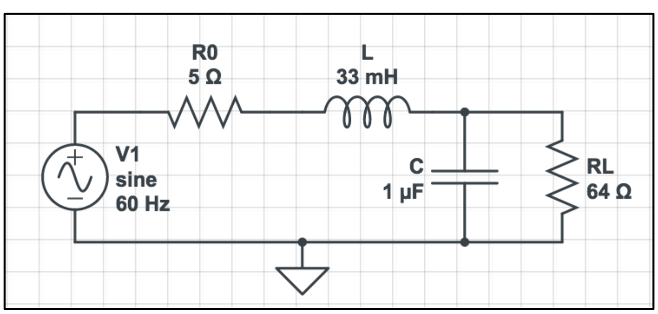

Figure 1: Testing Circuit

2.2 This deliverable is essential because it validates the fundamental engineering design of the grid test facility. The final circuit will be far more complex than that seen in Figure 1, but the roots will remain unchanged, with an overall system of generation to transmission to load, with DAQ scoping various points along the network.

2.3 **Transmission Lines**

2.3.1 The transmission lines were designed to model real-grid transmission lines based on RLC characteristics. Testing the transmission lines is significant because we will be able to confirm that the expected voltage drop across the lines is comparable to what actually occurs on the grid.

2.4 **Load Circuit**

2.4.1 Testing the variable resistive load is important because we need to observe how the voltage and current behave in the presence of various loads. We also must ensure that the resistive load circuit is performing properly without skewing results.

2.5 **Data Acquisition (DAQ)**

2.5.1 The DAQ testing is important because it serves as the first step toward programming the DAQ to perform more involved computations. At this point, we are simply testing whether we can read the waveform at various points throughout the test bench. Later, we will build upon this initial testing to provide information such as power factor and phase delay.

3.0 Equipment and Setup

3.1 **Overall Arrangement**

3.1.1 The test circuit is presented in Figure 1; the overall structure remained unchanged throughout the testing, but the values for R0, L, C, and RL changed in order to test various components. Figure 1 showcases values fit for the 30-mile transmission line by its RLC values. The load was tested at 64 Ω in this circuit as well. As visible in Tables 1 and 2 (refer to *Measurements and Data*), multiple arrangements were set up in order to test two separate transmission lines in addition to multiple resistive loads. Figures 2 and 3 demonstrate images from our testing procedure.

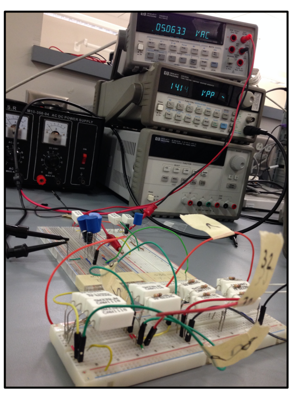

Figure 2

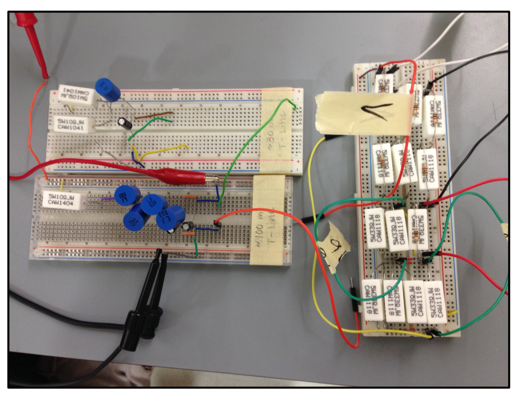

Figure 3

3.2 **Transmission Lines**

3.2.1 To test the transmission lines, a test signal was sent through the lines with an attached load. Comparing the measured output voltage to the calculated output voltage an error calculation was made. The transmission lines that we have designed model real-grid transmission lines by their resistive, inductive, and capacitive (RLC) characteristics per unit length in miles. The voltage drop that is seen from the source (generator) to load indicates the validity of our designs and whether we have successfully created standard transmission lines.

3.3 **Load Circuit**

3.3.1 The variable load will be tested in parallel with the transmission lines. Since the output voltage drop depends on the load, the value of the load is built into the calculation for change in voltage.

3.4 **Data Acquisition (DAQ)**

3.4.1 The DAQ was selected because it has a high number of analog inputs for measuring many points along the grid network. Moreover, it can be programmed in MATLAB. This is ideal for studying various components of the test facility, and MATLAB is easily understandable for undergraduate engineering students. The DAQ testing occurs by simply measuring the voltage output of an interface circuit connected to a waveform generator, and showing the result on a computer.

3.4.2 The DAQ shares common a ground, and is to be used to probe points throughout the test bench. For testing the DAQ without the interface circuit the waveform generator should be set for an output of 60 Hz 0-2.4V (thus, 1.2V DC offset, $2.4V_{pp}$). For testing the transmission lines and DAQ along with the interface circuit (transfer: $V_{OUT} = (V_{IN} + 12V) / 10$), no DC offset is needed and various voltages between -12V and 12V (interface output: 0V to 2.4V) may be used in order to test. However, for our test, the waveform generator is operating at 60 Hz, 12 V_{PP}. This combined with the transfer of the interface should result in readings between 0.6V and 1.8V. This interface circuit is shown in Figure 4.

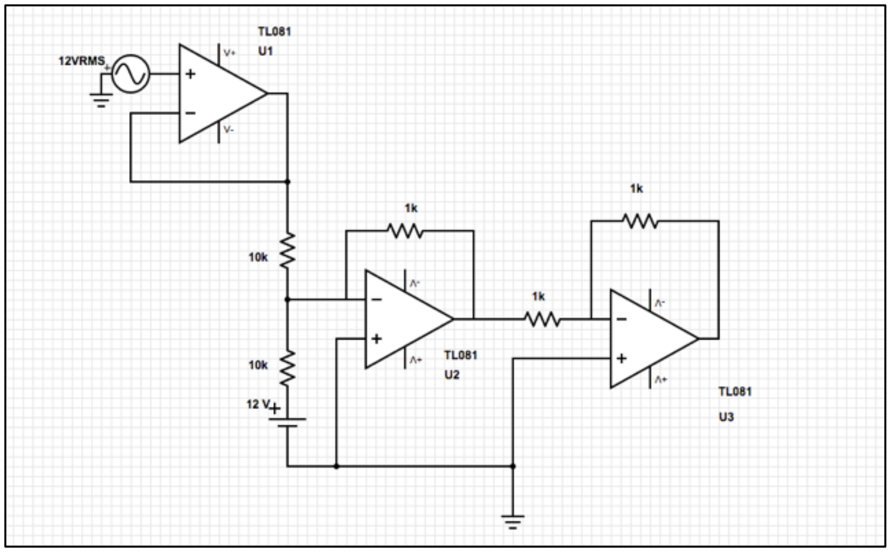

Figure 4: Op-Amp Interfacing Circuit For Measuring Test Voltages with DAQ

4.0 Measurements and Data

4.1 **Transmission Lines and Load Circuit**

4.1.1 For testing transmission lines (and thus the variable load), data was collected using a multimeter to measure AC voltage. Table 1 below shows the variety of arrangements used to test the transmission lines. The voltmeter reads the voltage across the resistive load.

Table 1: Transmission Line Testing

TL Characteristics				Setup					
TL Length	R (Ω)	L (mH)	C (μF)	Load (Ω)	Re(Z)	Im(Z)	Total Impedance (Ω)	Input Voltage (V)	Input Frequency (Hz)
30	5	33	1	64	68.99909039	12.416872	70.10744029	6.636	60
30	5	33	1	192	196.9972712	12.36861601	197.3851755	6.636	60
100	10	130	2	64	73.9963617	48.96174403	88.72831523	6.636	60
100	10	130	2	192	201.9890851	48.86523208	207.8157872	6.636	60

4.2 **Data Acquisition (DAQ)**

4.2.1 For testing the DAQ, the ground of the DAQ should be connected to the ground of the circuit (See Figure 1). Then, the DAQ port FIO0 should probe the output of the grid interface circuit connected to the testing circuit. This can be done by simply connecting the interface to a part of the circuit, connecting the red lead (FIO0) to the interface output, running the DAQ script, and observing the MATLAB output.

5.0 Conclusions

5.1 **Transmission Lines**

5.1.1 For the transmission lines, success is measured in terms of the percent error between expected output voltage and measured output voltage. Data from a test is provided in Table 2.

Table 2: Transmission Line Testing

TL Characteristics				Setup						Output Voltage		
TL Length	R (Ω)	L (mH)	C (μF)	Load (Ω)	Re(Z)	Im(Z)	Total Impedance (Ω)	Input Voltage (V)	Input Frequency (Hz)	Calculated (V)	Measured (V)	% Error
30	5	33	1	64	68.9990904	12.416872	70.10744029	7.0710678	60	5.8462621	2.4	-58.9481
30	5	33	1	128	132.998181	12.392744	133.5743096	7.0710678	60	6.4005977	3.59	-43.9115
100	10	130	2	64	73.9963617	48.961744	88.72831523	5	60	2.8065298	1.22	-56.5299
100	10	130	2	128	137.992723	48.9134881	146.4053313	5	60	3.5951055	1.96	-45.4814
100	10	130	2	300	309.982945	48.7838001	313.7981607	5	60	4.2854717	3.03	-29.296
100	10	130	2	600	609.965891	48.5576003	611.8956028	5	60	4.6152439	3.79	-17.8808
100	10	130	2	850	859.951679	48.3691004	861.3108962	5	60	4.7221183	4.09	-13.3863
100	10	130	2	1000	1009.94315	48.2560004	1011.095352	5	60	4.7618149	4.2	-11.7983
100	10	130	2	10000	10009.4315	41.4700043	10009.51742	5	60	4.9751146	4.96	-0.3038

5.1.2 The errors seen in Table 2 are a result of several conditions. First, the waveform generator has an internal resistance of 50 Ω, which introduces a new element that was not part of the calculations for expected output voltage. For such small loads that we connect to the generator, the impacts of this resistance become clear. As we increase the load resistance, it is clear that this problem is reduced. Additionally, the breadboard of the load circuit has a small internal resistance that was also not accounted for in the output voltage calculation (although this value is negligible relative to the remainder of the circuit).

5.2 **Load Circuit**

5.2.1 The loads under test were considered successful if they could be connected together with the transmission lines and offer an easily modifiable resistance. The circuit diagram in Figure 5 shows the binary load circuit that was provided at the time of testing.

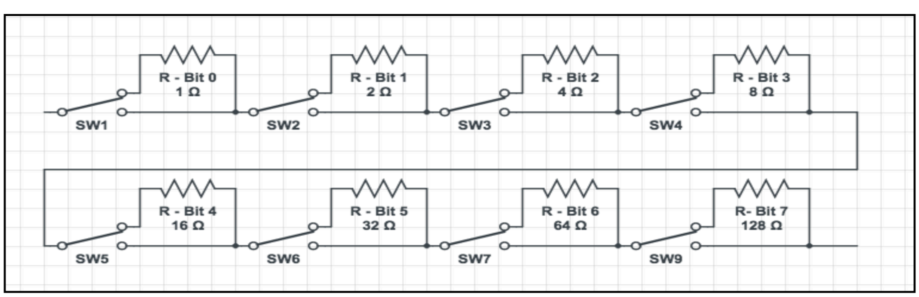

Figure 5: Resistive Load Circuit

As a binary load, each resistance value corresponds to a value 2^n where n is the bit order. Flipping any of the switches results in the corresponding resistor being shorted, changing the total resistance of the variable load.

5.3 **Data Acquisition**

5.3.1 The criteria for success for the DAQ is a continuous signal readout within 0.6V and 1.8V from the LabJack. Noisy signals will require filtering that is currently unavailable and therefore must be re-read. Since the objective for the DAQ testing is to confirm that it can read AC signals at points along the circuit, the test is deemed successful if readings are visible and sensible; this means that the collected data matches with the known input values. As more complex functionality is built into the DAQ, testing will be more quantitative, including measurements such as phase angle and power factor.

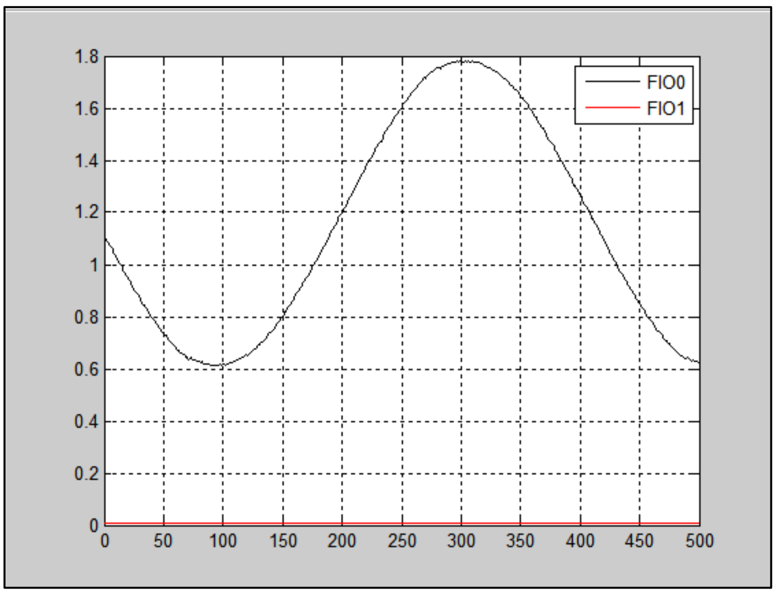

Figure 6: DAQ Reading of Interface Output for 60Hz, $12V_{pp}$ signal

Key Data:

V_{min} = .6121 Volts V_{max} = 1.7883 Volts

$V_{min,location}$ = 94 time units $V_{max,location}$ = 303 time units

Confirming 60 Hz input using waveform:

f_{sample} = 25 kHz → 1 time unit = 1/(25 kHz)

Δt = (303 time units – 94 time units) * (1/25 kHz) ≈ .0084 seconds

(1/(Δt*2)) = frequency of waveform = 59.8086 Hz ≈ 60 Hz

5.4 **Summary and Future Plans**

5.4.1 From the measurements and data obtained on prior to and on test day, it can be concluded that the initial design of the tested components are successful. The next step will be to reach the desired complexity of the transmission lines, DAQ, and generic loads, such as using PCBs in implementation and achieving tighter tolerance for error. The power generation aspect of the project, as well as possible integration of renewable source emulators, will be demonstrated in the upcoming design review.