DSD Final Exam January 12, 2011

1. (Reverse Engineering) What is the counter state diagram implied by the figure below? There are two inputs to this counter. A is asserted to enable counting.

D is used to change count direction, that is, go through the sequence in reverse order. (15%)

N1

S0

S1

N0

D

C

Q

Q

C

D

B

A

1. (FSM design and optimization) Consider a 4-bit sequence-detecting finite state machine. The machine has a single input X and output Z. The output is asserted after each 4-bit input sequence if it consists of one of the binary strings 0110 or 1010. The machine returns to the reset state after each and every 4-bit sequence.
2. Create a “state diagram” for this 4-bit sequence detector. (5%)
3. Use “ Implication Chart Method ” to reduce the number of states. (5%)
4. Use the RS Flip-flops to design the machine. (10%)
5. You have learned 4 types of **flip-flop**, D, R-S, J-K and T this semester.
   1. Please implement one type of flip-flops (RS) using basic logic gates and state their truth table. (You can use AND, OR, NOT, NOR, NAND, XOR and XNOR) (10%)
   2. Please design a four bit simple ring counter using T flip-flop. (5%)
   3. Please design a four bit Johnson counter using R-S flip-flop. (5%)
6. Please design a counter which can count from 0 to 15 and display on a seven-segment LED display. (You can use all kinds of logic gates and flip-flop) (15%)

 

1. Configurations for 16 hexadecimal digits
2. names of segments
3. (10%) When you were doing your final program project (Reverse engineering, or Forward Design), what is your project? What is your role in your project?

What is the most difficult part in your role and please describe it, then how you have solved your problem?

1. (20%) Semi-conductor theory. We say that TSMC has the industry leading 40nm semiconductor process technology

(a) (10%) When the poly-silicon and diffusion layer width is reduced by a factor of R, so are others. That is, the source-drain voltage, the width, the length, oxide thickness (T0) all scaled by R

Please answer what is the Packing density (gates/area)? Power/gate, gate delay (speed) in terms of R. Explain with simple explanations using the simple circuit theory (For instance, resistance, capacitance, and speed), and make your own assumptions.

(b) (5%) What is Moors’ Law? If hardware chips can follow Moors’ Law, can software programming productivity follow it? Why and why not? How to match the speed of Moors’ Law in modern digital system design? (Hint: software design vs. hardware design).

(c) (5%)Current research shows that Moors’ Law may reach its limit in 10 years for CMOS technology. The solution may go to multiple CPU/GPUs in one chip. What are the impacts for the students who majored in computer science?