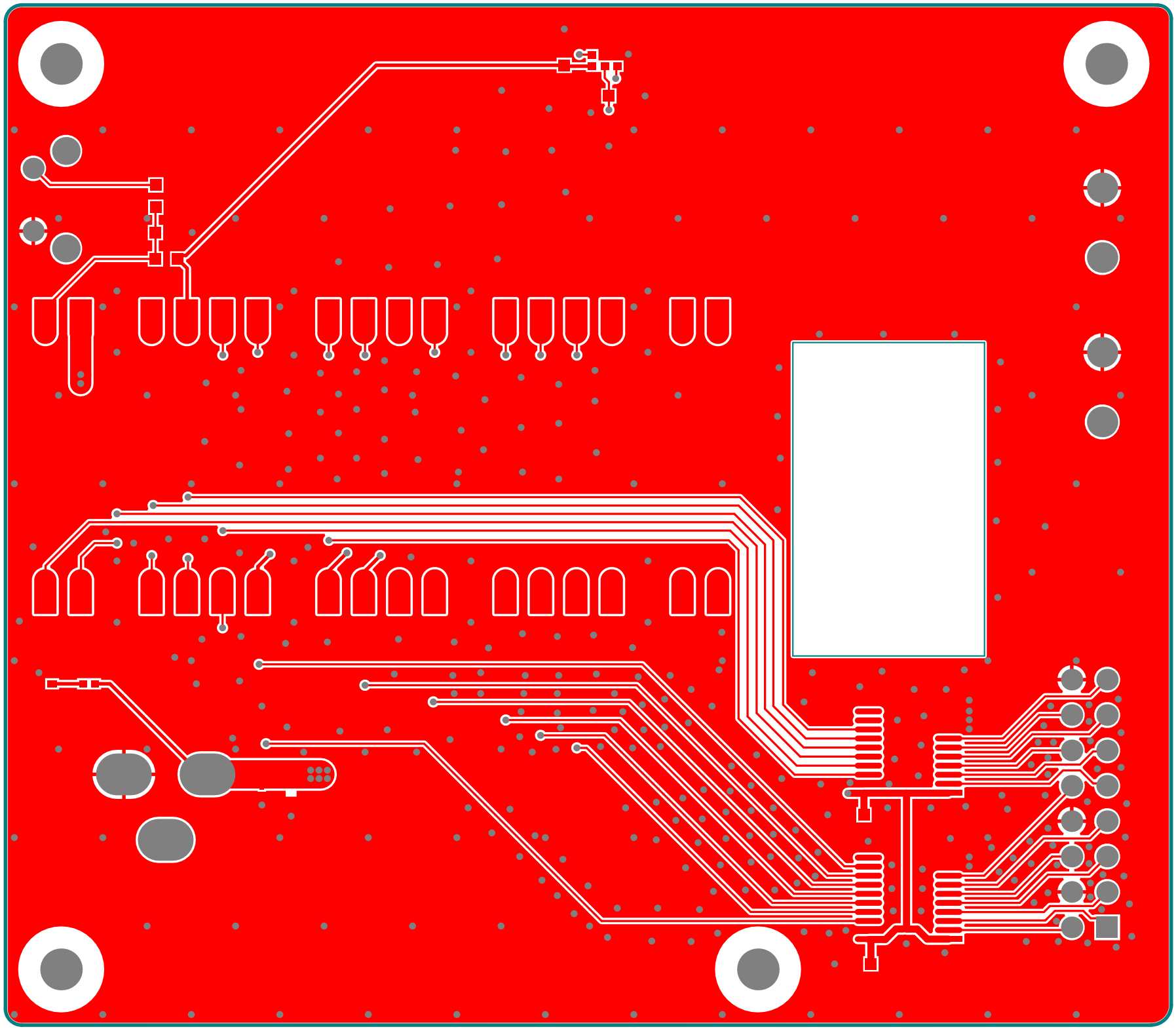
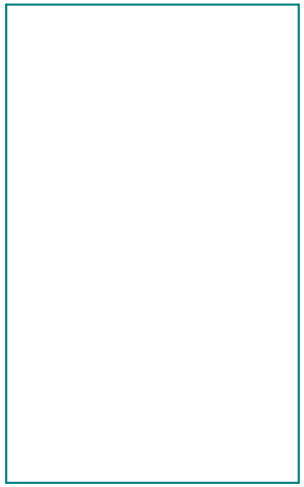
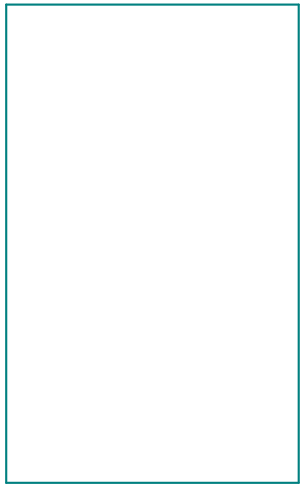
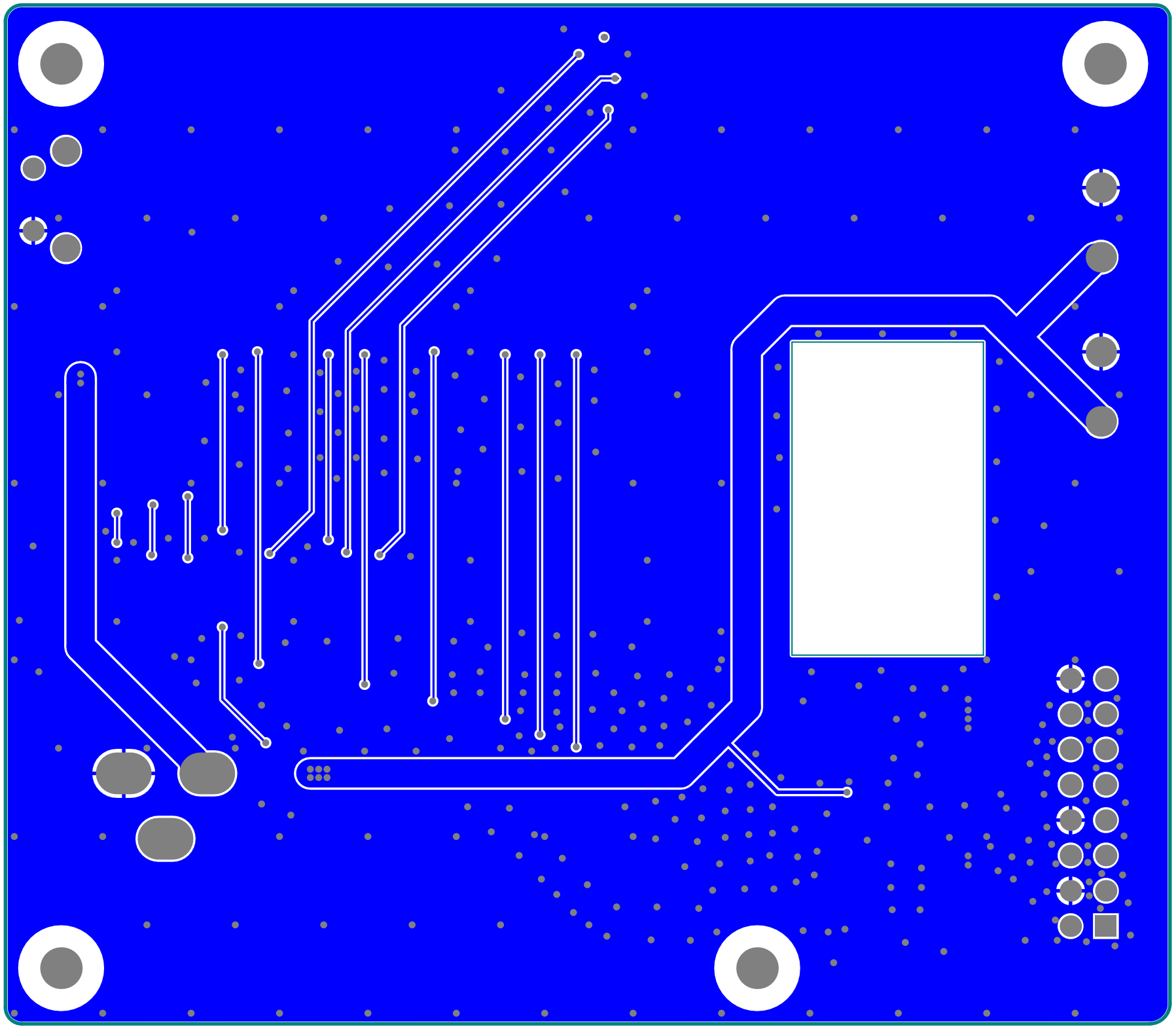
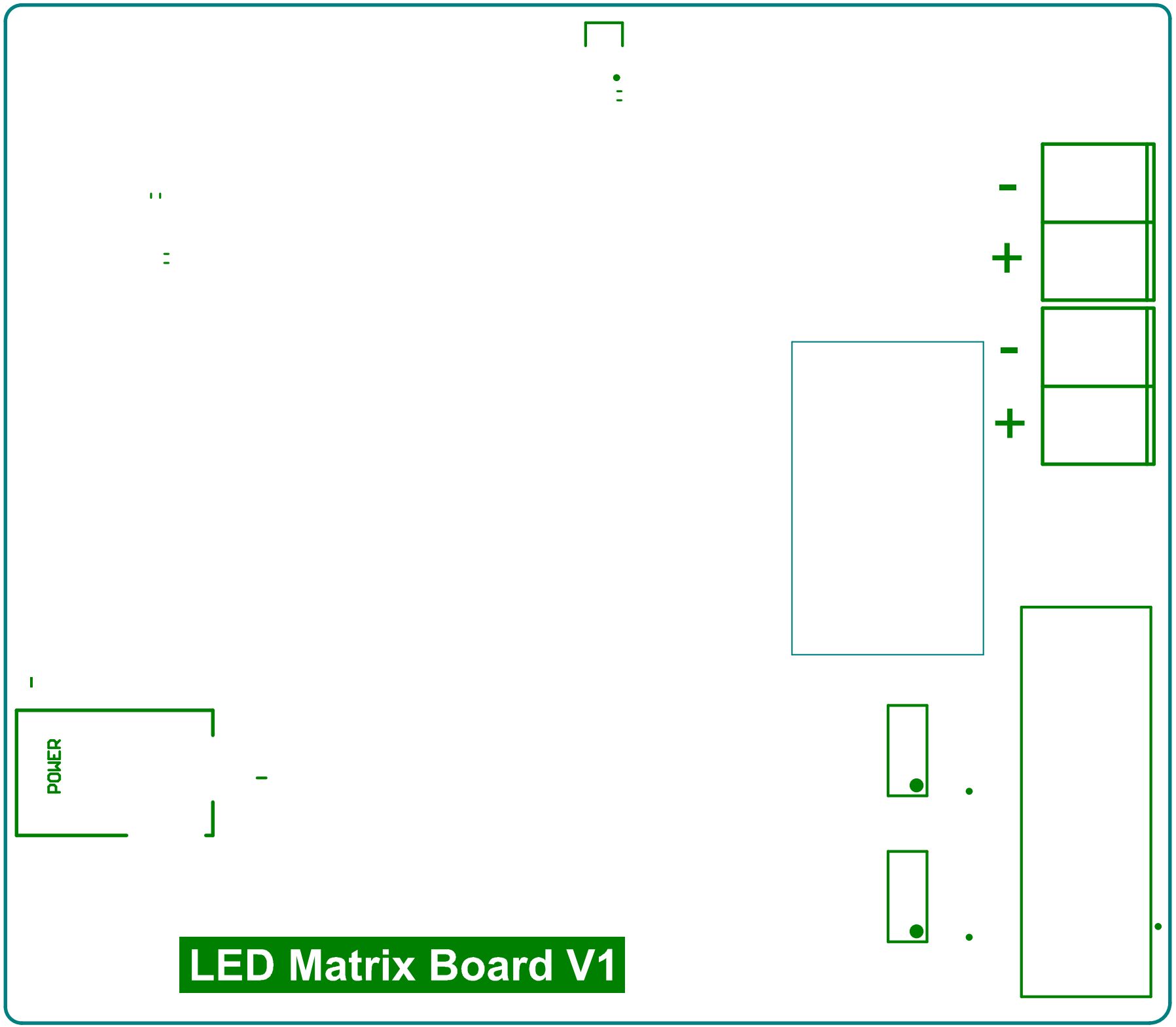
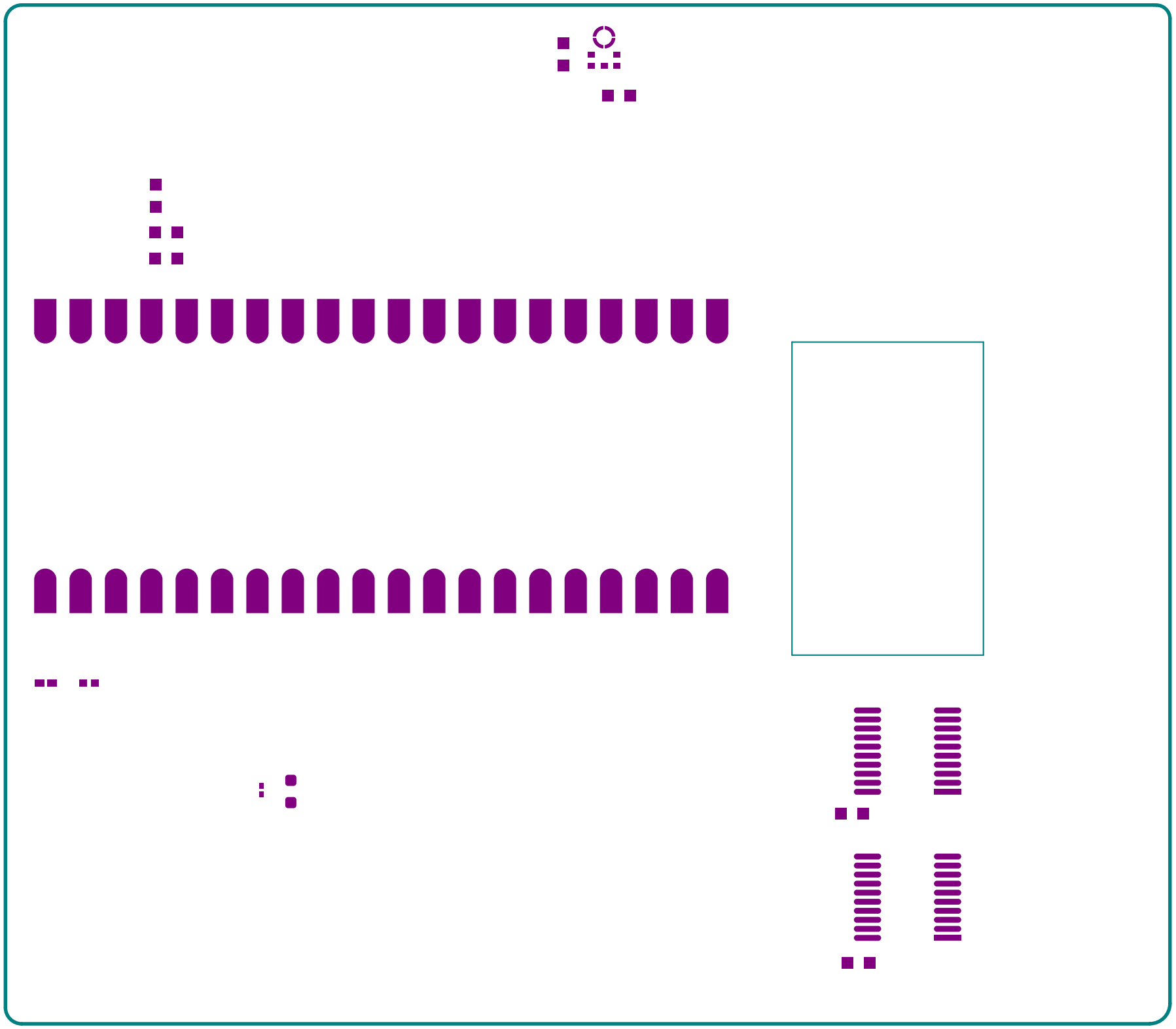


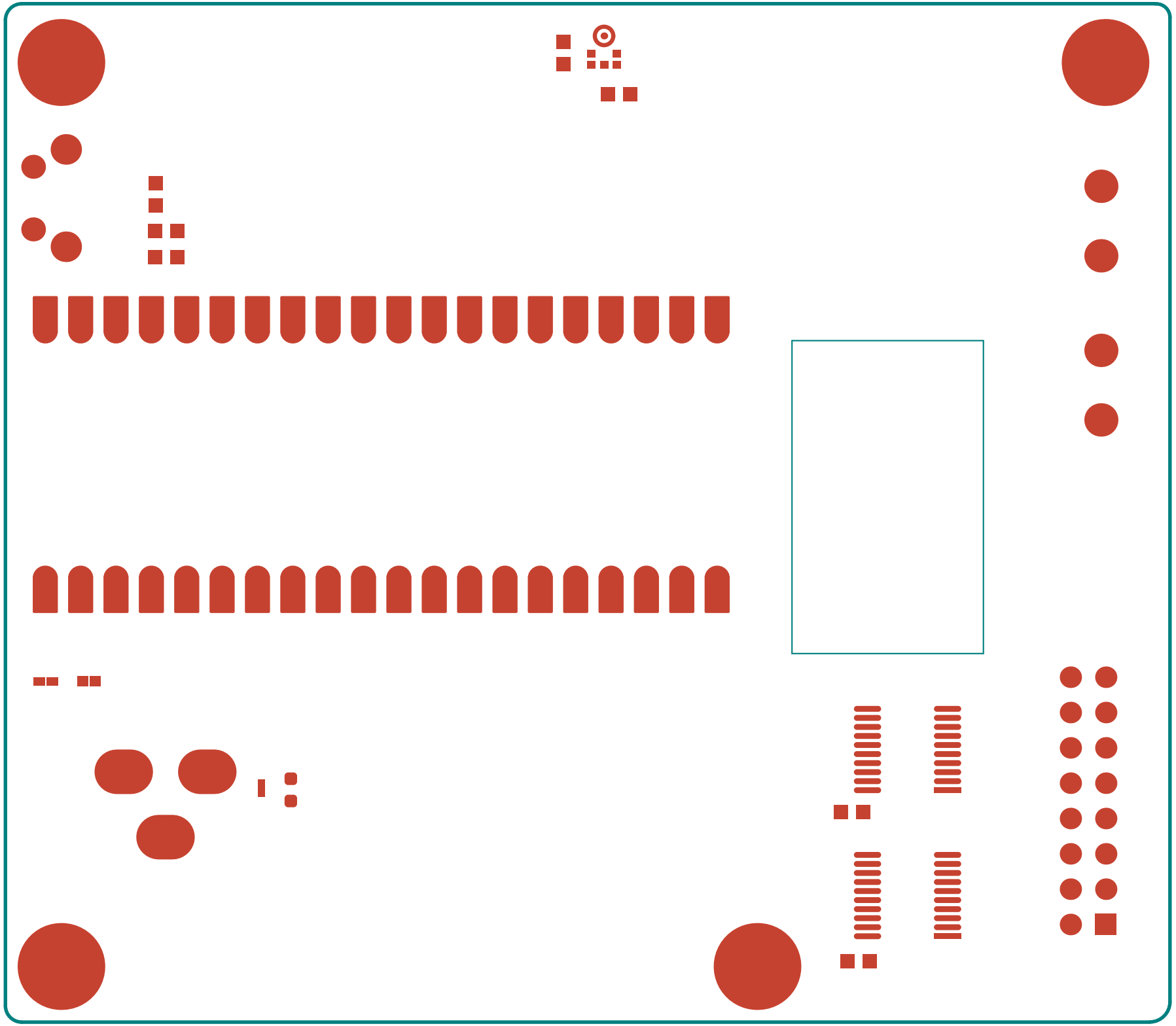


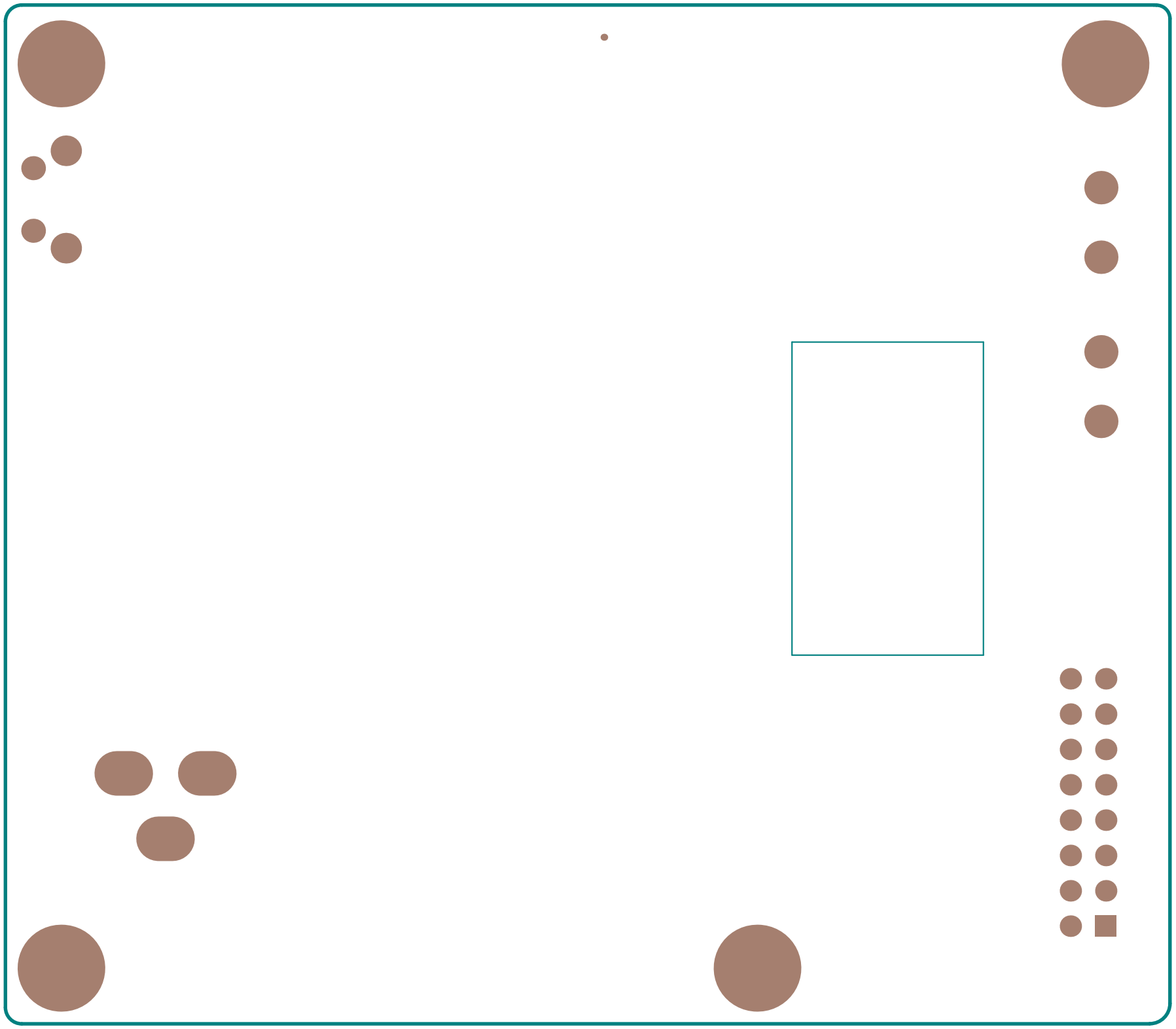


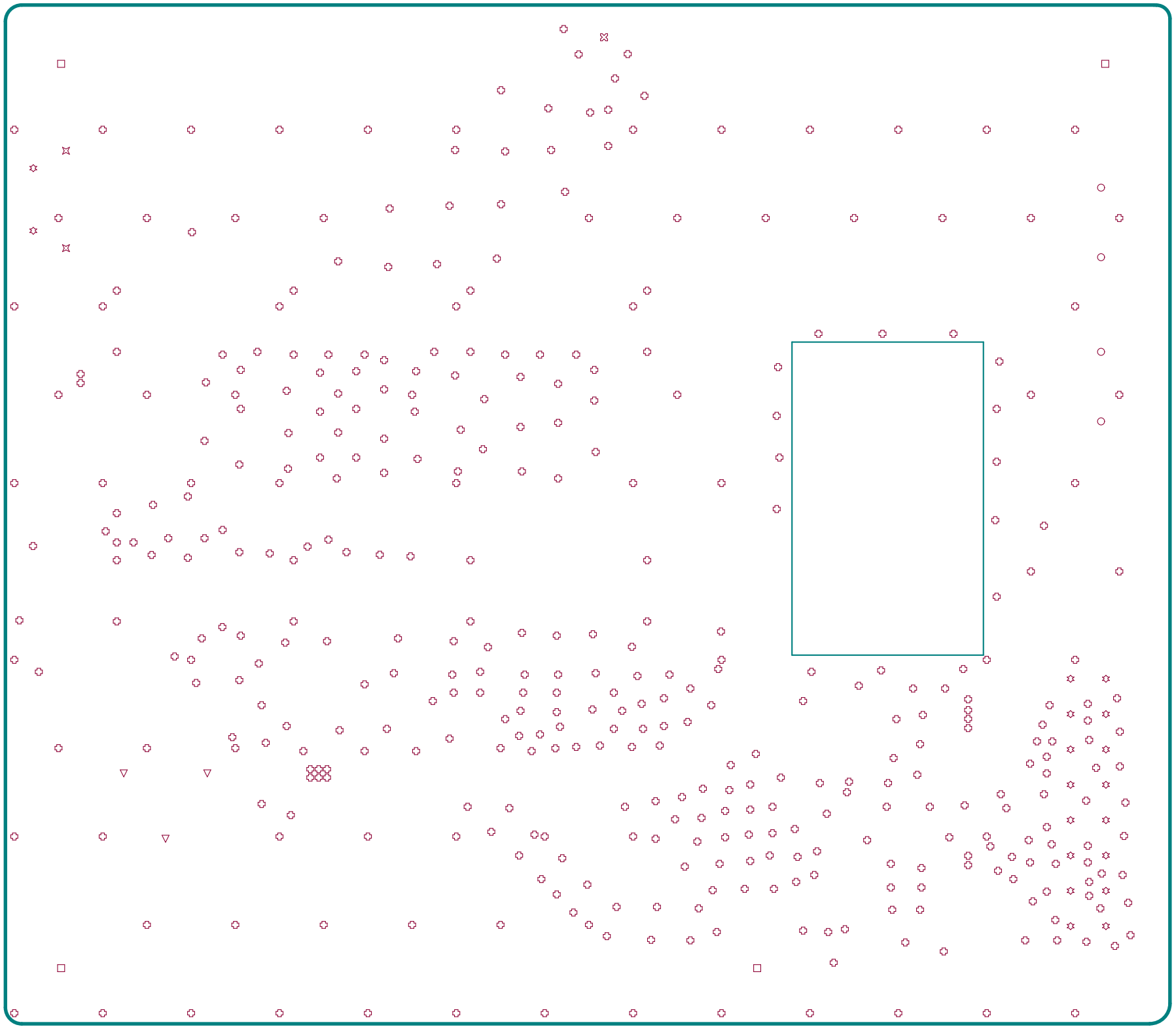


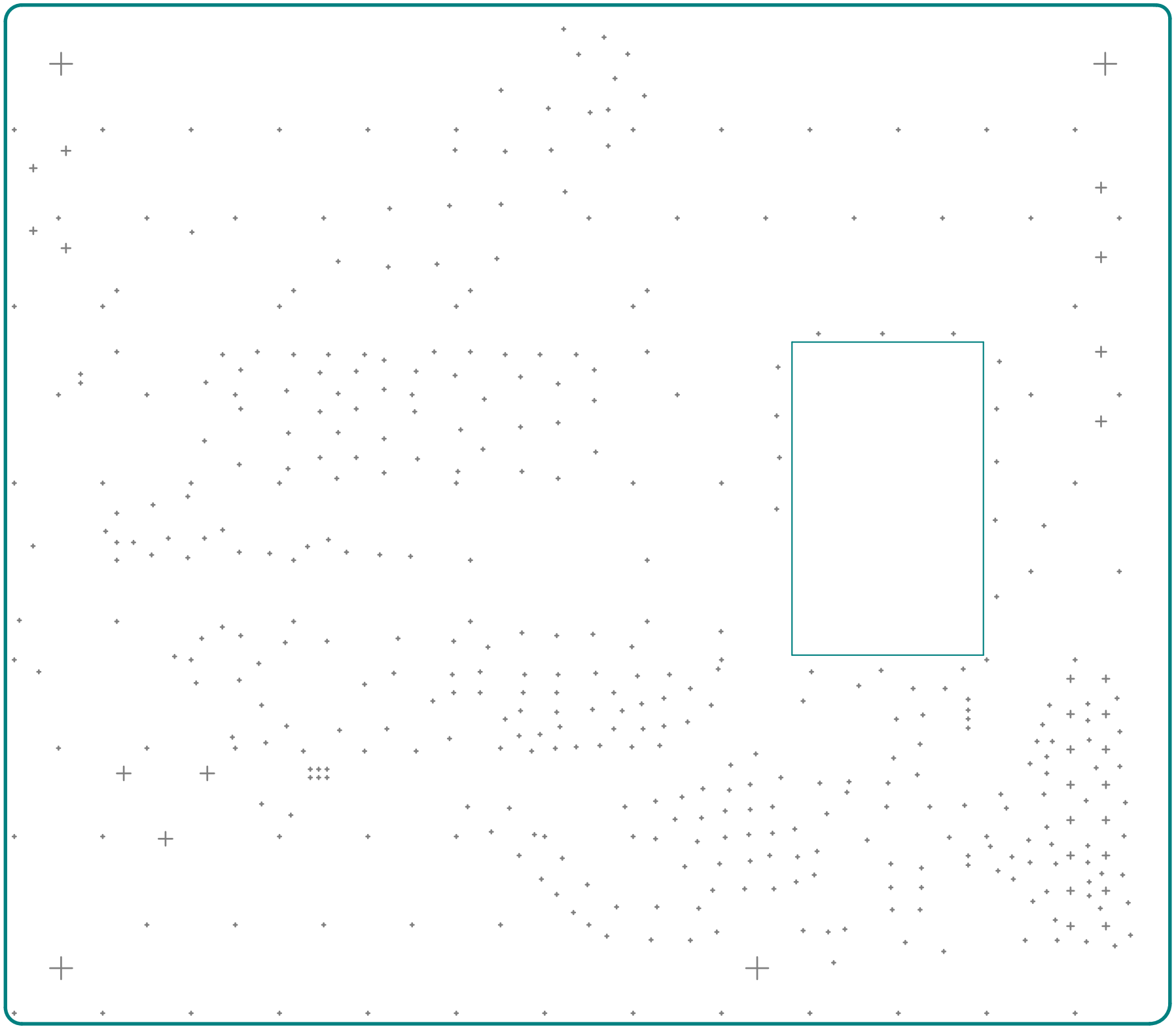

POWER
LED Matrix Board V1











NOTES: UNLESS OTHERWISE SPECIFIED0

1. SPECIFICATIONS/TOLERANCES:
A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES XXXXXXXX.ZIP
B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES IS NOT ALLOWED
D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS)
B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

3. DRILLING:
A. VIA DIAMETERS SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS ARE FINISHED DIMENSIONS.
B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:
A. APPLY LPI SOLDER MASK OVER BARE COPPER USING PROVIDED DATA.
B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR PURPLE.
C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. SILKSCREEN/MARKING:
A. SILKSCREEN PCB PER PROVIDED DATA USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.

B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL NOT BE APPLIED ON ANY PART OF THE PCB

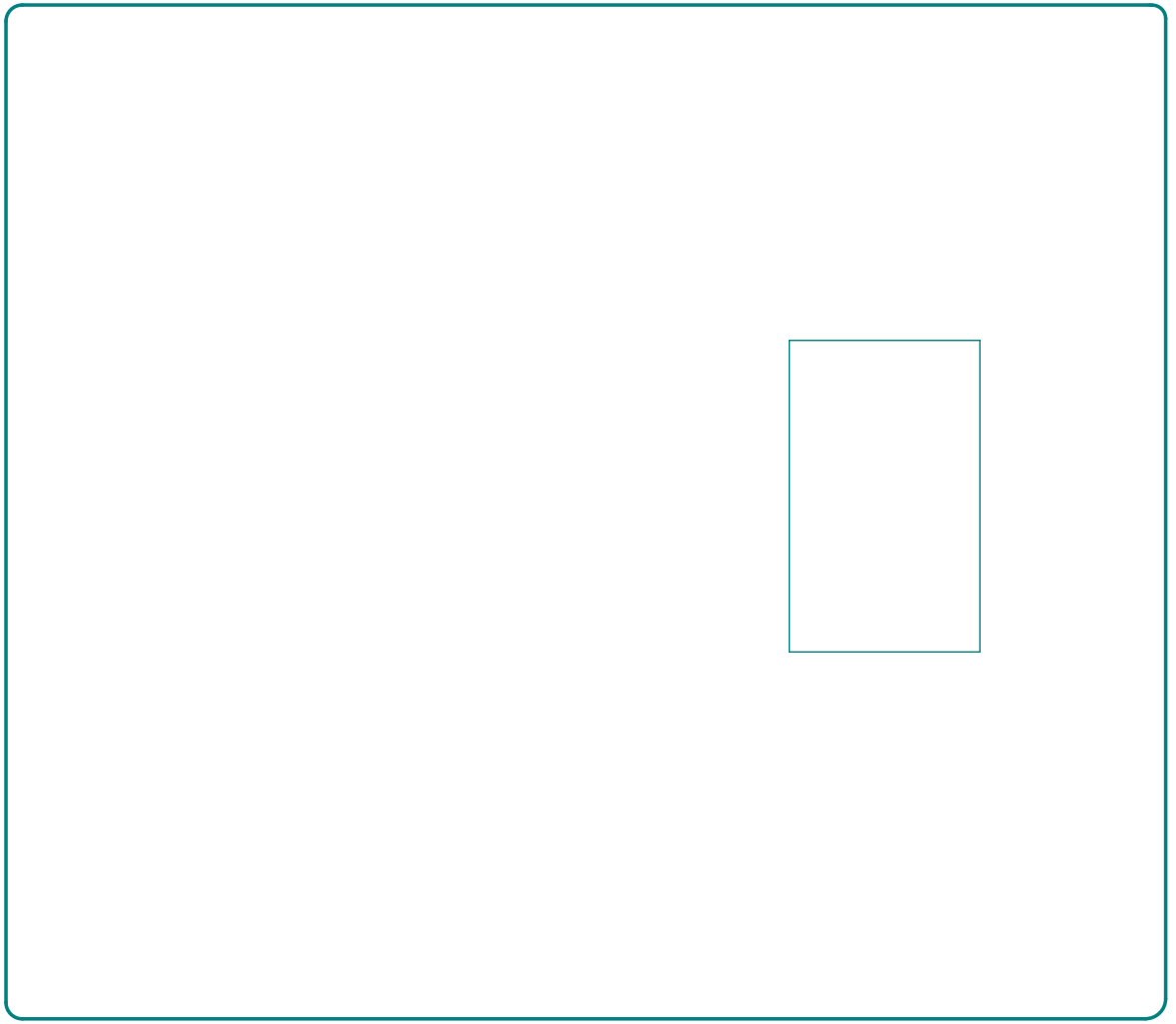
C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE. USING PROVIDED DATA.

6. ELECTRICAL TEST:
A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING GERBER DATA AND AN IPC-D-356 NETLIST.
B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS
C. APPLY TEST STAMP IN NON-LEGEND AREA ON SECONDARY SIDE OF PCB.

7. FINAL FINISH:
A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

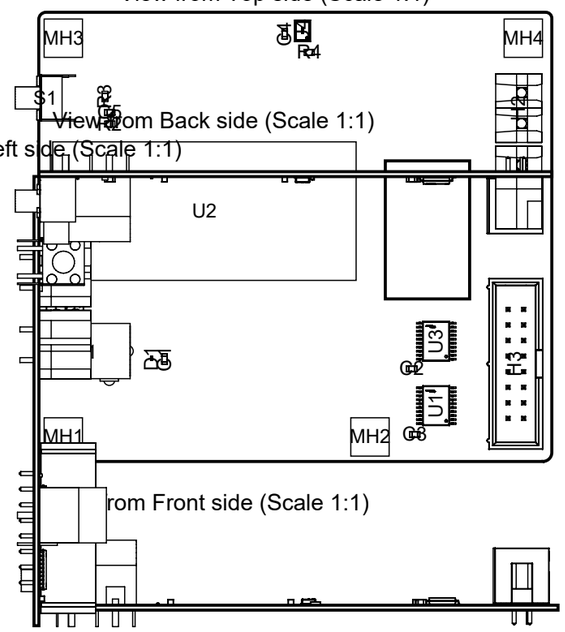
8. IMPEDANCE:
A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE REPLACED BY SUPPLIER PREFERRED (SPECIFICATIONS AS APPROVED).



| | | |
|---|---|---|
| Project: LED Matrix Board | | |
| Company: Morse Micro | | |
| Drawn By: Jonathan Garnier | | |
| | | |
| Date: 31/12/2025 | Rev: 1.0 | |

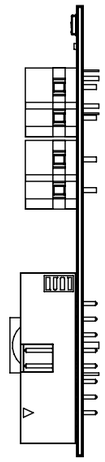
View from Top side (Scale 1:1)




View from Back side (Scale 1:1)

View from Left side (Scale 1:1)

View from Right side (Scale 1:1)

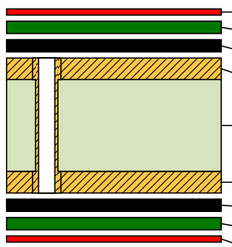


rom Front side (Scale 1:1)

Transmission Line Structure Table

| Transmission Line | Target Impedance | Calculated Impedance | Trace layer | Wide Trace Width | Reference layers |
|---|---|---|---|---|---|
| Coated Coplanar Waveguide With Ground | 50 | 46.79 | Top Layer | 0.80mm | Bottom Layer |

Layer Stack Legend



| Material | Layer | Thickness | Dielectric Material | Type | Gerber |
|---|---|---|---|---|---|
| | Top Overlay | | | Legend | GTO |
| Surface Material | Top Solder | 0.02mm | PSR-4000-BN-Colour | Solder Mask | GTS |
| ENIG | Top Surface Finish | 0.02mm | | Surface Finish | |
| CF-004 | Top Layer | 0.04mm | | Signal | GTL |
| *Core* | | *0.69mm* | *Core* | *Dielectric* | |
| CF-004 | Bottom Layer | 0.04mm | | Signal | GBL |
| ENIG | Bottom Surface Finish | 0.02mm | | Surface Finish | |
| Surface Material | Bottom Solder | 0.02mm | PSR-4000-BN-Colour | Solder Mask | GBS |
| | Bottom Overlay | | | Legend | GBO |

Total thickness: 0.84mm