Low-Power CMOS Digital Electronics for Radio, mm-wave and sub-mm Astrophysics

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ABSTRACT

Here we present the characterization of the performance of a novel design for a digital spectrometer that could be used for high resolution cm/mm/submm spectroscopy. The CMOS ASIC spectrometer design, developed at JPL and UCLA, has dramatically lower power consumption than current approaches that generally employ Field Programmable Gate Arrays (FPGAs). Particularly for space missions and for small satellites, power consumption is a major issue. The order of magnitude lower power consumption of the ASIC approach is thus critical for future missions employing large-format focal plane arrays. Our task was to evaluate this 1024 channel, 1.3-GHz bandwidth CMOS spectrometer in terms of ability to integrate and its filter shape. The chip was to be tested largely at half-maximum speed to allow for use of the polyphase filter bank. The results of this testing show that the ASIC spectrometer can be made to perform largely as expected based on its design parameters, however, they suggest that more testing of the spectrometer chip could be beneficial. Follow-up tests and newer versions of the chip are discussed at the end of the proceeding.

Keywords: ASIC, Astronomy, CMOS, Cubesat, Digital signal processing, DSP, Spectroscopy, Spectrometer

1. INTRODUCTION

Many branches of astronomy rely on high-resolution spectroscopy, including study of molecules in the Earths atmosphere, and probing of interstellar clouds. Such studies are generally carried out by heterodyne systems, in which the incoming signal is mixed to a low frequency, where it is sent to a spectrometer for analysis. This spectrometer needs to have resolution high enough to resolve the spectral line, and enough frequency coverage to encompass the entire line. Current digital technology can do this, but most approaches consume 10s of watts of power for a spectrometer with 1000 channels covering 1 GHz. This is prohibitive for focal plane arrays with 10s or more pixels, which are required to image extended sources in a reasonable amount of observing time.

A promising new technology called Application Specific Integrated Circuit (or ASIC) based on silicon CMOS technology shows potential to revolutionize heterodyne spectroscopy technology. Such a circuit has been designed by a team led by Dr. Adrian Tang of JPL. This new spectrometer technology offers drastically reduced power consumption and far greater compactness and lower weight than alternative technologies. If we can demonstrate that the CMOS spectrometer performs appropriately, it can be an enabling technology for a variety of suborbital and space missions.

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The objective of this project was to verify the performance of a novel design for a digital spectrometer that could be used for high resolution cm/mm/submm spectroscopy. The CMOS ASIC spectrometer design, developed at JPL and UCLA, has dramatically lower power consumption than current approaches that generally employ Field Programmable Gate Arrays (FPGAs). The ASIC approach has the drawback that once designed and fabricated, its functionality cannot be changed (unlike the FPGA that can be reprogrammed if there is an issue). Thus, it is particularly important to ensure that the design works properly so that future, even more capable designs with greater bandwidth and more channels, will perform properly. Note that this spectrometer chip was the sixth iteration created by Adrian Tang, and as such, the chip may be referred to as the "SVI" throughout this proceeding. ASU and JPL are both interested in astronomical submillimeter spectroscopy, employing aircraft, balloon, and space missions. Particularly for the latter and for small satellites, power consumption is a major issue. The order of magnitude lower power consumption of the ASIC approach is thus critical for future missions employing large-format focal plane arrays. Verifying the performance of this first prototype ASIC spectrometer thus offered an excellent opportunity for collaboration between ASU and JPL. A number of tests were thus designed to verify integration ability and spectral resolution:

1. The Allan Variance of the spectrometer was measured with a white noise input in order to evaluate its long-term integration stability.
2. The bin filter shape of the spectrometer of multiple bins was measured to verify consistency between bins and determine the precision of the output.
3. The bin filter shape was measured with varying clock power levels to investigate certain anomalous behavior that was found during testing.

2. TEST 1: ALLAN VARIANCE WITH WHITE NOISE INPUT

In order to perform this test, the setup depicted and diagrammed in Figure 1 below was used. The spectrometers hardware averaging settings were set to average on low clock 0 and high clock 40. The spectrometers polyphase filter bank (PFB) setting was disabled in order to run the spectrometer at its full clock speed. The PFB is a mechanism for alleviating two of the major drawbacks that occur when performing discrete Fourier transforms, namely, leakage of tone into surrounding bins, and loss of energy between bins. Since a spectrometer such as ours relies heavily on these discrete Fourier transforms, we expect the PFB to have a significant effect on our output. However, when the PFB is enabled, approximately 50% more resources are required to process a signal than when it is disabled. Because of this, the clock on the SVI spectrometer we tested was designed to only run at maximum speed when it has the PFB disabled.

The spectrometer was run at its maximum clock speed of nominally 1.3GHz. The clock input signal frequency was manually adjusted to a value between 20MHz and 21MHz until lock-in was achieved. However, the precise clock frequency was not recorded, and in general, lock-in was not achieved at the same frequency on every run. The clock input signal power level was -10dBm. A 1000MHz low-pass filter was used between the white noise source and the spectrometer. The output of each bin was measured at every output period for a duration of roughly one week. Because our Allan Variance code requires a power-of-2 count of measurements, not all the data was used. A picture of the testing setup done at ASU can be seen in figure 2.

The clock and averaging setting used resulted in an average data collection rate of 1 measurement per bin per 2119ms. The plots in figure 3 show sample Allan Variance results. For Gaussian noise, the Allan Deviation should vary as $t^{-0.5}$, and thus the Allan Variance, which is the square of the Allan Deviation, should vary as t^{-1}. The curves show that the spectrometer exhibits this behavior for integration times up to 1000 s. For longer times, the Variance exceeds that expected from the input signal. The Allan Time is the time up to which the spectrometer adds essentially no noise, and for this unit is 1000 s. This is practically not significant since microwave receivers themselves typically have Allan times of order 30 s or at maximum 100 s. Thus, such receivers have to switch on and off source at least this rapidly. In practice, the ASIC spectrometer would not be a significant constraint on observational approach.

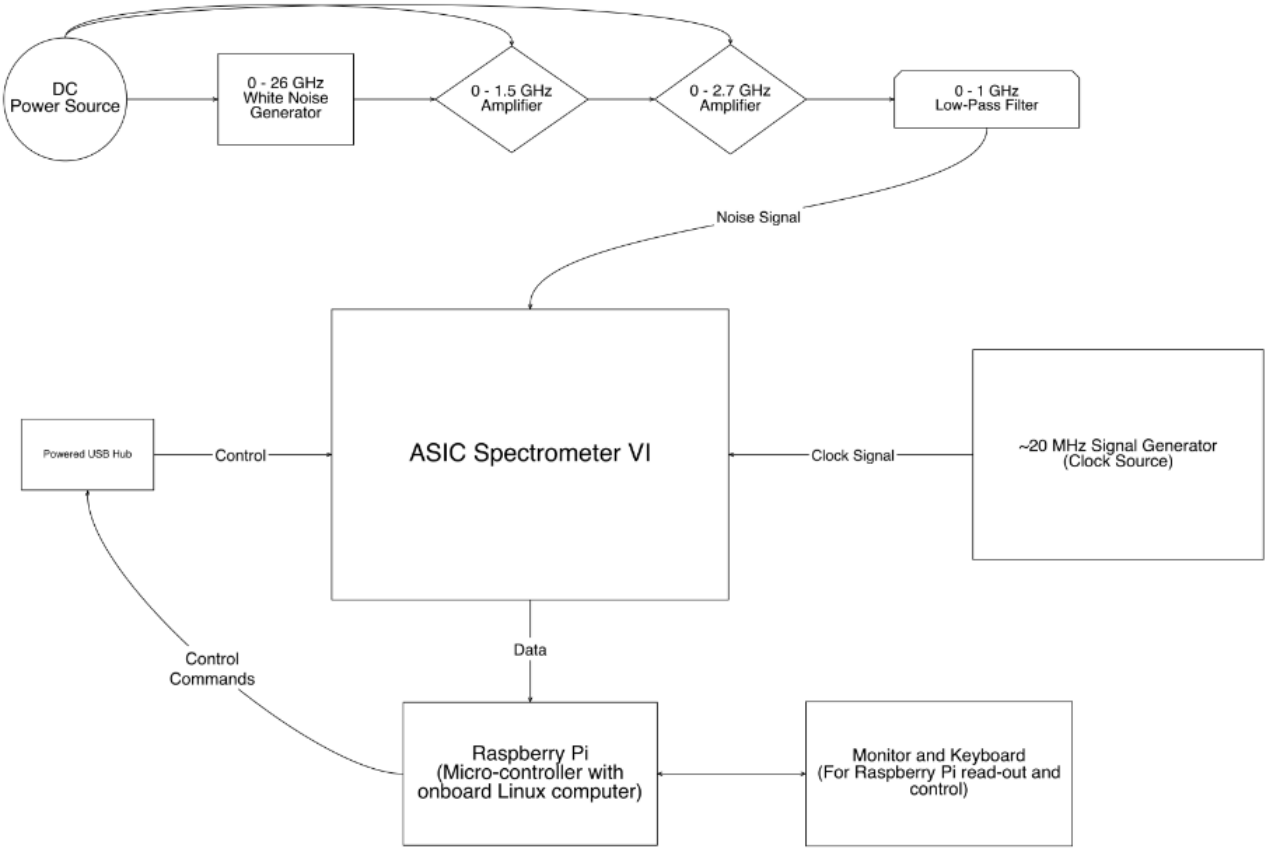

Figure 1. Block diagram for testing the Allan variance of the CMOS spectrometer

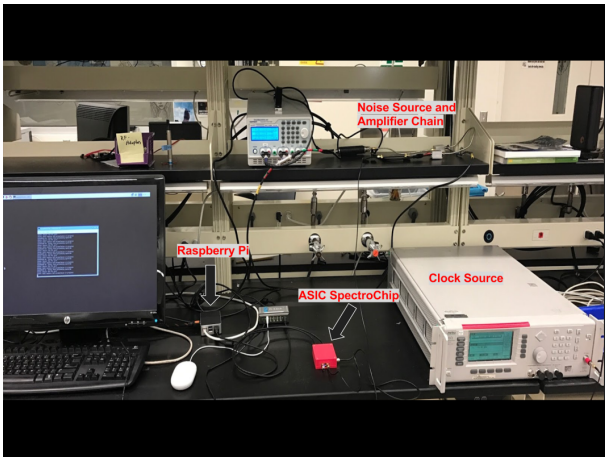

Figure 2. Labeled photograph of testing setup for Allan variance testing.

The fact that the Allan variance plots are all quickly shifted away from the t^{-1} line but retain the shape as expected is a peculiar issue. While the important part of the results is where the "turn-off" from

the desired slope occurs, one would expect the data to more closely resemble the green t^{-1} line. One of the possibilities is that there is a systematic error somewhere in our setup. The same Allan variance and filter shape testing is currently taking place on the newest model of the chip, and the setup is being more closely monitored and controlled. We will address this more in the "discussion" section.

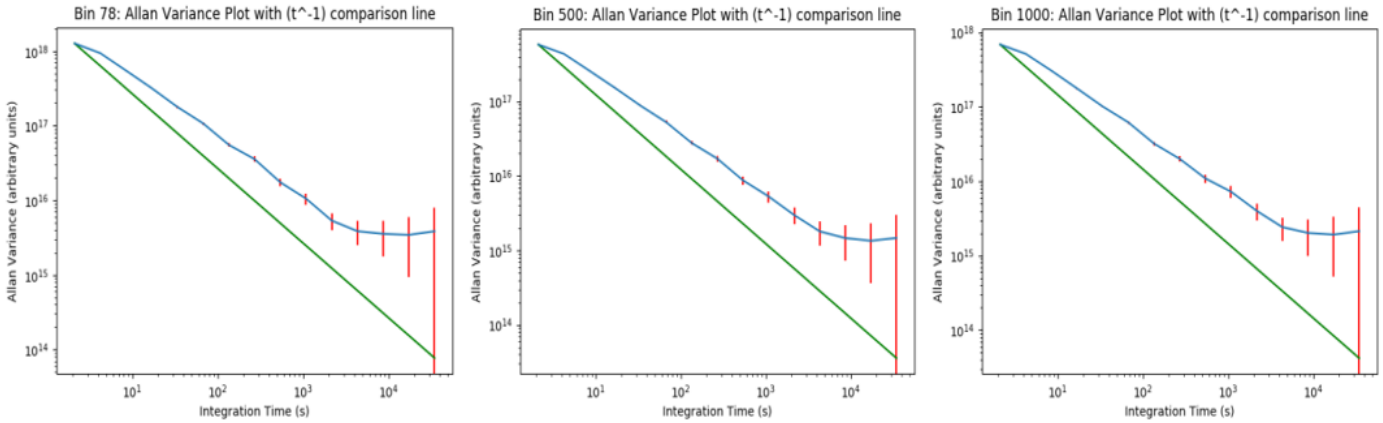

Figure 3. Results of Allan variance testing from a white noise generator. The plots above show three separate bins; bin 78 (left), bin 500 (center), and bin 1000 (right). Each bin is slightly larger than 1 MHz in bandwidth.

3. TEST 2: BIN FILTER SHAPE TESTING WITH PFB TOGGLED

Testing of bin filter shapes was performed according to the diagram and picture shown in Figure 4 and 5 below. The spectrometer and clock were set identically to in Test 1, with the following exceptions: the hardware averaging was set to be done on low clock 0 and high clock 10. The spectrometer was set to run at half-speed, which is nominally .65GHz.

A sinusoidal input signal was swept across a range of frequencies at least 20MHz wide roughly centered around the bin being tested. The sweep was performed in .04MHz increments. The output of the bin being measured was measured 10 times at each incremental frequency, resulting in roughly 11 seconds of measurement at each frequency.

Bins 78, 500, and 1000 were each measured twice in this manner, once with the PFB enabled and once with it disabled. Results are shown in Figure 6 below. The output levels as a function of input frequency for each bin were plotted to visualize the filter shape. Statistical error bars are not depicted, but for 95% of measurements made, the statistical error was less than 1dB. The functions look much as we expect: a sinc-like function is observed when PFB is disabled, and a more square-topped function is observed with PFB enabled. The 3dB width of the filter shape with PFB disabled was measured to be 0.6MHz, and with PFB enabled to be 0.5MHz.

4. TEST 3: FILTER SHAPE TESTED WITH VARIABLE CLOCK SOURCE POWER

The spectrometer was tested in an identical fashion to Test 2, with the following exception: the clocks power level was varied between -10dBm (green line in Figure 6), -13dBm (blue line in Figure 6), and -15dBm (orange line in Figure 6) . For this test, we focused only on Bin 900, and it was measured with the PFB enabled.

We expected that the clock power would not affect the filter shape of the spectrometer significantly, as the spectrometer only uses the clock input for a reference when processing the actual signal input. The results are shown in Figure 6. When we compared a clock power of -10dBm (green) with a power of -15dBm (orange),

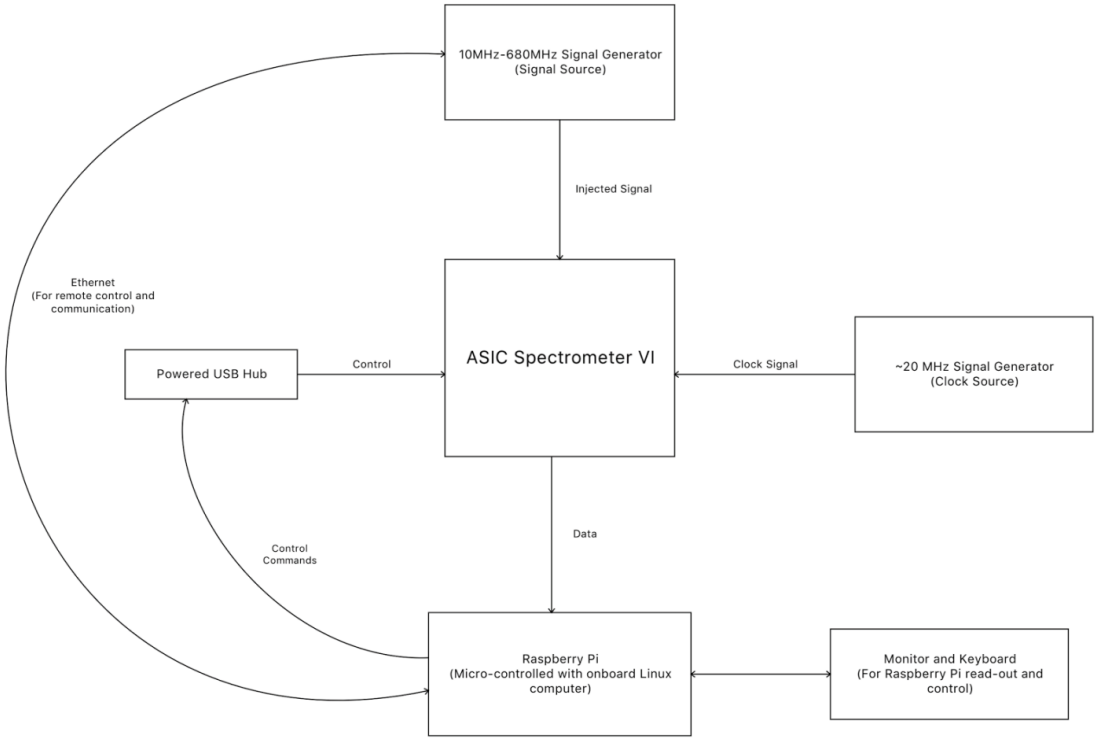

Figure 4. Block diagram of filter testing setup

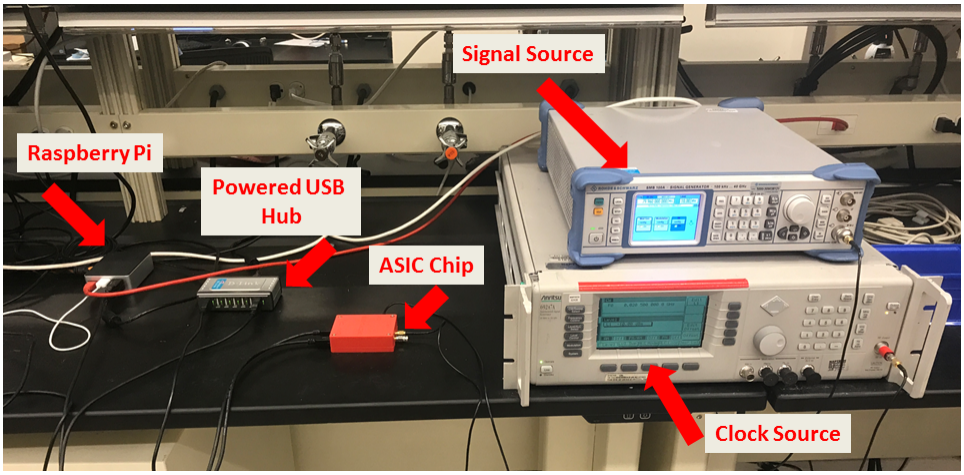

Figure 5. Labeled photograph of filter shape testing setup.

we found that there was a shift of less than 1Mhz between them. This shift was well within our anticipated range of change. However, setting the clock power in between these two at -13dBm (blue), we see drastically different qualitative features. As for the -10dBm and -15dBm tests, there is still a peak around 582Mhz, but it is significantly lower by nearly 20dB. Furthermore, a 0dB peak seems to appear around the 600Mhz input point, which in the green and orange lines was nearly a noise floor. Finally, the noise floor itself has dropped in the -13dBm case from around -32dB to -40dB.

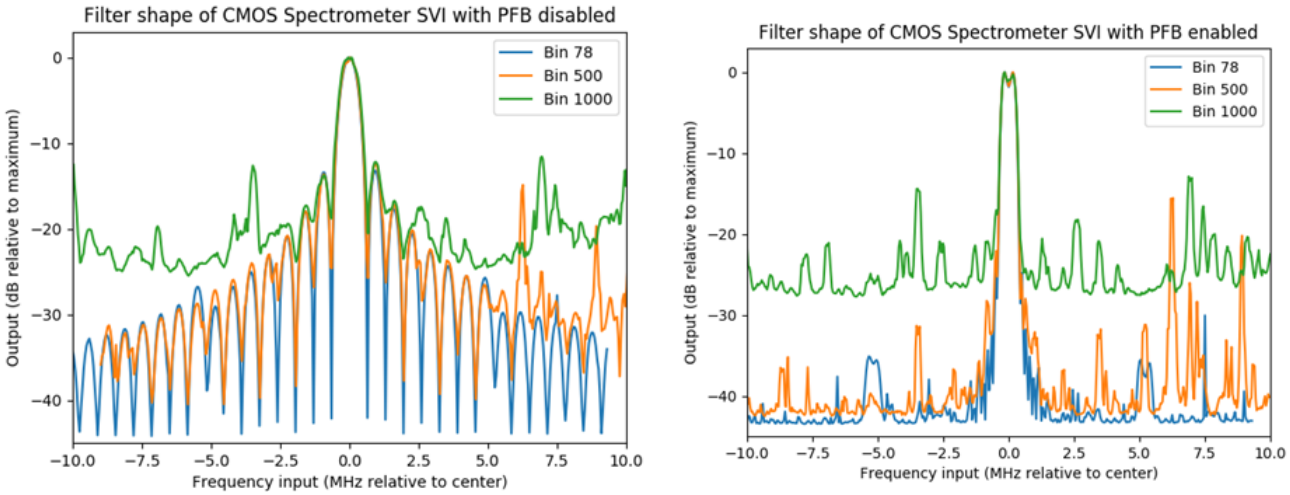

Figure 6. Filter shape results of bin 78 (blue), 500 (orange), and 1000 (green). The filter shapes were collected with both the PFB off (left) and on (right). As predicted, applying the PFB algorith, had a significant effect on the data.

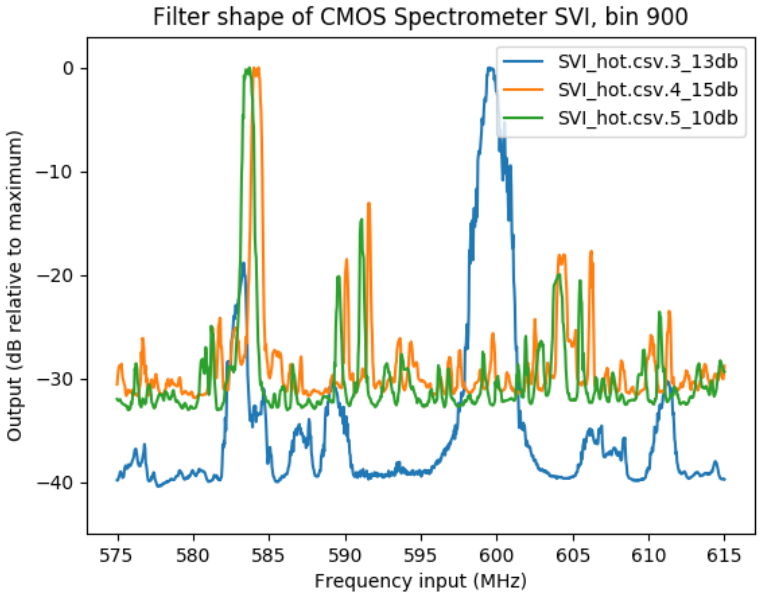

Figure 7. Response of bin 900 given different clock power levels across a spectrum of frequencies. Clock powers of -10dB (green) and -15dB (orange) gave results as expected. Surprisingly, -13dB had unusual signatures. This issue has been communicated to Adrian Tang and is addressed in the "discussion" section.

5. DISCUSSION

Notable results of our testing are as follows: we have seen that the Allan Variance plots for white noise input exhibit a turnoff between 103 and 104 seconds, but the Allan time is even longer when measuring the Allan Variance of the difference of the outputs of two bins. The filter shapes look much as they were expected to, with 3dB widths of .6MHz with PFB disabled and .5MHz with PFB enabled. The noise floor of bin 1000, however, was 15dB higher than those of bins 500 and 78. Finally, the filter shape appears to be anomalous when the clock power level is set to -13dBm.

While the results of both the Allan variance and filter shape testing show great promise for astronomical use of the SVI spectrometer chip, it is apparent that more experimentation is needed. After the original testing process was finished, the results were sent to the chips inventor, Adrian Tang. Taking into consideration some of the issues we had with the SVI model, a newer version was created and dubbed the "SVII." Apart from doubling the sampling rate of the spectrometer to 6 Gb/s which increased the bandwidth to 3GHz, the clock input was modified. Instead of using any external clock source to create a reference signal for the chip, the SVII comes with a Crystek crystal operator that oscillates at exactly 23.4375MHz. This allows for there to be a known clock frequency, and more importantly, clock power. Since one of the more notable issues with the SVI was the change in noise floor at different clock powers, this improvement completely eliminates the need to test such a parameter.

Our lab plans to do the exact same Allan variance and filter shape testing to the SVII except this time we want to assure that our testing environment is as controlled as possible. The white noise source used for the Allan variance test needs around 70dB of amplification before it reaches a level which can be recognized by the spectrometer chips. In the test setup done for this proceeding, the amplifier chain was simply put on a lab bench attached to the noise source and SVI. In order to eliminate all possible sources of error, the amplifier chain for the SVII testing has been placed in a custom-made Faraday cage fashioned out of a Hammond box so that no RF interference can make its way into the results. Furthermore, a heat sink has been manufactured onto the back of the SVII to avoid any thermal noise that could occur from the considerable heating during the signal acquisition process. With the inclusion of these environmental changes, we hope to see less peculiar results in the Allan variance testing.

6. CONCLUSION

The results of this series of tests show that the ASIC spectrometer can be made to perform largely as expected based on its design parameters. However, they suggest that more testing of the spectrometer chip is required. Based on the Allan Variance plots obtained in part 1 (figure 3), it is possible that there is an issue with the long-term integration of the chip; however, the reduced turnoff seems to indicate that while the output may have been drifting, the relative outputs between bins was drifting to a lesser extent. It is possible that the overall drift was an artifact of our testing system, rather than the chip itself, and so additional testing would be useful to confirm this.

The filter shape testing confirms that the spectrometer has the resolution expected, and that its polyphase filter bank works properly. The higher noise floor for certain bins is something which could warrant investigation, but a -27dB noise floor is likely sufficiently low for the applications it will be used in. Finally, the anomalous filter shapes exhibited for a clock power level of -13dBm (figure 85) could be an artifact of the test system used, but definitely warrant further investigation. The testing also demonstrated that the peak of the filter shape is not necessarily constant; testing this against the clock input frequency would likely be useful.

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