Behavioral model of Memory Controller scheduler

BUG REPORT

- **ACT to ACT (Different Bg)**
  Satisfied
- **ACT to READ (Bank does not matter)**
  Delay of 3 dimm cycles to issue RD0
- **Act to Write (Bank does not matter)**
  Delay of 3 Dimm Cycles to issue WR0
- **Read to Read (same bank group)**
  Satisfied
- **Read to Read (different bank group)**
  Delay of 4 Dimm Cycles
- **Write to Write(same bank group)**
  Delay of 2 dimm cycles
- **Write to Write(different bank group)**
  Delay of 2 dimm cycles
- **Write to Activate (different bank group/same bank group)**
  Delay 1 dimm cycle.