AARHUS
UNIVERSITY
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3. MARCH, 2015

CLOCK DOMAINS AND TIMING

AGENDA

- Clock Domains
- Timing/Synchronization Issues
- FPGA Clock Generation & Distribution
- Reset Circuits

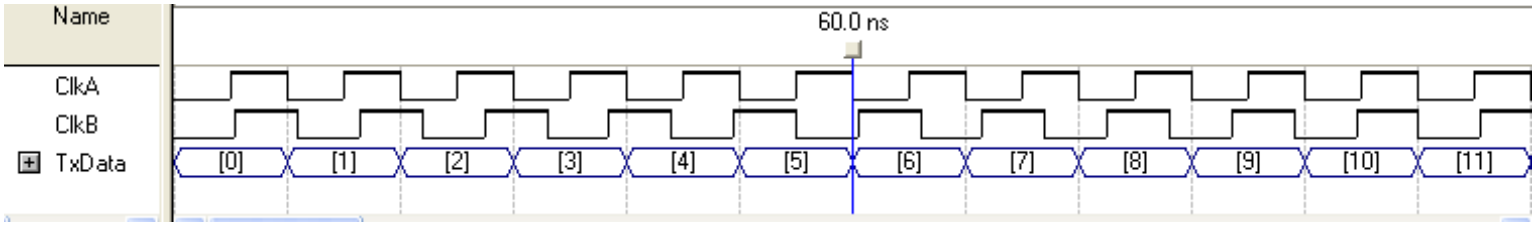
CLOCK DOMAINS

Tx Data

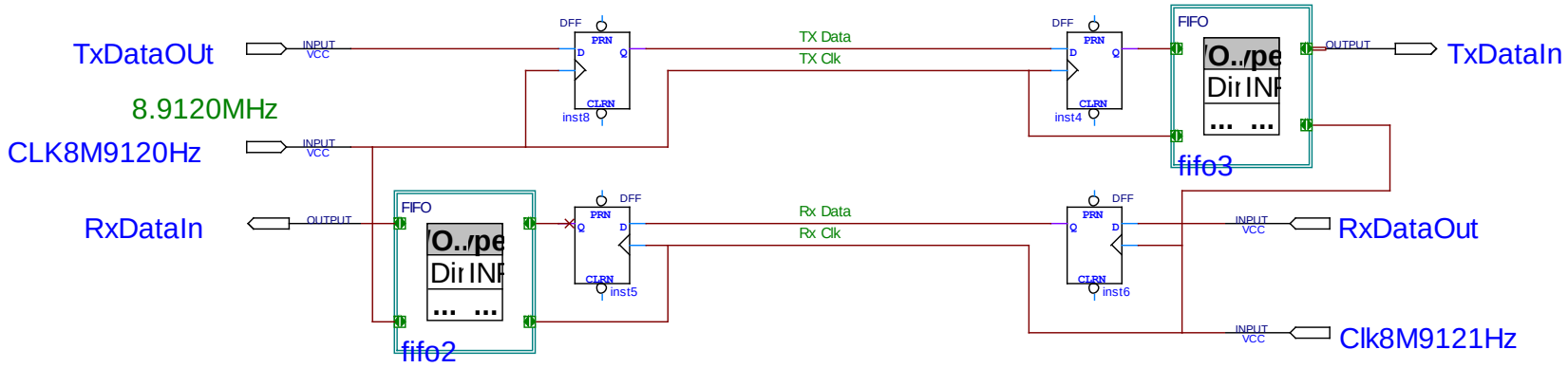
Rx Data

8.1920 MHz

8.1921 MHz



CLOCK DOMAINS

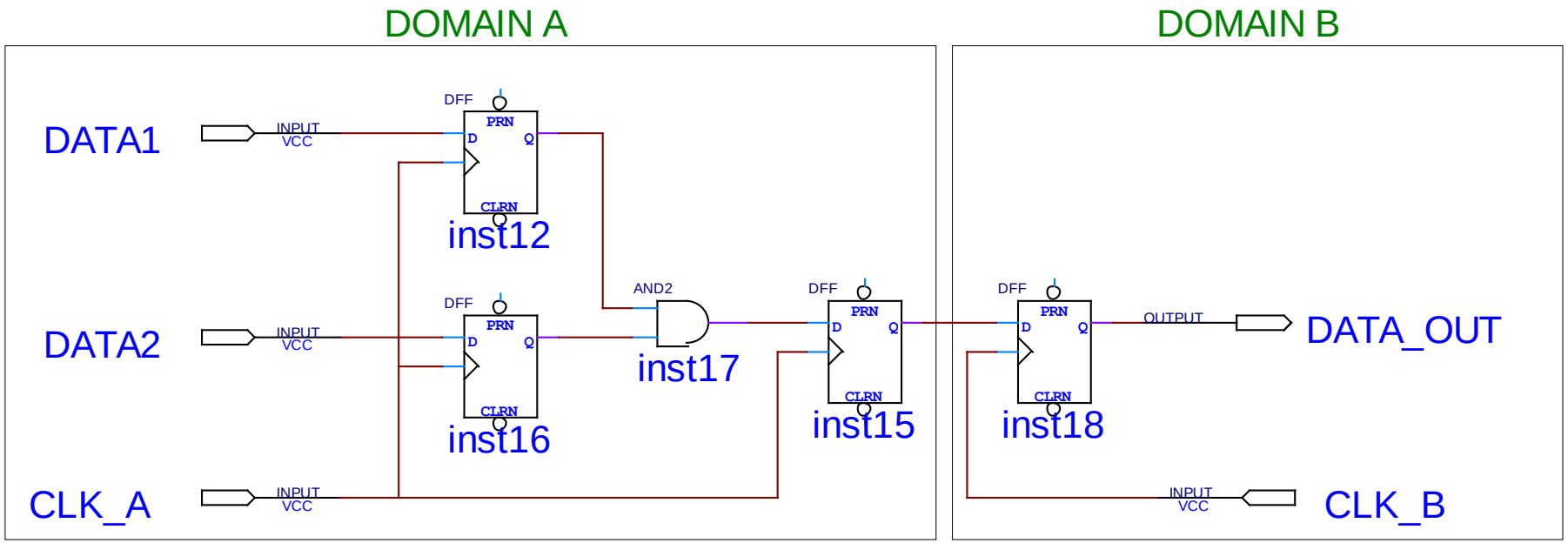


Solution:

› Tx / Rx Data have companion clocks

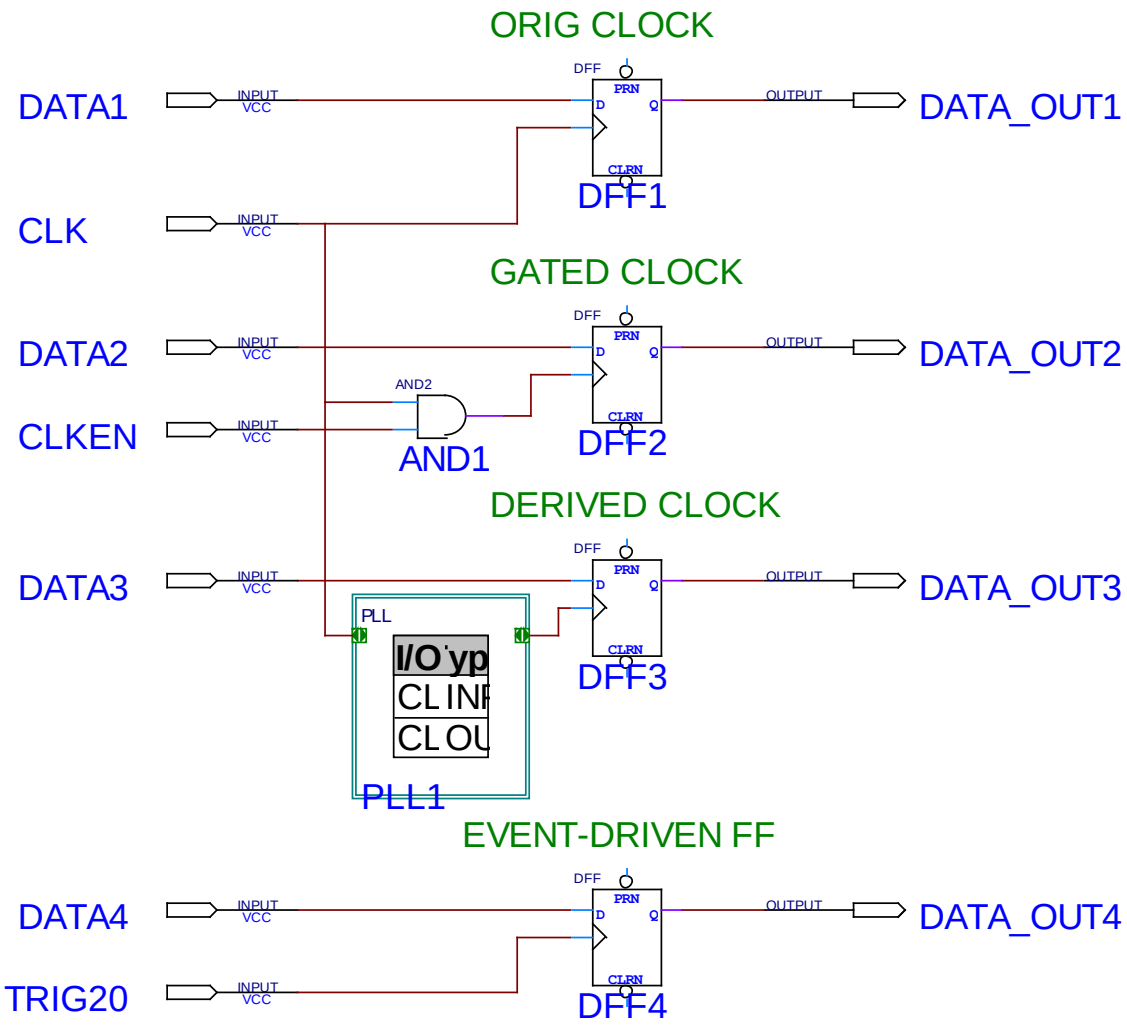
› Clock domain crossing in FIFO / Dual-Port Mem etc.

CLOCK DOMAIN DEFINITION



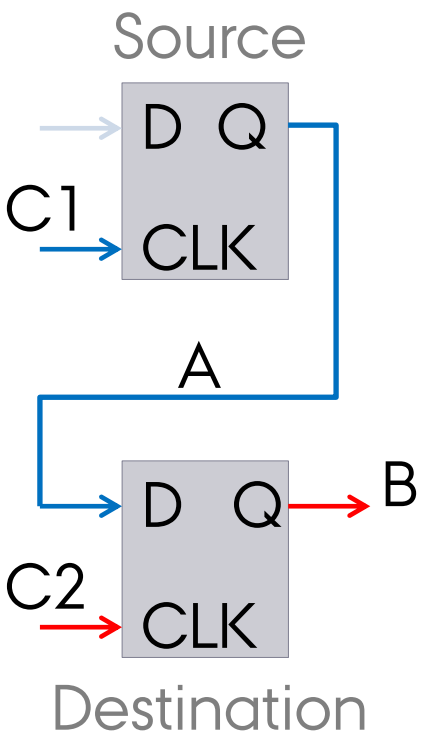
› A Clock Domain is a section of logic where all synchronous elements are clocked by the same clock

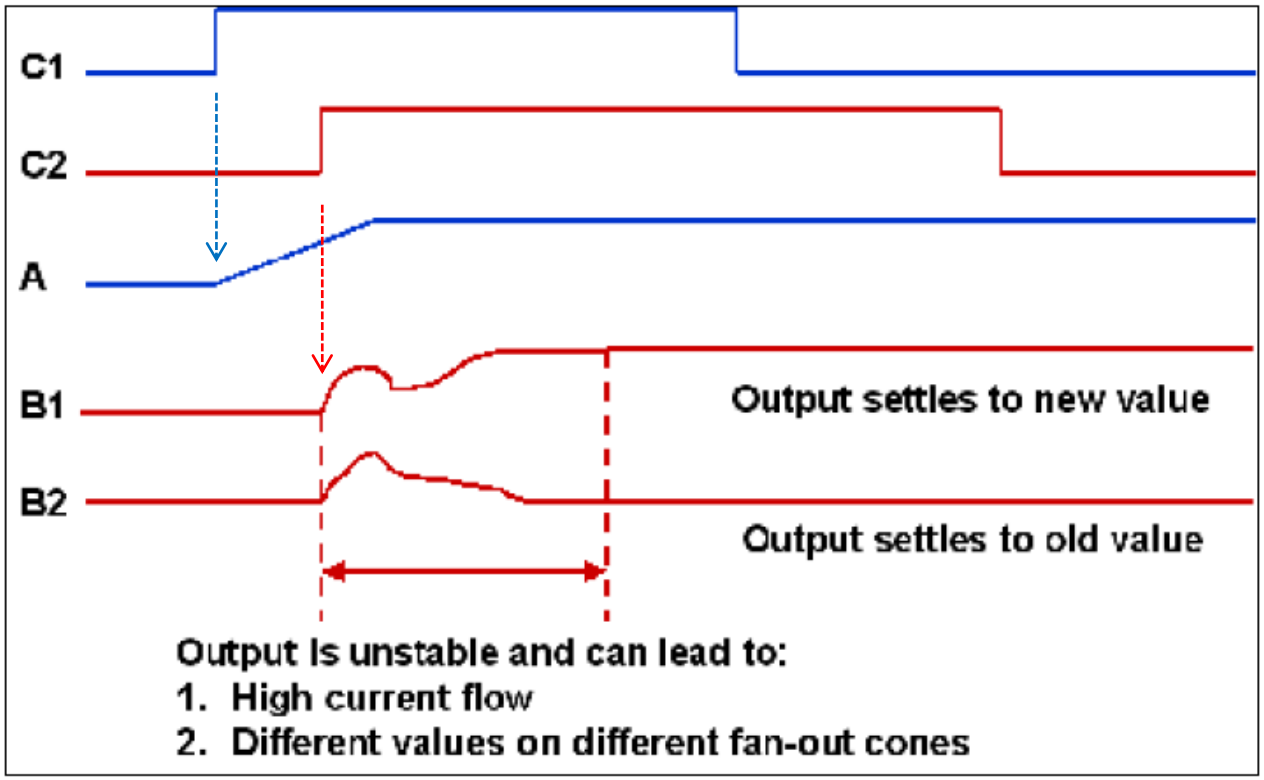
CLOCK DOMAINS TYPES



Clock Domain crossing issues

METASTABILITY



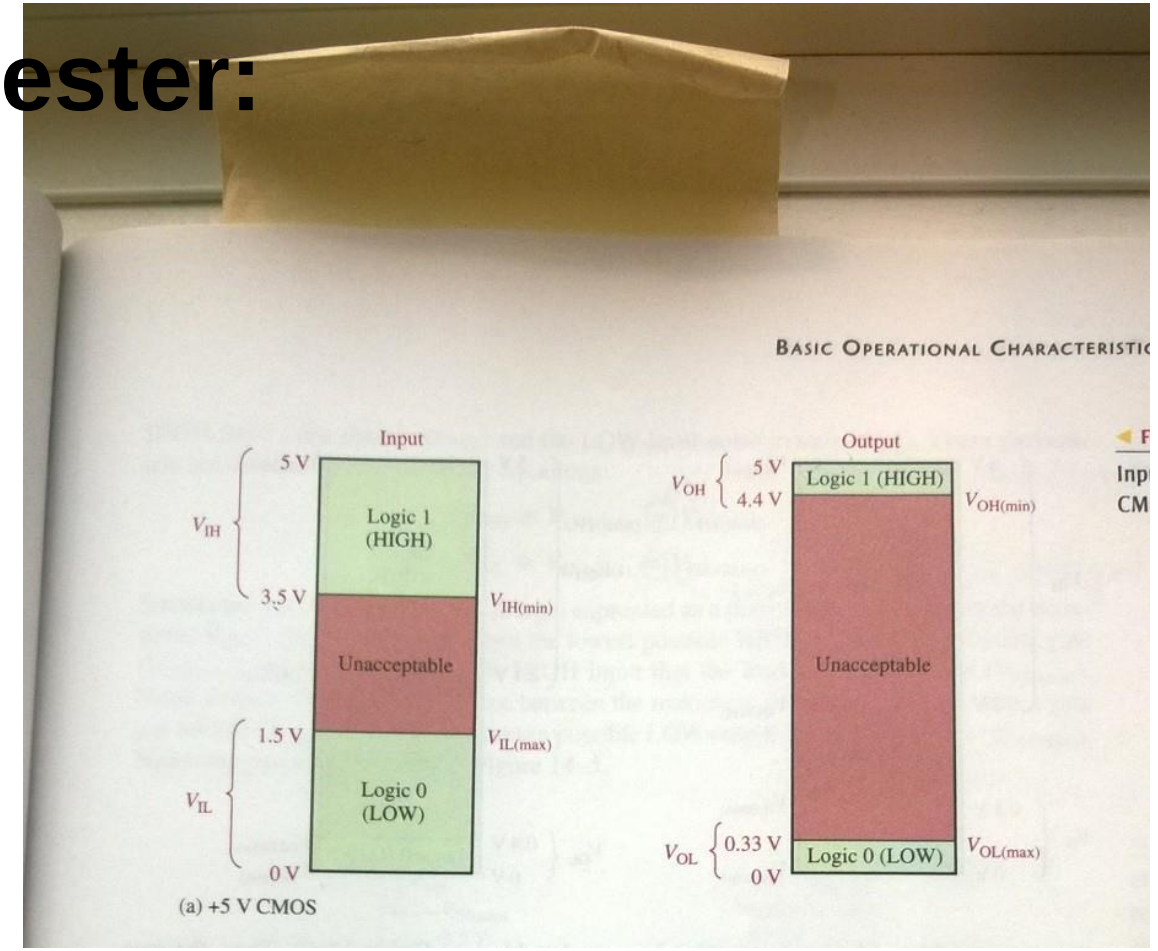


[Verma: Understanding clock domain crossing issues]

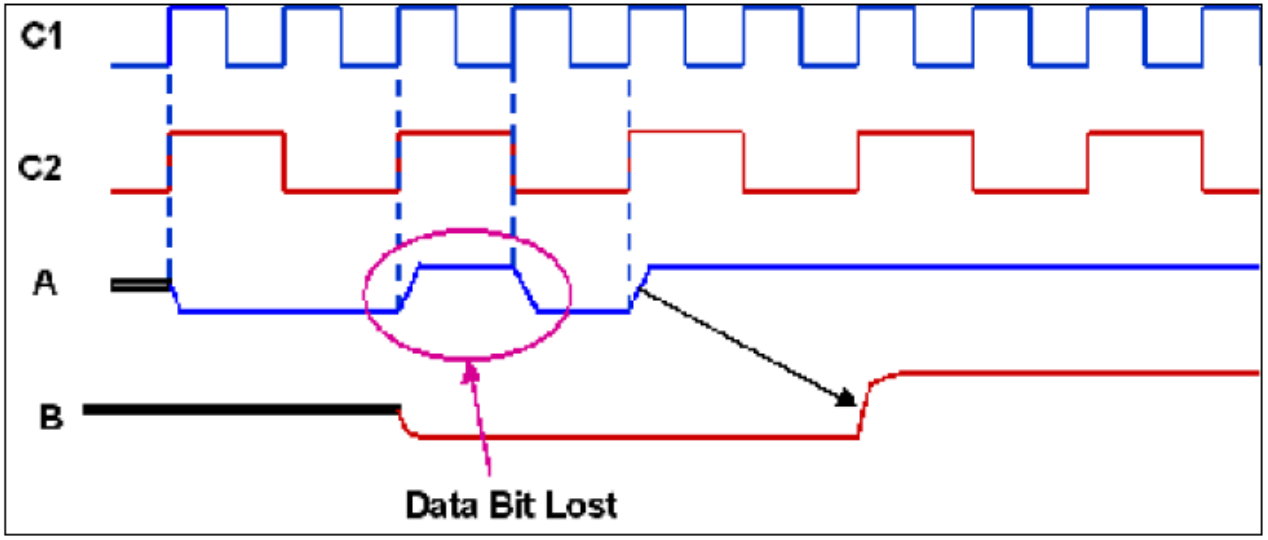
› Metastability occurs when source and destination clocks edges are too close

A STEP BACK...

To 1st. Semester:



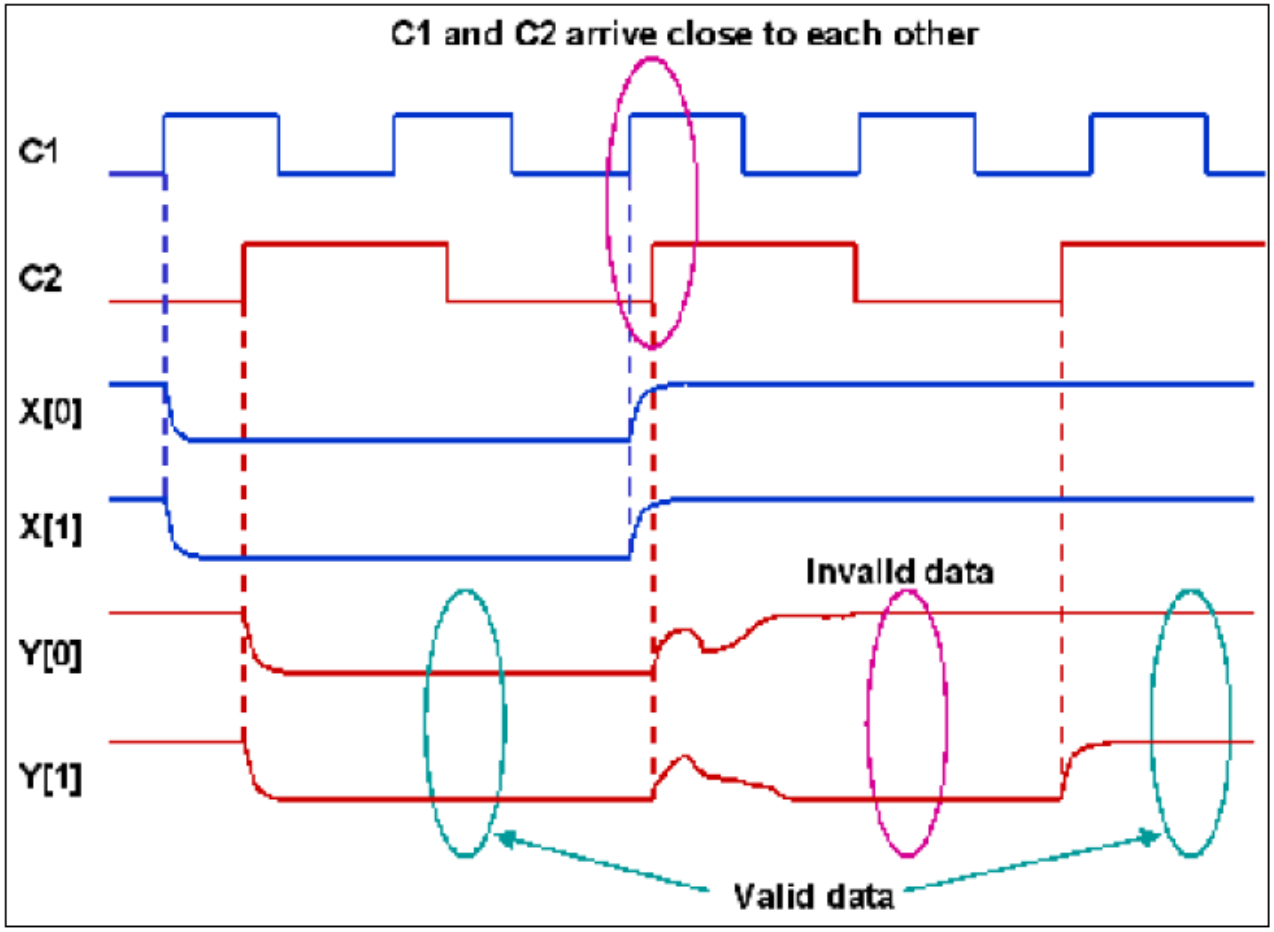
DATA LOSS



[Verma: Understanding clock domain crossing issues]

› Destination Clock is too slow to capture all input signal changes

DATA COHERENCY



[Verma: Understanding clock domain crossing issues]

› Data Coherency Issues: Individual bits of a bus may take different number of cycles to settle due to metastability

?

The main problem in crossing multiple clock domains is:

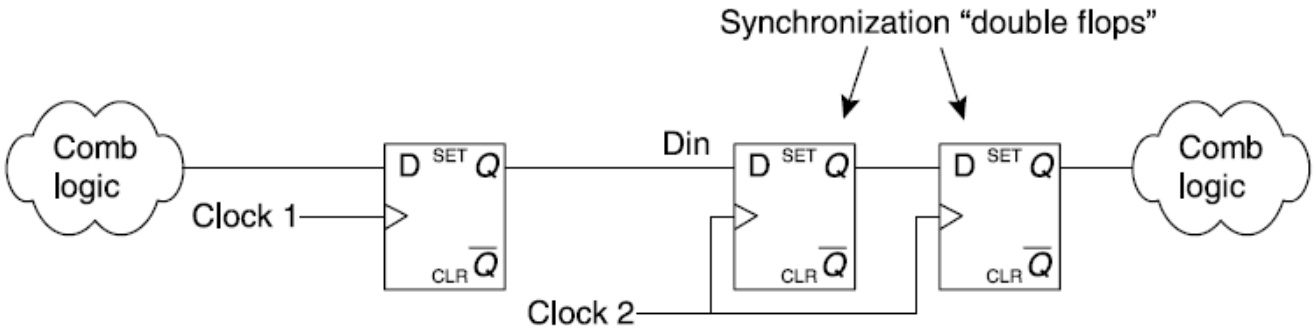
1. Instability
2. Metastability
3. Clock loss
4. Resampling

Solutions to Clock Domain Issues

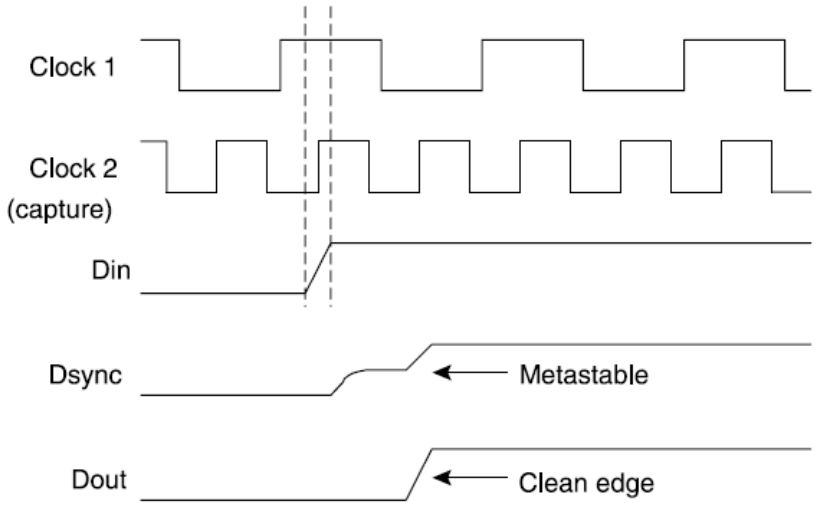
SOLUTIONS

Clock Type	Async / Sync	Solution
Gated Clock	Synchronous, but with poorly defined phase	Avoid! Except for ASIC designs!
Derived	Synchronous, Integer or Rational multiple, well defined phase	Phase Shift / FIFO / DP MEM / FSM, double flopping
Event-Triggered	Asynchronous	Double Flopping / DP MEM / FIFO / FSM, Handshaking
Asynchronous Clocks	Asynchronous	Double Flopping / DP MEM / FIFO / FSM, Handshaking

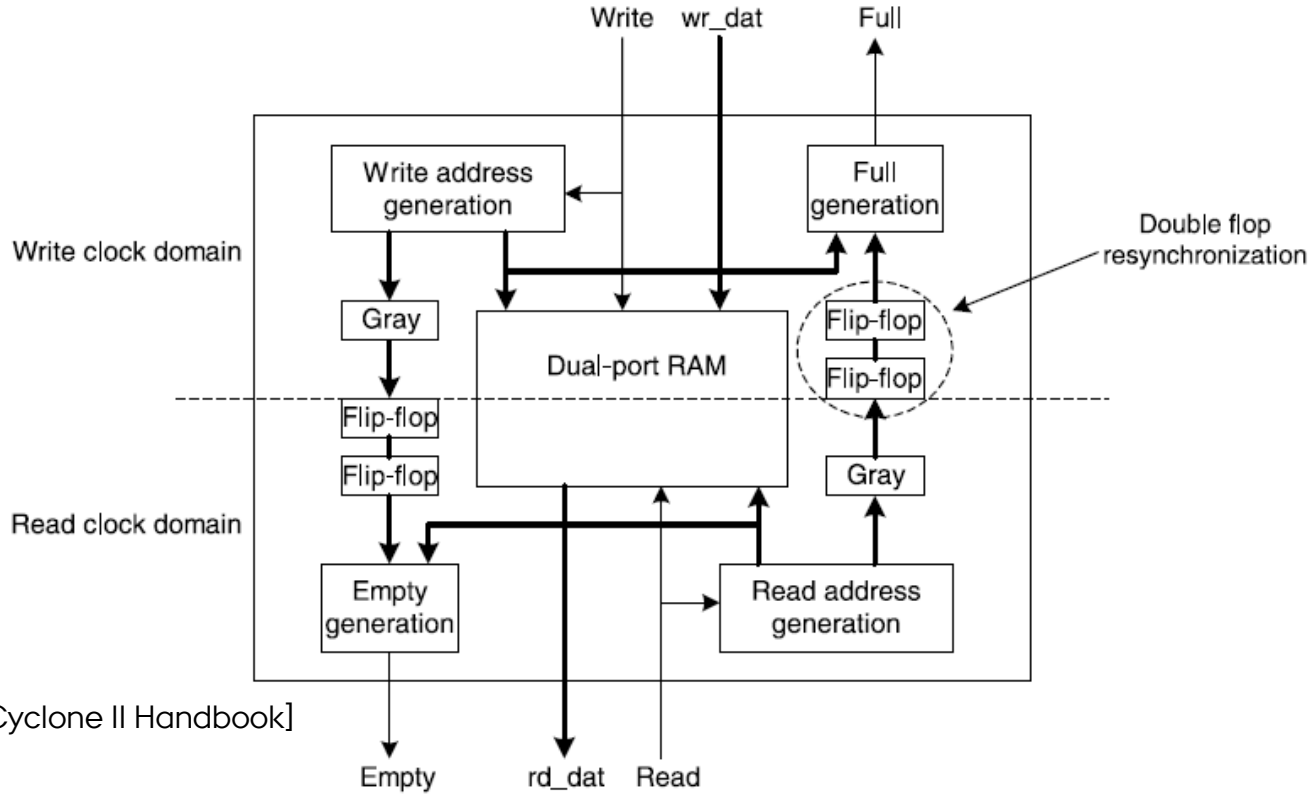
DOUBLE FLOPPING



- Double Flopping allows the metastable signal to settle
- Only useful for single-bit signals



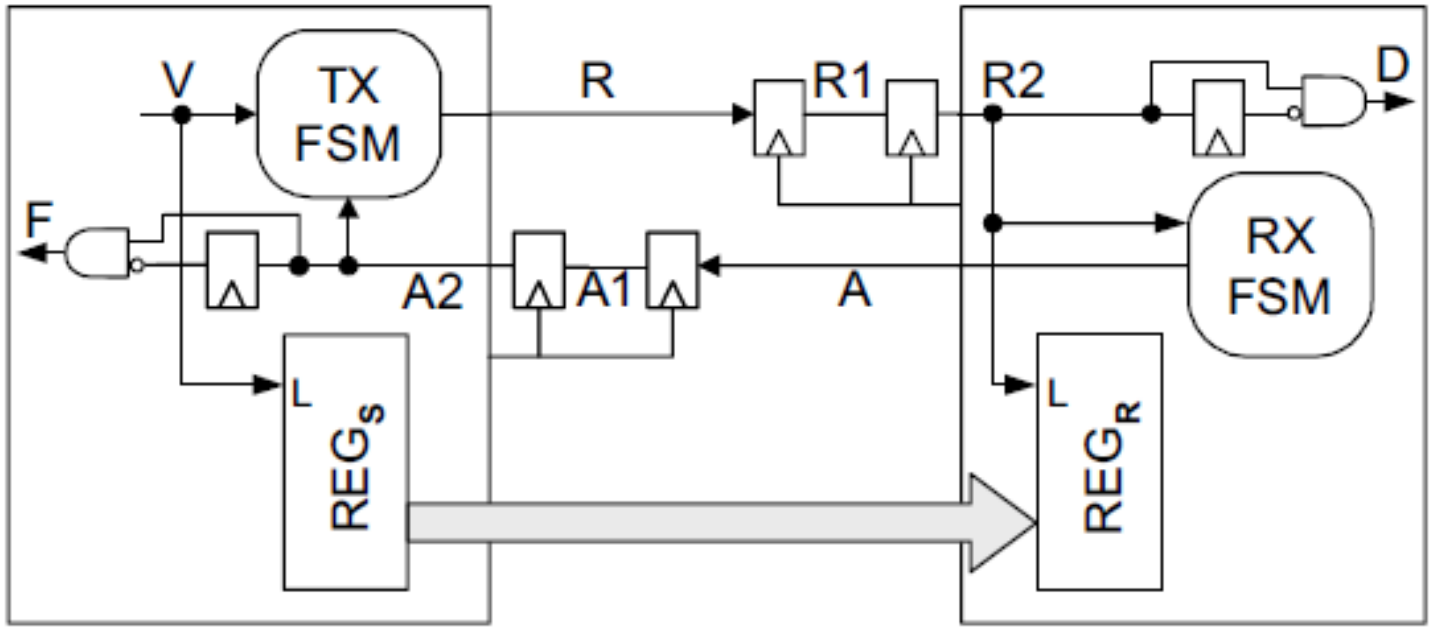
FIFO / DUAL-PORT MEMORY



[Altera Corp: Cyclone II Handbook]

- FIFOs and Dual-Ported Memory, is commonly used
- Does not require external synchronization
- System design must ensure FIFO does not overflow
- Gray Coding used for address transfer

PUSH SYNCHRONIZER



[Ran Ginosar: Fourteen Ways to Fool Your Synchronizer]

› Example of a handshaking / FSM method for multi-bit cross-domain transfer

PUSH SYNCHRONIZER CODE

```
-- TRANSMITTER
if rising_edge(tx_clock) then
  A2 <= A1; A1 <= A;
  A3 <= A2; F <= not A3 and A2;
  case (tx_fsm_state) is
    when idle =>
      if (V = '1') then
        tx_fsm_state <= req;
        R            <= '1';
      end if;
    when req =>
      if (A2 = '1') then
        tx_fsm_state <= waiting;
        R            <= '0';
      end if;
    when waiting =>
      if (A2 = '0') then
        tx_fsm_state <= idle;
      end if;
    when others =>
      tx_fsm_state <= idle;
      R            <= '0';
  end case;
end if;
```

```
-- RECEIVER (input R, output A)
if rising_edge(rx_clock) then
  R2 <= R1; R1 <= R;
  R3 <= R2; D <= not R3 and R2;
  case (rx_fsm_state) is
    when idle =>
      if (R2 = '1') then
        rx_fsm_state <= ack;
        A            <= '1';
      end if;
    when ack =>
      if (R2 = 0') then
        rx_fsm_state <= idle;
        A            <= '0';
      end if;
    when others =>
      rx_fsm_state <= idle;
      A            <= '0';
  end case;
end if;
```

CLOCK DOMAINS SUMMARY

- Passing signals between clock-domains is not trivial.

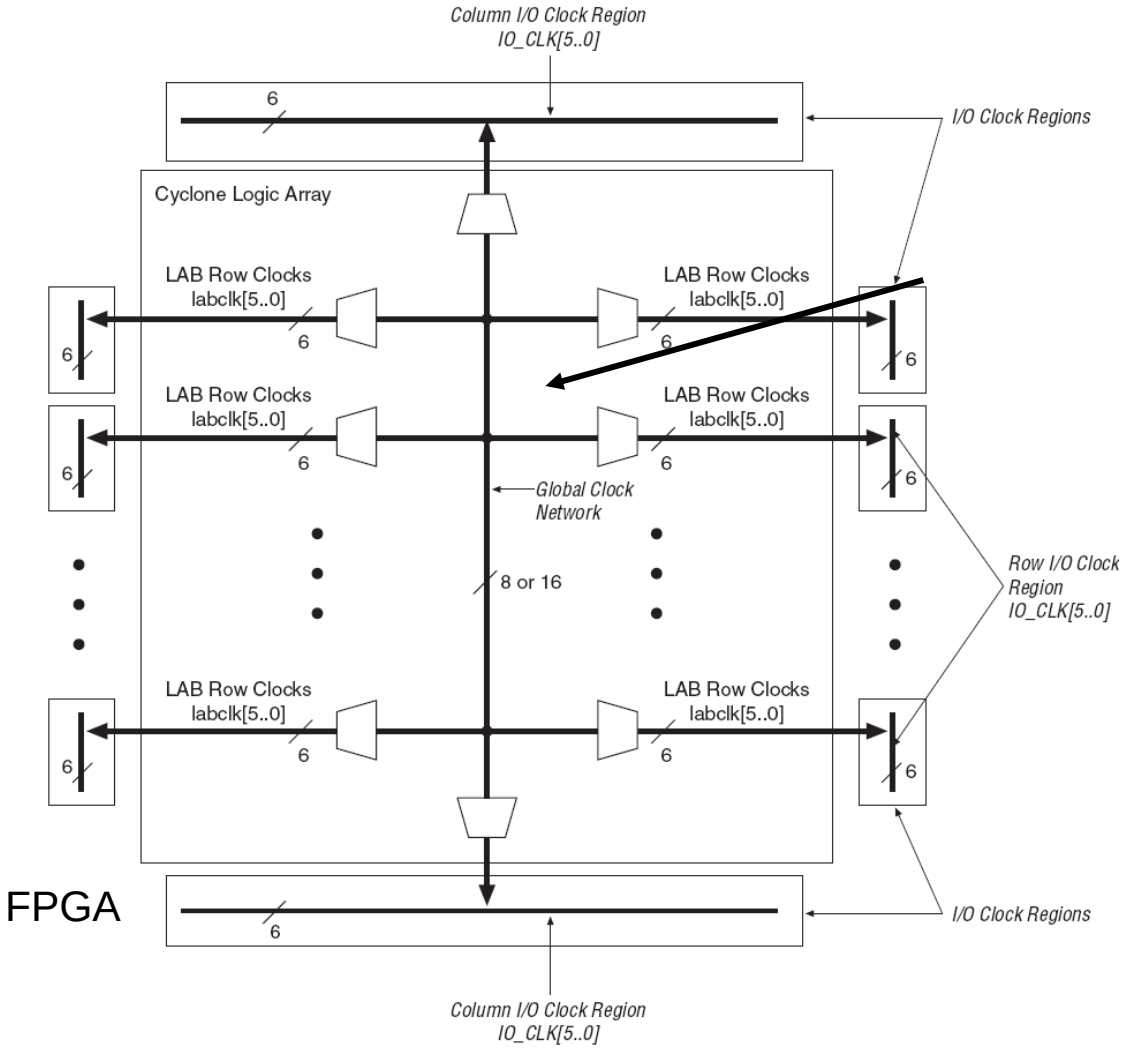
- Single signals: Use double flopping
- Multiple signals: Use FIFO / DP RAM / FSM etc.

- If the clock phase between the clock domains is well defined, then a simple phase shift between the two may be enough

- Going from a fast to a slow clock domain, the signal must be held stable for one destination clock cycle

Clocks in the FPGA

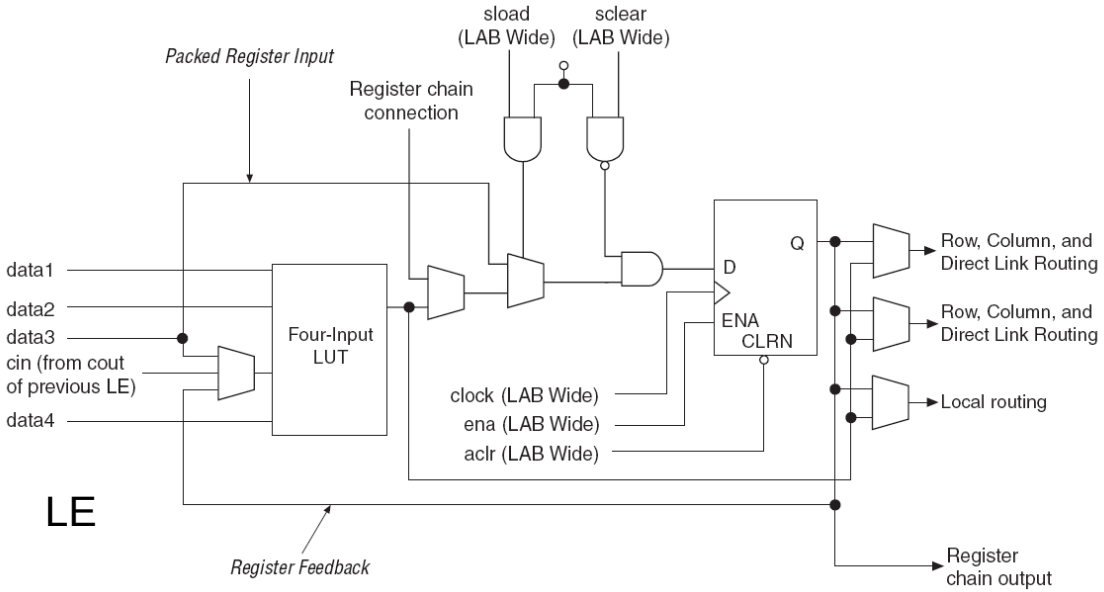
CLOCK DISTRIBUTION IN CYCLONE II

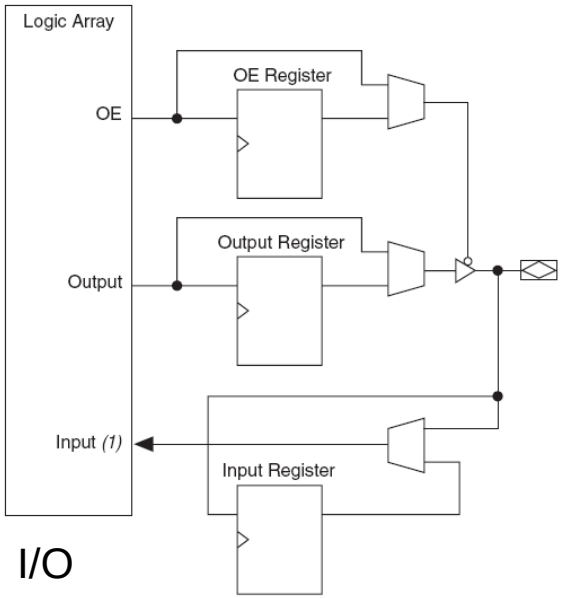


[Altera Corp: Cyclone II Handbook]

- 8/16 Global clock nets
- Max 6 clock nets per LAB (Logic Array Block)
- Dedicated Clock Inputs

CLOCKS IN LOGIC- / IO ELEMENTS

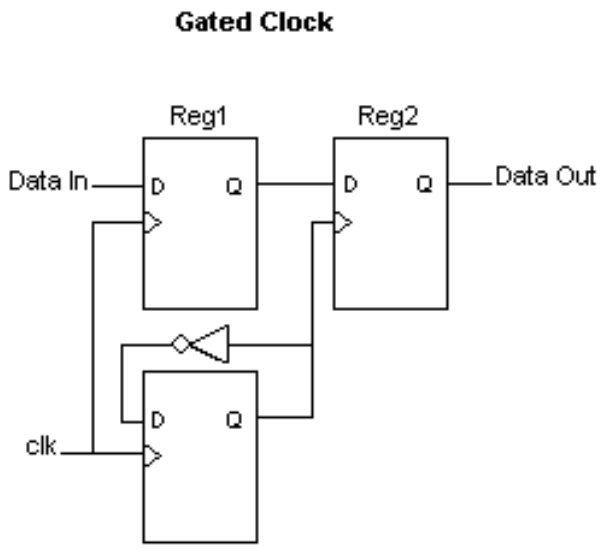




[Altera Corp: Cyclone II Handbook]

› Clock enable per I/O cell and per LE
› Different Input- / Output clocks allowed within an I/O cell

GATED CLOCKS (1)



[Altera Corp: Troubleshooting Internal Hold Violations]

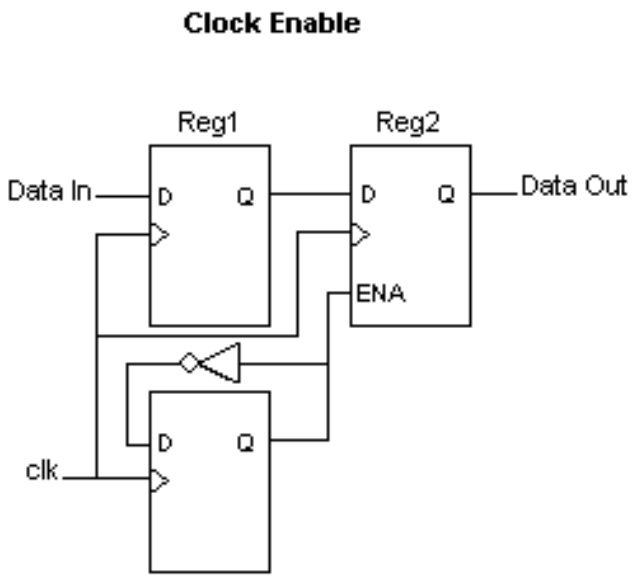
```
-- Gated Clock - BAD!
Process(clk)...
if rising_edge(clk) then
   clk2 <= not clk2;
   s1 <= DataIn;
end if;

-- Clk Enable, rising edge
Process(clk2)...
if rising_edge(clk2) then
 DataOut <= s1;
end if;
```

Problem?

- Gated clocks use normal inter-connect instead of global clock nets
- Unpredictable clock phase

GATED CLOCKS (2)



[Altera Corp: Troubleshooting Internal Hold Violations]

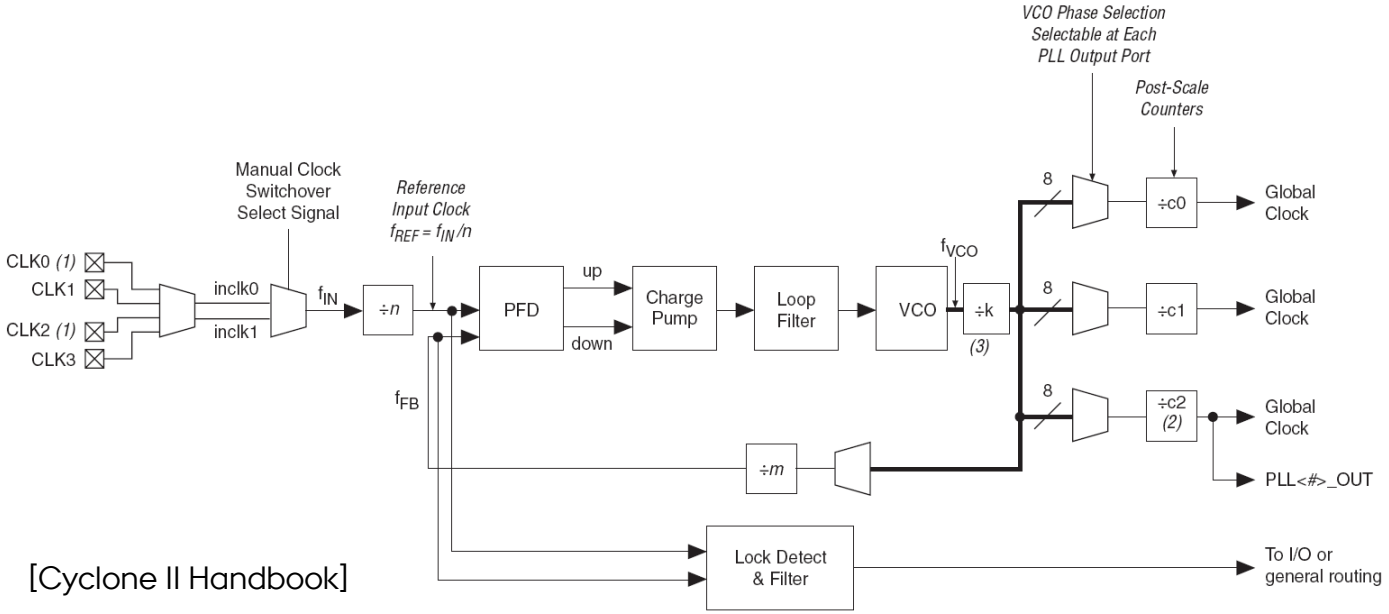
```
-- Clk Enable, rising edge
process(clk)...
if rising_edge(clk) then
 s1 <= DataIn;
 clk_en <= not clk_en;
 if clk_en = '1' then
  DataOut <= s1;
end if;

-- Waiting for a rising edge
if rising_edge(clk) then
 event_last <= event;
 if (event = '1' and event_last = '0') then
   DataOut <= DataIn;
  end if;
end if;
```

› Use *Clock Enable* instead of gated clocks
› Architecure supports *Clock Enable*

PLLS I CYCLONE II

Figure 2–16. Cyclone II PLL *Note (1)*



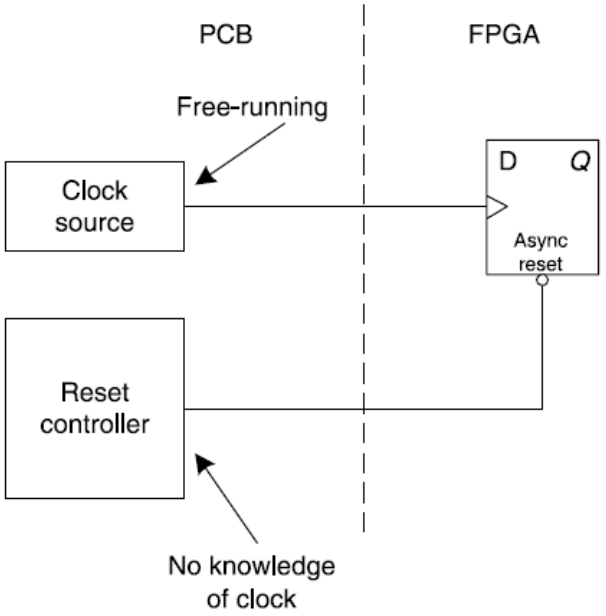
[Cyclone II Handbook]

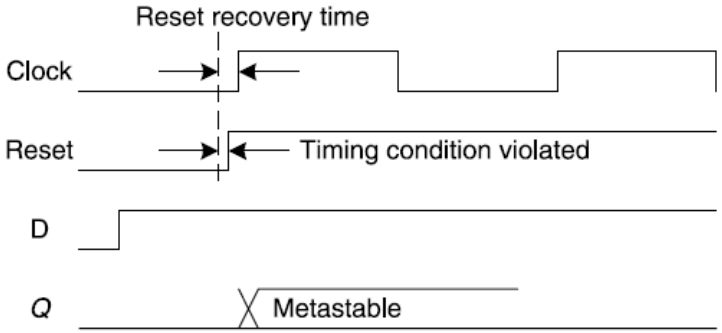
› The PLL multiplies/divides and phase-shifts the input frequency
› The PLL uses dedicated clock inputs
› Output is connected to global clock nets
› Note! Simulation Resolution > VCO frequency

CLOCKS IN AN FPGA SUMMARY

- Only a limited number of low-skew clock nets exist
- Avoid gated clocks in FPGAs
- Use clock enable signals instead.
- Supported by the architecture
- Synchronous to the main clock
- Use PLLs to generate derived clocks and to control the clock phase

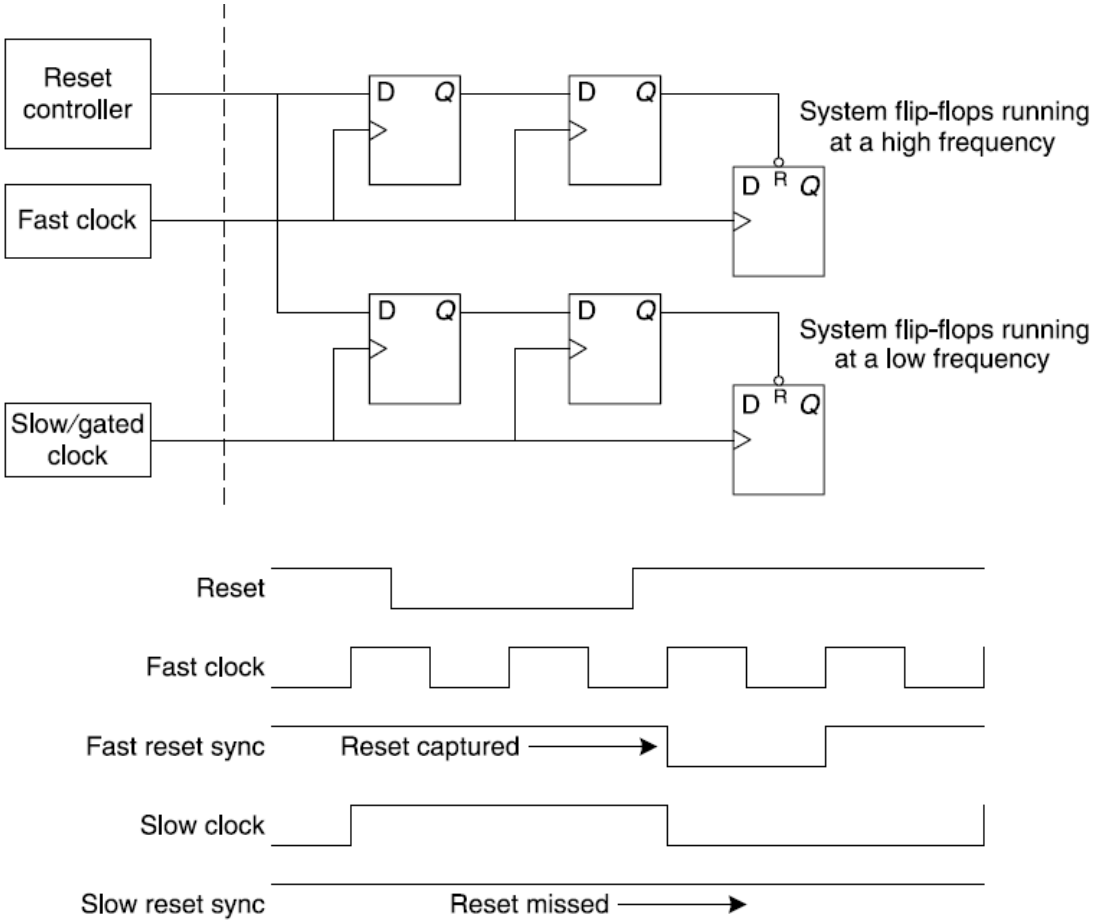
RESETS





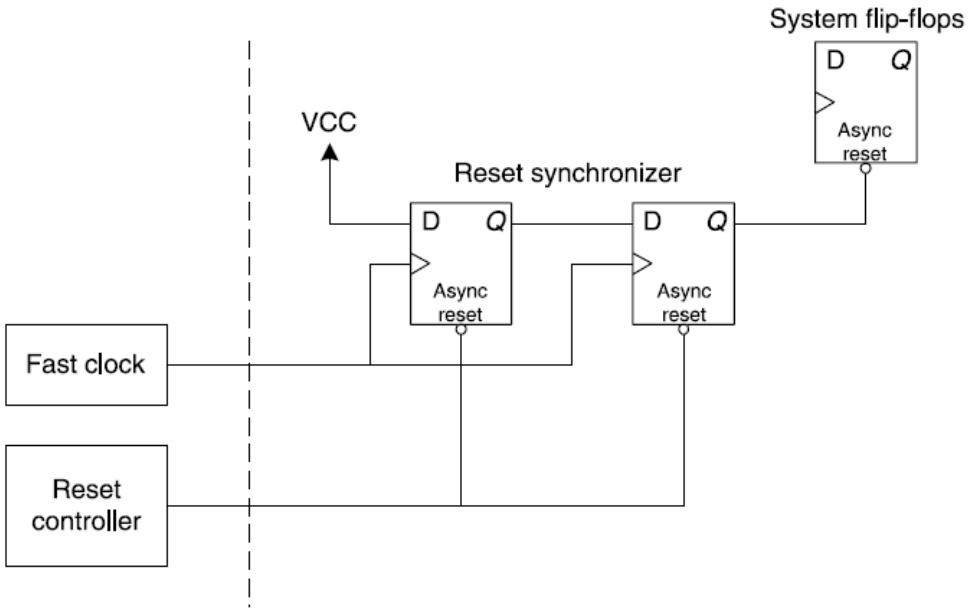
› Asynchronous reset signals must be synchronized to their respective clocks to avoid timing violations

SYNCHRONOUS RESET



› If the reset pulse is too short, it will be missed

ASYNC- / SYNC RESET SOLUTION



› Suggested solution provides asynchronous assertion and synchronous de-assertion of Reset

RESETS SUMMARY

- Asynchronous Resets must be synchronized to the clock domain where it is being used.
- Resets must be double flopped when crossing a clock domain => One Reset per clock domain