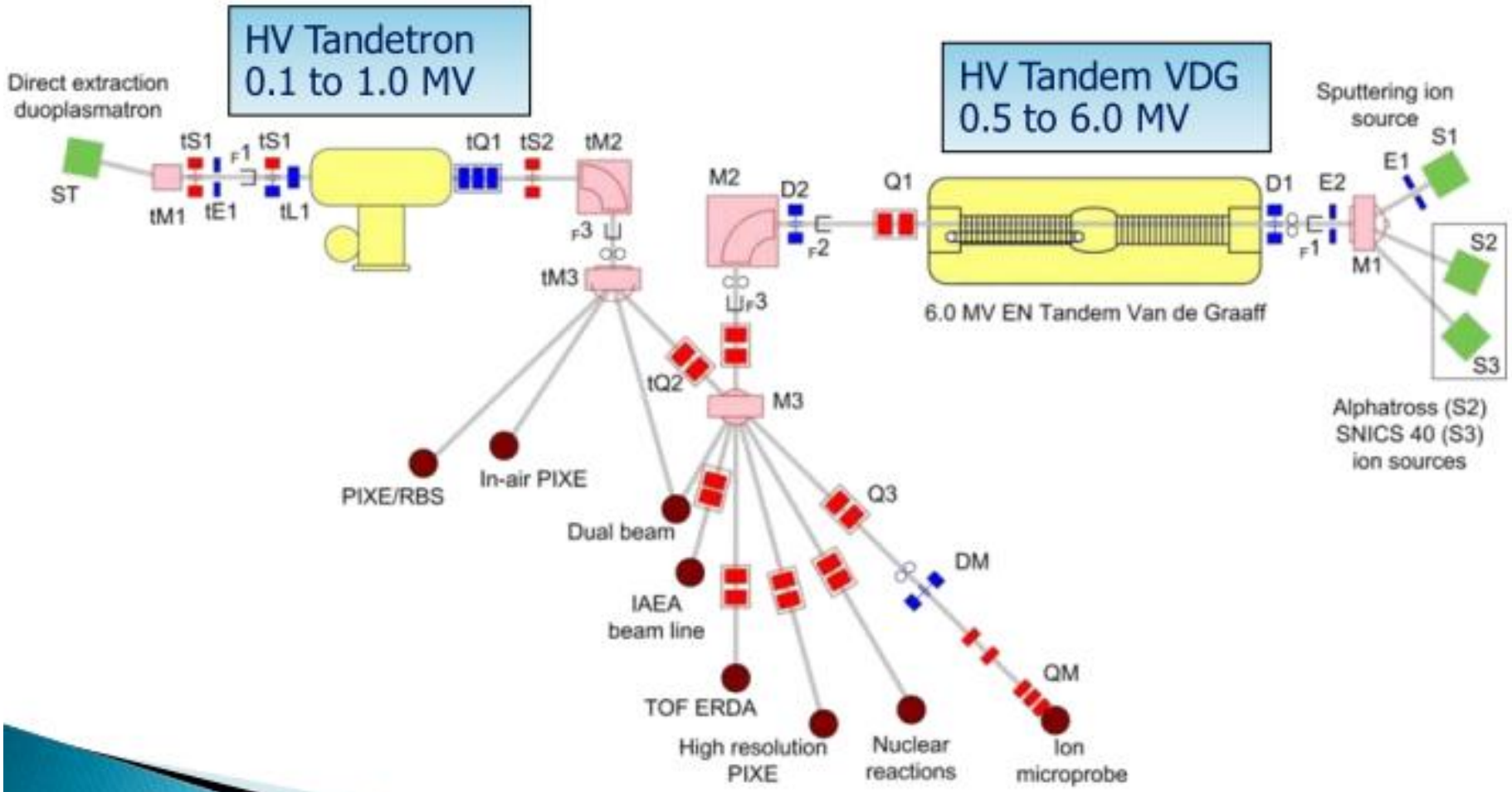
AARHUS
UNIVERSITY
SCHOOL OF ENGINEERING

PETER HØGH
MIKKELSEN
2. JANUARY, 2017

DESIGN OF SYSTEMS ON PROGRAMMABLE CHIPS

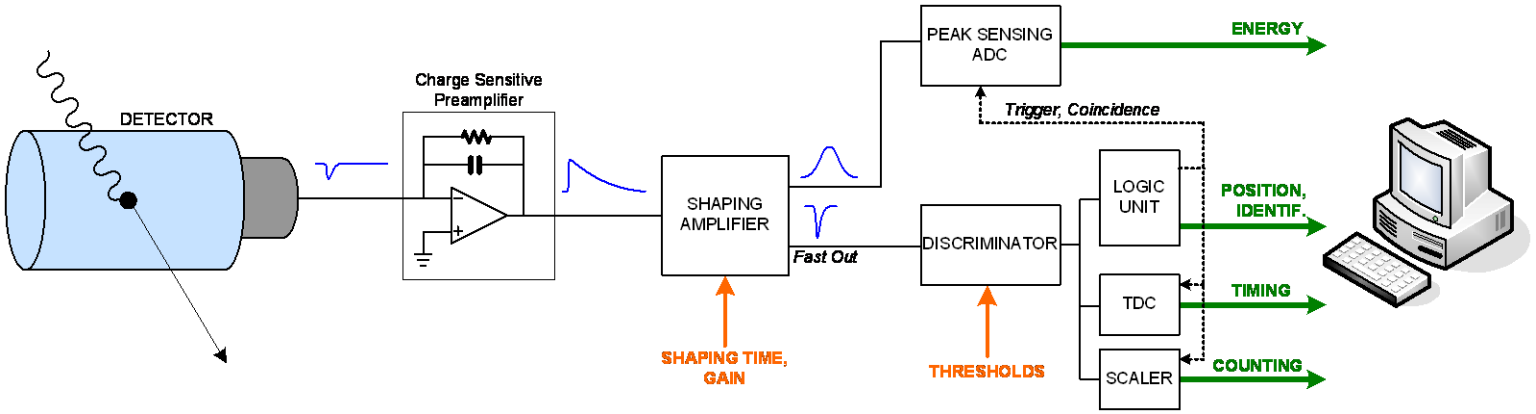
INTRODUCTION

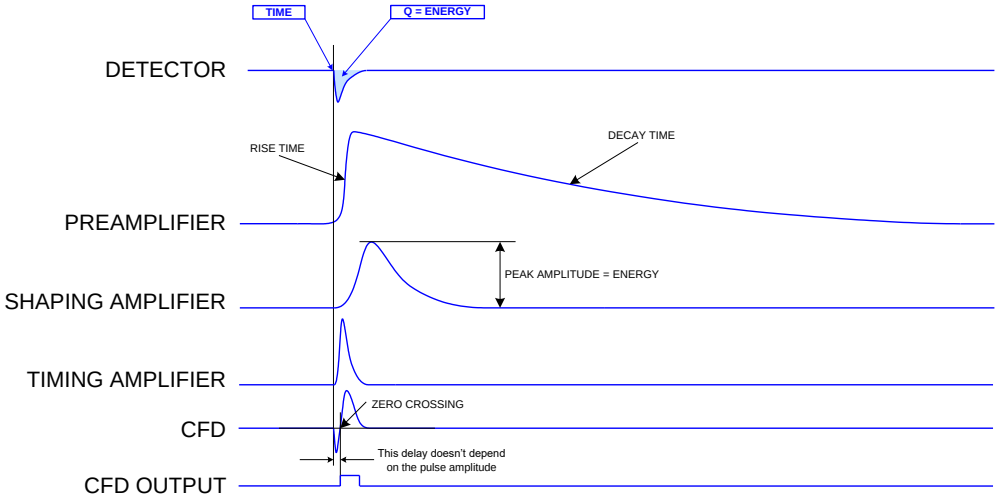
PHYSICS DATA ACQUISITION



[Cosic, Donny Domagoj: FPGA Based Data Acquisitions Systems, DAQ Workshop 2011]

PHYSICS DAQ: OLD APPROACH



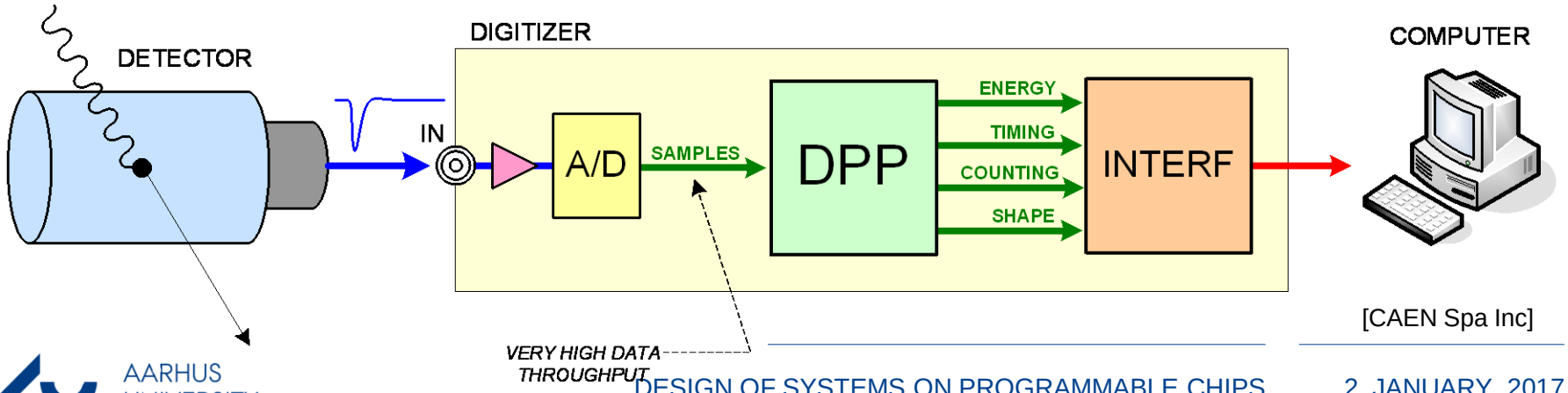


- Typically used with semiconductor detectors (Si, Ge)
- The preamp. output signal is rather slow (typ. decay time = 50us)
- Very high energy resolution (good S/N ratio)

[CAEN Spa Inc]

PHYSICS DAQ: DIGITAL APPROACH

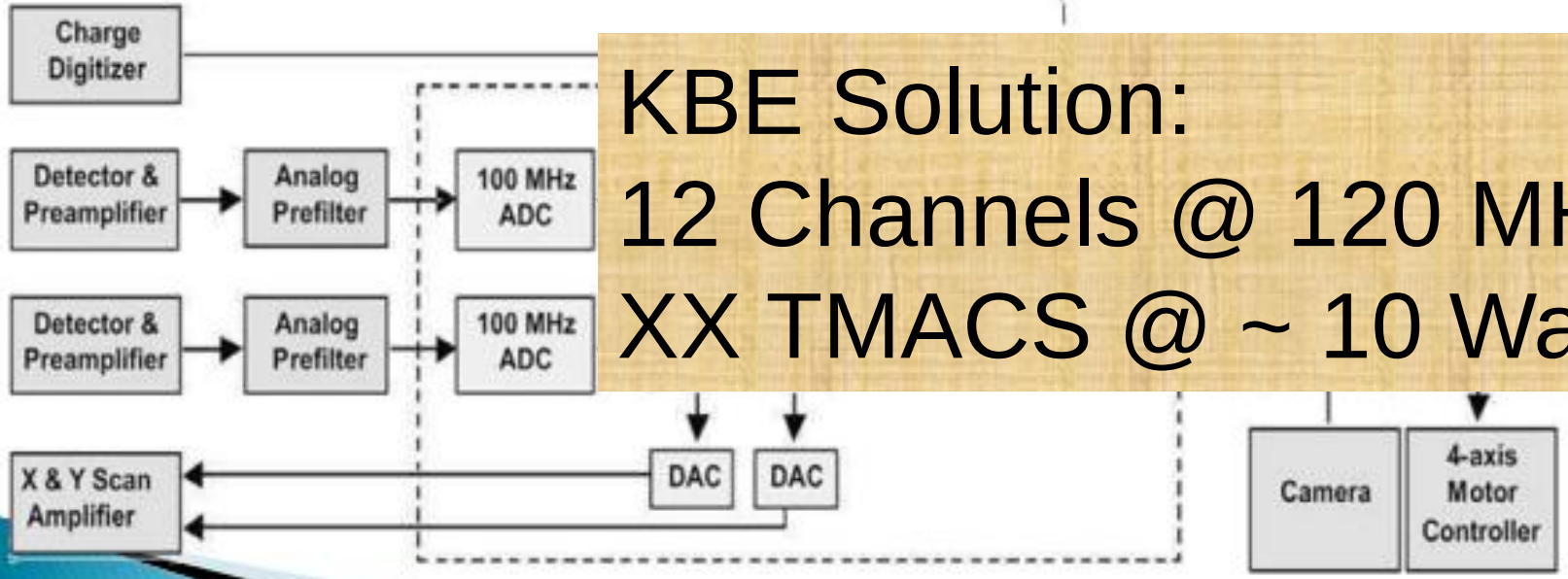
- One single board can do the job of several analog modules
- Full information preserved: *A/D conversion as early as possible, data reduction as late as possible*
- Reduction in size, cabling, power consumption and cost per channel
- High reliability and reproducibility
- Flexibility (different digital algorithms can be designed and loaded at any time into the same hardware)



[CAEN Spa Inc]

PHYSICS DAQ: SOLUTION

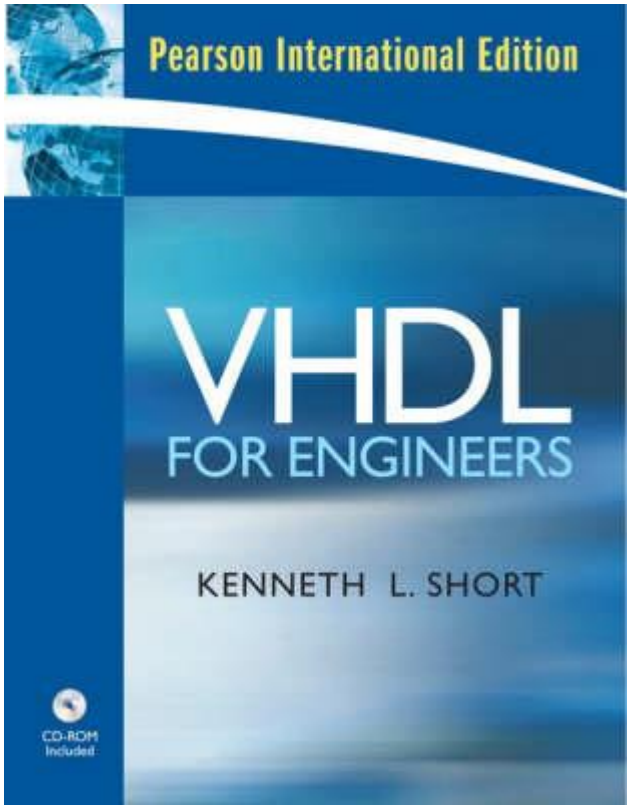
- Xilinx Virtex 4 FPGA
- 14bit 105 MHz ADC (2x)
- 14bit 160 MHz DAC (2x)
- PCI Interface



KBE Solution:
12 Channels @ 120 MHz:
XX TMACS @ ~ 10 Watt

[Cosic, Donny Domagoj: FPGA Based Data Acquisitions Systems, DAQ Workshop 2011]

BOOK



”VHDL for Engineers”
By
Kenneth L. Short

+

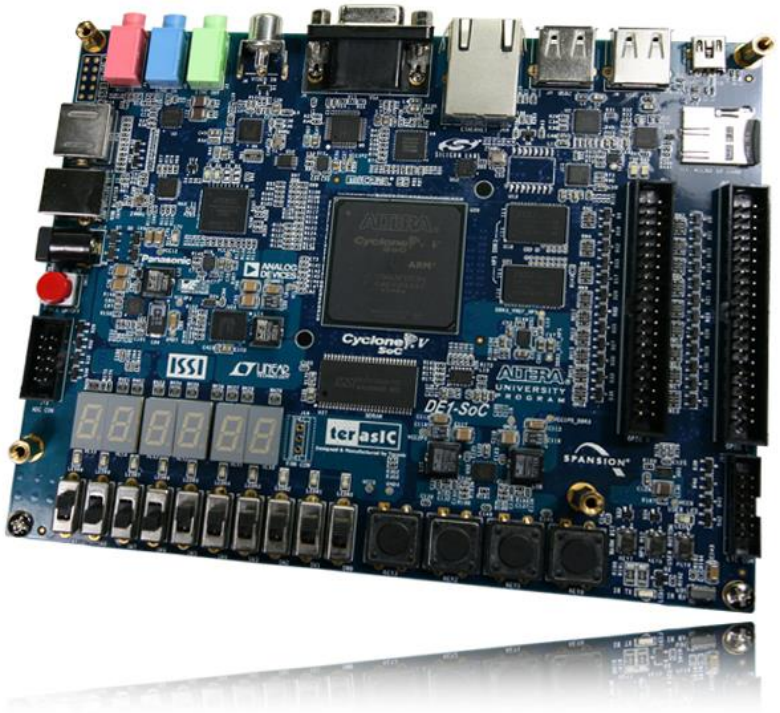
Notes on Black Board

DEVELOPMENT BOARD

Cyclone V SoC
Dual-core ARM Cortex-A9 (HPS)
85K Logic Elements
4,450 Kbits embedded memory

64MB (32Mx16) SDRAM on FPGA
1GB (2x256Mx16) DDR3 on HPS
Micro SD Card Socket on HPS

Two Port USB 2.0 Host
USB to UART
10/100/1000 Ethernet
24-bit Audio CODEC
500 KSPS 12-bit ADC



LÆRINGSMÅL

› Implementere programmer for FPGA'er, skrevet i VHDL
› Anvende modelsim og test benches til at udføre simulation af VHDL design
› Redegøre for begreber som: clock domæner, clock skew, pipelining, PLL- og memory komponenter
› Anvende soft cores til opbygning af et SoC (System On Chip) system
› Implementere C programmer til afvikling på SoC
› Implementere signal behandlings algoritmer i VHDL

SYLLABUS

- Repetition af basale VHDL begreber
- Test benches og assertions
- Anvendelse af memory komponenter i FPGA
- Design Constraints
- Clocks og Timing
- SOPC Builder (generering af system)
- Arkitektur for Altera FPGA
- Anvendelse af signal behandlings algoritmer i VHDL
- Systembusser (Memory Mapped + Streaming)

EKSAMEN

› Prøveform:
› 3 x Multiple-Choice med hjælpemidler (3x10%)
› Afsluttende opgave 2-3 studerende (70%)

› Bedømmelsesform:
› 7-trins skala ekstern censur