



3.3.Pin Descriptions

Bus Interface Pins					
Pin Name	I/O	Туре	Descriptions		
			Select the interface mode		
			IM2 IM1 IM0 Interface		
			0 0 0 MIPI-DBI Type B 24-bit bus (DB_EN = 1)		
		Digital Input	0 0 0 MIPI-DBI Type B 18-bit bus (DB_EN = 0)		
IM2, IM1, IM0	ı		0 0 1 MIPI-DBI Type B 9-bit bus		
			0 1 0 MIPI-DBI Type B 16-bit bus		
			0 1 1 MIPI-DBI Type B 8-bit bus		
			1 0 1 MIPI-DBI Type C Option 1 (3-line SPI)		
			1 1 0 MIPI DSI		
			1 1 1 MIPI-DBI Type C Option 3 (4-line SPI)		
			Reset input signal		
RESX	I	Digital Input	Initialize the chip with a low input. Be sure to execute a power-on		
			reset after supplying power.		
			DBI Type B: Chip select input signal		
		Digital Input	Low: the chip is selected and accessible		
CSX	I		·		
			High: the chip is not selected and not accessible		
			Fix to IOVCC or DGND level when not in use.		
		Digital Input	DBI Type B: Data/Command Selection pin		
D/CX	Ī		Low: Command		
B/OX	•		High: Parameter		
			Fix to IOVCC or DGND level when not in use.		
			DBI Type B: WRX pin, serves as a write signal		
		Digital Input	DBI Type C: SCL pin as Serial Clock when operates in the serial		
WRX/SCL			interface		
			Fix to IOVCC or DGND level when not in use.		
			DBI Type B: serve as a read signal		
RDX	I	Digital Input	Fix to IOVCC or DGND level when not in use.		
			DBI Type C		
SDA	I/O	Digital I/O	DIN/SDA: serial data input/output bi-direction pin		
			Fix to IOVCC or DGND level when not in use.		
		Digital Output	DBI Type C		
SDO	0		SDO: Serial data output		
			Leave the pin open when not in use.		
TE		B. I	Serve as a TE (Tearing Effect) output signal		
TE	0	Digital Output	Leave the pin open when not in use.		
CABC_PWM	0	Digital Output	The PWM frequency output for LED driver control		





			Leave the pin open when not in use.	
MIPI_CLOCK_P	1	MIPI-DSI Input	DSI	
			Positive polarity of low voltage differential	clock signal
		mpat	Leave the pin open when not in use.	
		MIPI-DSI Input	DSI	
MIPI_CLOCK_N	ı		Negative polarity of low voltage differential	clock signal
			Leave the pin open when not in use.	
		MIPI-DSI I/O	DSI	
MIPI_DATA_P	I/O		Positive polarity of low voltage differential	data signal
			Leave the pin open when not in use.	
		MIPI-DSI	DSI	
MIPI_DATA_N	I/O	I/O	Negative polarity of low voltage differential	data signal
		"	Leave the pin open when not in use.	
	I/O	Digital I/O	Interface Mode	Data Pin in Use
			MIPI-DBI Type B 24-bit bus (DB_EN = 1)	DB [23:0]
			MIPI-DBI Type B 18-bit bus (DB_EN = 0)	DB [17:0]
			MIPI-DBI Type B 16-bit bus	DB [15:0]
DB [23:0]			MIPI-DBI Type B 9-bit bus	DB [8:0]
			MIPI-DBI Type B 8-bit bus	DB [7:0]
			MIPI-DPI 24-bit	DB [23:0]
			MIPI-DPI 18-bit	DB [17:0]
			MIPI-DPI 16-bit	DB [15:0]
			Fix to DGND level when not in use.	
VSYNC		Digital Input	DPI: Frame synchronizing signal	
VOTNO	1		Fix to DGND level when not in use.	
HSYNC		Digital Input	DPI: Line synchronizing signal	
TIGTING	<u>'</u>		Fix to DGND level when not in use.	
ENABLE		Digital Input	DPI: A data ENABLE input signal	
LIVADLE	'	Digital Input	Fix to DGND level when not in use.	
DOTCLK		Digital Input	DPI: Dot clock signal	
DOTOLN	'		Fix to IOVCC level when not in use.	

LCD Driving Signals			
Pin Name	I/O	Туре	Descriptions
S960~S1	0	Source Output	Source output voltage signals applied to the liquid crystal Leave the pin open when not in use.





			Gate driver output pins
G480~G1	0	Gate Output	VGH: the level selecting gate lines
G400~G1			VGL: the level not selecting gate lines
			Leave the pin open when not in use.
VCOM	0	I CD Output	The common voltage in DC VCOM driving
VCOIVI		LCD Output	The voltage range is set between -2V to 0V.
VGS	i	Dower CND	Reference level for grayscale generating circuit
	I Power GND	Fix to GND level	

Charge-pump and Regulator Circuit				
Pin Name	I/O	Туре	Descriptions	
		Charge Pump Output	Power supply for the source driver and VCOM driver. Input voltage	
DDVDH	0		from the set-up circuit (4.5 to 6V).	
		Output	Connect to a stabilizing capacitor between DDVDH and GND.	
		Charge Pump	Power supply for the source driver and VCOM driver. Input voltage	
DDVDL	0	Output	from the set-up circuit (-6 to -4.5V).	
		Output	Connect to a stabilizing capacitor between DDVDL and GND.	
VGH	0	Charge Pump	Power supply for the gate driver	
VGIT		Output	Connect to a stabilizing capacitor between VGH and GND.	
VGL	0	Charge Pump	Power supply for the gate driver	
VGL		Output	Connect to a stabilizing capacitor between VGL and GND.	
VCL	0	Charge Pump	VCL = -VCI ~ -2	
VCL		Output	Connect to a stabilizing capacitor between VCL and GND.	
		LDO Output	MIPI DSI core power pad	
MIPI LDO	0		Connect to a stabilizing capacitor between MIPI_LDO and GND	
WIIFI_LDO			when operating in the MIPI DSI Interface.	
			Leave the pin open when not in use.	
C52A, C52B	0		Capacitor connection pins for the step-up circuit 1	
C52A, C52B		Analog Output	Connect to a stabilizing capacitor between C51A and C51B.	
C41A, C41B			Connect to a stabilizing capacitor between C52A and C52B.	
C11A, C11B			Connect to a stabilizing capacitor between C41A and C41B.	
C12A, C12B			Connect to a stabilizing capacitor between C11A and C11B.	
012A, 012B			Connect to a stabilizing capacitor between C12A and C12B.	
C21A, C21B	0	Analog Output	Capacitor connection pins for the step-up circuit 2.	
		O Analog Output	Connect to a stabilizing capacitor between C21A and C21B.	

Power Pads				
Pin Name	I/O	Туре	Descriptions	





			A supply voltage to the analog circuit. Connect to an external power
VCI	Р	Power Supply	supply of 2.5 ~ 3.3V.
			Connect to a stabilizing capacitor between VCI and GND.
IOVCC	Р	Power Supply	A supply voltage to the digital circuit. Connect to an external power
10,000	'	1 Ower Supply	supply of 1.65 ~ 3.3V.
VDD (VCORE)		O Power Supply	Internal logic voltage output
VDD (VCORE)			Connect to a stabilizing capacitor between VDD and GND.
			Ground for the internal logic: DGND = 0V
DGND	Р	Power GND	When using COG, connect to GND on the FPC to prevent
			noise.
			AGND for the analog side: AGND = 0V
AGND	Р	Power GND	When using COG, connect to GND on the FPC to prevent
			noise.

Test Pads				
Pin Name	I/O	Type	Descriptions	
DUMAN	DUMAN	-	Dummy pad	
DUMMY	-		Leave the pin open when not in use.	
TC [0.0]		I -	Test pins, these pins are internal weak pull low.	
TS [2:0] I			Leave the pin open when not in use.	
TESTP	1.	Power GND	Test pins.	
			Fix to GND level	