4. System Interfaces

The ILI9488 supports MIPI DBI, DPI, and DSI. DBI supports (8-/9-/16-/18-/24-bit interface) Parallel Interface (Type B) and Serial Interface (Type C). The interface mode can be selected by IM [2:0] pins, as shown in Table 3 below.

Table 3: Interface Selection

IM2	IM1	IM0	Interface	Data Pins in Use	
				Command/Parameter	GRAM
0	0	0	DBI Type B 24-bit (DB_EN = 1)	DB [7:0]	DB [23:0]: 24-bits Data
0	0	0	DBI Type B 18-bit (DB_EN = 0)	DB [7:0]	DB [17:0]: 18-bits Data
0	0	1	DBI Type B 9-bit	DB [7:0]	DB [8:0]: 9-bits Data
0	1	0	DBI Type B 16-bit	DB [7:0]	DB [15:0]: 16-bits Data
0	1	1	DBI Type B 8-bit	DB [7:0]	DB [7:0]: 8-bits Data
1	0	1	DBI Type C Option 1 (3-line SPI)	SDA/SDO	
1	1	0	DSI	MIPI_DATA_P, MIPI_DATA_N, MIPI_CLOCK_P, MIPI_CLOCK_N	
1	1	1	DBI Type C Option 3 (4-line SPI)	SDA/SDO	

4.1. DBI Type B Parallel Interface

The ILI9488 includes an Index Register (IR), which stores the index data of internal Control Register (CR) and GRAM. The chip-select D/CX (active low) is used to enable or disable the ILI9488 chip. The RESX (active low) is an external reset signal, the WRX is a parallel data write strobe, the RDX is a parallel data read strobe, and DB [23:0] is a parallel data bus.

The ILI9488 latches the input data at the rising edge of the WRX signal. The D/CX is the signal for data/command selection. When D/CX = 1, DB [23:0] bits are RAM data or command parameters. When D/CX = 0, DB [23:0] bits are commands. The DBI Type B bi-directional interface is used for communication between the MCU controller and the LCD driver chip. The selection and operation of the parallel interface is shown in Table 4.

Table 4: DBI Type B Parallel Interface

IM2	IM1	IM0	MPU-Interface Mode	WRX	RDX	D/CX	Function
0	0	0	DBI Type B 24-bit (DB_EN = 1)	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	0	0	DBI Type B 18-bit (DB_EN = 0)	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	0	1	DBI Type B 9-bit	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	1	0	DBI Type B 16-bit	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data
0	1	1	DBI Type B 8-bit	↑	"H"	"L"	Write command code
				"H"	↑	"H"	Read internal status
				↑	"H"	"H"	Write parameter or display data
				"H"	↑	"H"	Read parameter or display data

4.1.1. Write Cycle Sequence

The WRX signal is driven from high to low then pulled back to high during the write cycle. The host processor provides information while the display module captures the information from the host processor on the rising edge of the WRX. Figure 1 below shows the write cycle of the DBI Type B interface.

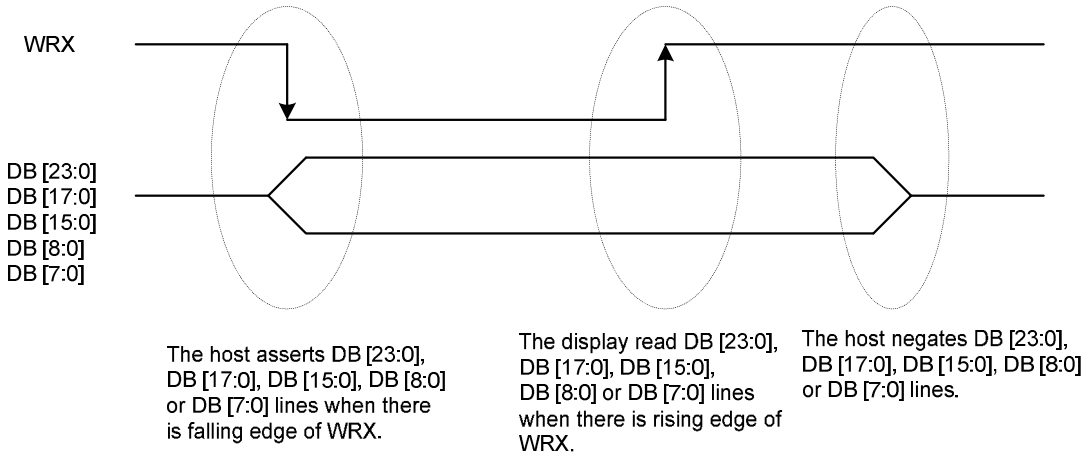

Figure 1: DBI Type B Write Cycle

Note: WRX is an unsynchronized signal that can be terminated when not being used.

When the D/CX signal is driven to low level, the input data on the interface is interpreted as command information. The D/CX signal can also be pulled to high level when the data is RAM data or command parameter.

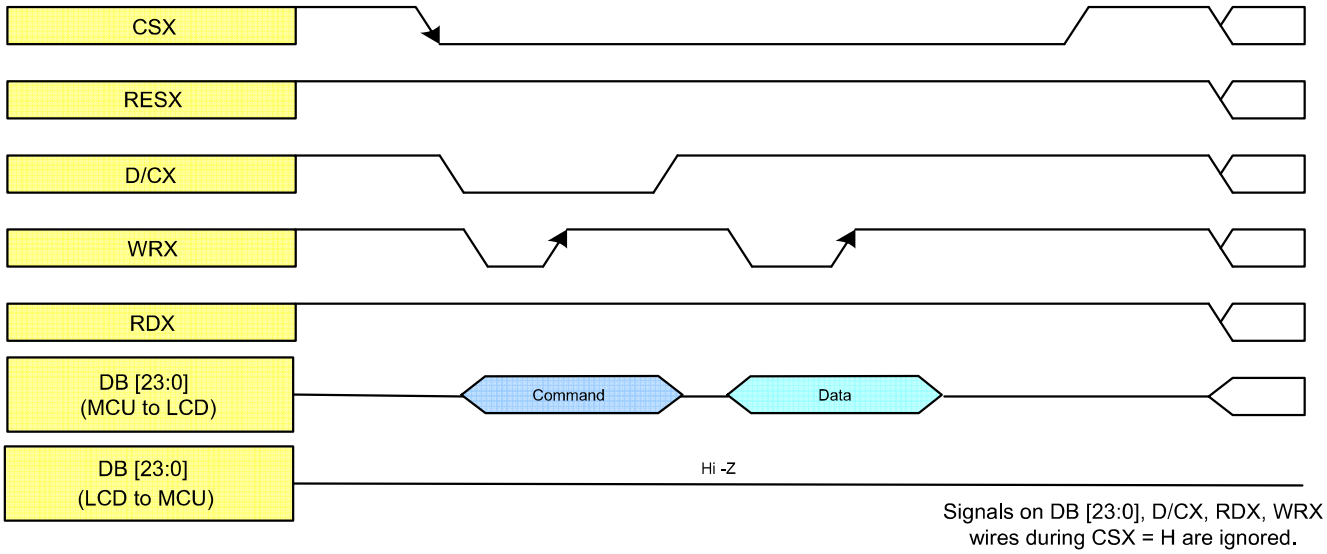

Figure 2: DBI Type B Write Cycle Sequence

4.1.2. Read Cycle Sequence

The RDX signal is driven from high to low and then pulled back to high during the read cycle. The display module provides information to the host processor while the host processor reads the display module information on the rising edge of the RDX signal. Figure 3 below shows the read cycle of the DBI Type B interface.

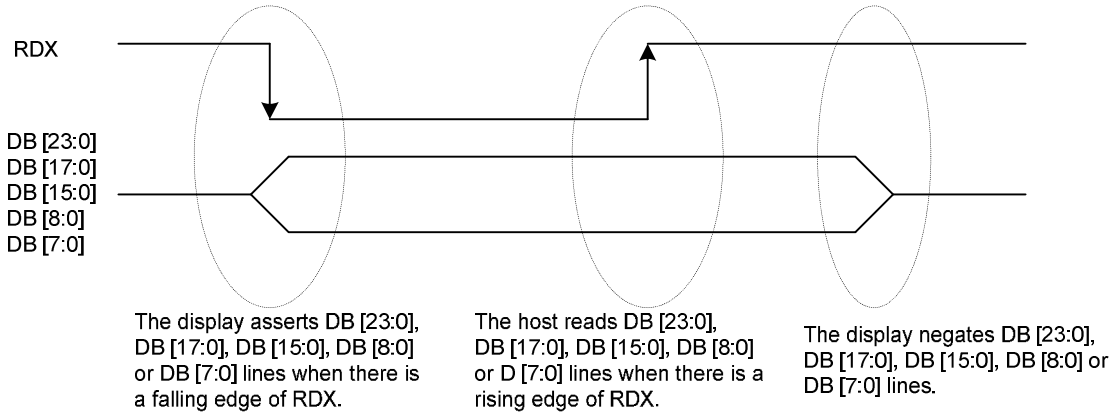

Figure 3: DBI Type B Read Cycle

Note: RDX is an unsynchronized signal that can be terminated when not being used.

When the D/CX signal is driven to the low level, the input data on the interface is interpreted as internal status or parameter data. The D/CX signal can also be pulled to a high level when the data on the interface is RAM data or a command parameter data.

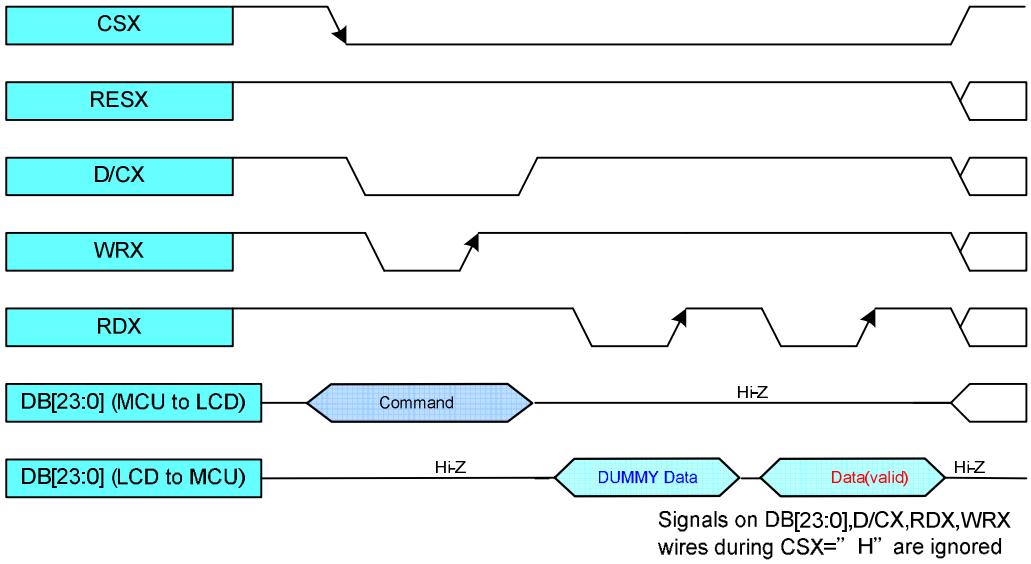

Figure 4: DBI Type B Read Cycle Sequence

Note: Read Data is only valid when the D/CX input is pulled high. If the D/CX signal is driven to low during the read cycle then the display information outputs will be High-Z.