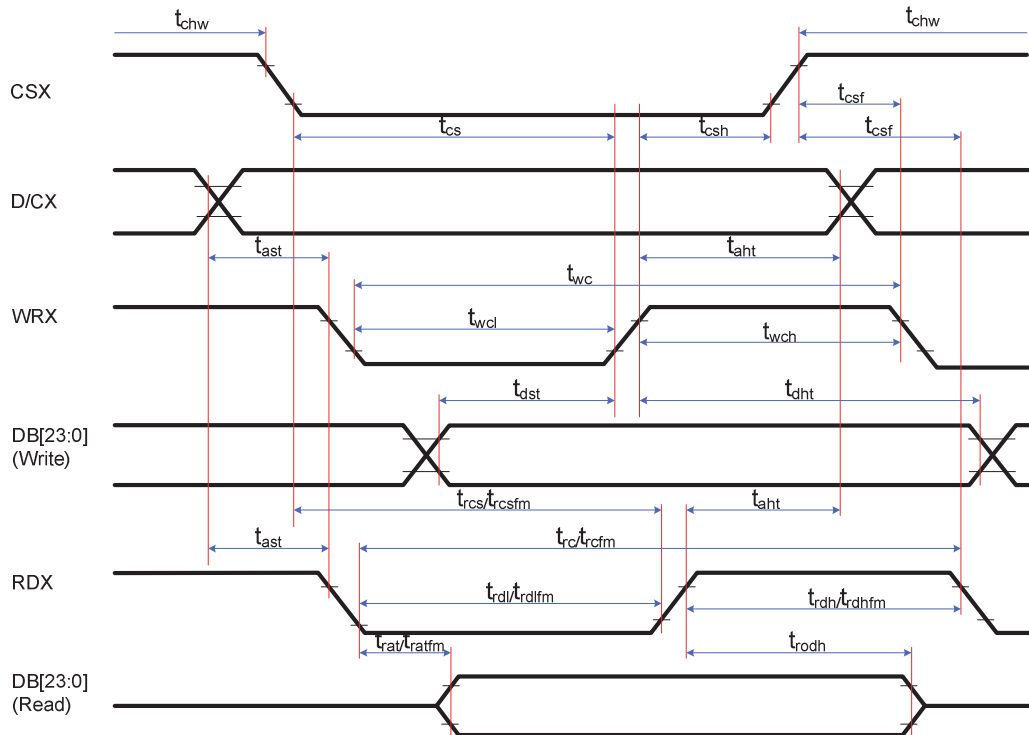


## 17.4. AC Characteristics

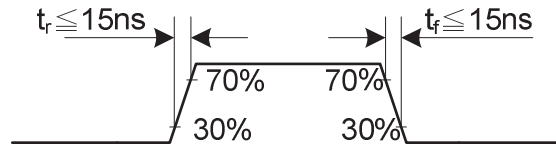
### 17.4.1. DBI Type B (Display Parallel 8-/9-/16-/18-/24-bit interface) Timing Characteristics



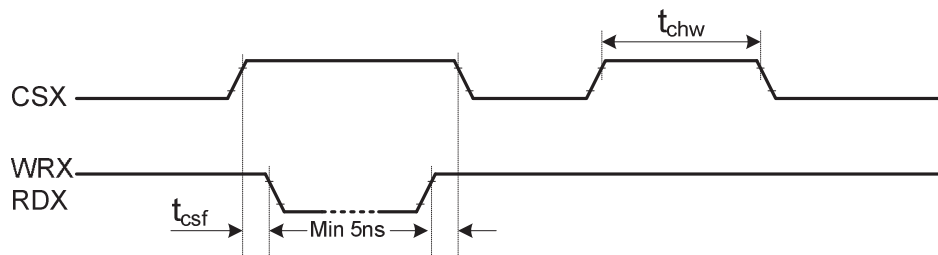
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	-
	that	Address hold time (Write/Read)	0	-	ns	-
CSX	tchw	CSX "H" pulse width	0	-	ns	-
	tcs	Chip Select setup time (Write)	15	-	ns	-
	trcs	Chip Select setup time (Read ID)	45	-	ns	-
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	-
WRX	tcsf	Chip Select Wait time (Write/Read)	0	-	ns	-
	twc	Write cycle	30	-	ns	-
	twrh	Write Control pulse H duration	15	-	ns	-
RDX (FM)	twrl	Write Control pulse L duration	15	-	ns	-
	trcfm	Read Cycle (FM)	450	-	ns	When read from Frame Memory
	trdhfm	Read Control H duration (FM)	90	-	ns	
RDX (ID)	trdlfm	Read Control L duration (FM)	355	-	ns	When read ID data
	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	For maximum, CL=30pF For minimum, CL=8pF
DB [23:0], DB [17:0], DB [15:0], DB [8:0], DB [7:0]	trdl	Read Control pulse L duration	45	-	ns	
	tdst	Write data setup time	10	-	ns	
	tdht	Write data hold time	10	-	ns	
DB [23:0] (Read)	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
DB [23:0] (Read)	trod	Read output disable time	20	80	ns	

**Notes:**

1.  $T_a = -30$  to  $70\text{ }^{\circ}\text{C}$ ,  $\text{IOVCC} = 1.65\text{V}$  to  $3.3\text{V}$ ,  $\text{VCI} = 2.5\text{V}$  to  $3.3\text{V}$ ,  $\text{AGND} = \text{DGND} = 0\text{V}$
2. Logic high and low levels are specified as 30% and 70% of  $\text{IOVCC}$  for input signals.
3. Input signal rising time and falling time:



4. The CSX timing:



5. The Write to Read or the Read to Write timing:

