

## CSE 3666 - Lab 7

Jonathan Ameri

```
# TODO:
# instantiate x and y registers, and adder
# reg_x =
# reg_y =
# adder =
# x_init and y_init are the load_data signal to reg_x and reg_y, respectively

reg_x = RegisterShiftLeft(x, x_init, load, x_en, clock, reset)
reg_y = RegisterShiftRight(y, y_init, load, y_en, clock, reset)
adder = Adder(adder_out, p, x)

# set up control signals for registers
@always_comb
def comb_regs():
    p_reset.next = load
    if (y & 1) == 0:
        p_en.next = 0
    else:
        p_en.next = 1
    # TODO:
    # set the p_en signal
    # p_en.next = ...
```

```
(myhdlenv) MacBook-Pro-4:lab6 jonathanameri$ python3 mul.py 17 36 202
load cnt prod x y p_en x_en y_en done
1 0 0000000000000000 000000000010001 00100100 0 1 1 0
0 1 0000000000000000 000000000100010 00010010 0 1 1 0
0 2 0000000000000000 0000000001000100 00001001 1 1 1 0
0 3 0000000001000100 0000000010001000 00000100 0 1 1 0
0 4 0000000001000100 0000000010001000 00000010 0 1 1 0
0 5 0000000001000100 0000000100010000 00000001 1 1 1 0
0 6 00000001001100100 0000010001000000 00000000 0 1 1 0
0 7 0000001001100100 0000100010000000 00000000 0 1 1 0
0 8 0000001001100100 0001000100000000 00000000 0 1 1 1
0 8 0000001001100100 0010001000000000 00000000 0 1 1 1
17 * 36 = 612
1 0 0000000000000000 000000000100100 11001010 0 1 1 0
0 1 0000000000000000 0000000001001000 01100101 1 1 1 0
0 2 0000000001001000 0000000010010000 00110010 0 1 1 0
0 3 0000000001001000 0000000100100000 00011001 1 1 1 0
0 4 0000000101101000 0000001001000000 00001100 0 1 1 0
0 5 0000000101101000 0000010010000000 00000110 0 1 1 0
0 6 0000000101101000 0000100100000000 00000011 1 1 1 0
0 7 0000101001101000 0001001000000000 00000001 1 1 1 0
0 8 0001110001101000 0010010000000000 00000000 0 1 1 1
0 8 0001110001101000 0100100000000000 00000000 0 1 1 1
36 * 202 = 7272
(myhdlenv) MacBook-Pro-4:lab6 jonathanameri$
```