CSE3666 Exam 2 Preparation

Read the announcement about Exam 2 in HuskyCT carefully.

This is not exactly a practice exam. The actual exam will be different.

Please study homework, labs, lecture slides and quizzes, probably before trying to solve problems here.

Solutions will not be provided. However, students can write their solutions collaboratively.

1. Design a combinational circuit that checks if a 4-bit input N is a prime number. The output G is 1 if and only if N is prime. Construct a truth table. Write a logical expression for G. Implement it in MyHDL.

```
@block
def isPrime(N, G):
```

2. A half adder is an adder without carry in. It adds two bits `a` and `b`, and produces sum `s` and carry `cout`. Implement a half adder in Python with MyHDL, using the Not, And2, Or2, and/or Xor2 gates that are already implemented. The interface of the gates is listed below, where `a` and `b` are inputs and `z` the output.

```
Not(z, a)                       And2(z, a, b)
Or2(z, a, b)                    Xor2(z, a, b)

@block
def HalfAdder1bit(a, b, s, cout):
    # s = a ^ b. Figure out the logic expression for cout
    # TODO

    return instances()
```

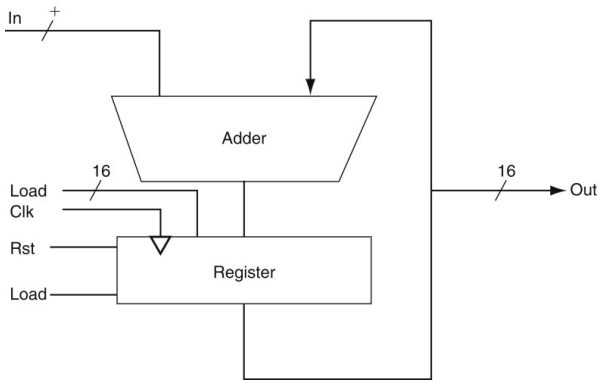
3. The setup time and hold time of the register is 2ns and 1ns, respectively. The propagation delay of the register is 3 ns. The propagation delay of the adder is 10 ns. Assume there is no delay on wire. In is kept steady at 100. Both load and reset signals are 0. The clock cycle time is 30ns. The clock changes from 0 to 1 at time t. At that moment, the input to register's value is 150 and has been steady for at least 5ns.

a) When does the Out signal change? What is its new value?

b) When does the output of Adder change? What is its new value?

c) When does the Out signal change again? What is its new value?

d) What is the minimum cycle time for the accumulator?



4. Operation of the multiplier. Study the homework questions.

5. Analyze the timing of the multiplier in lecture slides. The setup time and hold time of the register is 2ns and 1ns, respectively. The propagation delay of the register is 3 ns. The propagation delay of the adder is 10 ns. The propagation delay on the Control is 5 ns. The ALU/adder needs the signal from the Control module. There is no delay on wire. When the clock signal changes from 0 to 1 at time t, describe how the signals change in the circuit. The analysis is similar to questions in Q3.

6. Convert the following decimal numbers to binary numbers. Show results as normalized binary numbers. The exponent is in decimal. Keep only 5 bits after the binary point.

   2.71, 3.5

7. Convert the following binary numbers to decimal.

   $110.111, \quad 1.1101 \times 2^{10}, \; 1.1101 \times 2^{-2}$

8. Find the single precision representation of the numbers in Q6 and Q7. There is a tool in RARS (Tools/Floating Point Representation) that helps us understand floating point numbers.

9. Given a single/half precision number, find its normalized binary representation and decimal representation.

10. Single cycle processor. Given an instruction word (machine code), find out the value of all the signals. Note that the hardware module produces result even if the result is not needed. For example, the adder that computes the branch target address generates an address even if the instruction being executed is LW, SW, or R-type.

11. Explain how different hardware modules are used in the execution of instructions. For example, how is ALU is used in R-type, LW, SW, and BEQ instructions?

12. Explain how the processor can be improved to support more instructions. Study the homework questions and the questions in lecture slides.

    XOR, ANDI, ORI, ADDI, JAL, JALR, BNE, …

13. Analyze the execution of instructions in pipeline. Suppose the processor is executing the following instruction sequence and LW is located at address 0x0004 00C0.

    a) Draw the single-cycle pipeline diagram when LW is in the WB stage.
    b) Find out the PC in each pipeline stage, if PC is passed into the stage.
    c) Find out rd in each pipeline stage, if rd signal is present.

```
lw      x5, 20(x1)
sub     x10, x11, x12
add     x12, x13, x14
sw      x12, 30(x1)
beq     x12, x22, loop
```

14. Given the delay of major components, find the smallest cycle time of a pipelined processor. Study the example in slides.

    a) What if we also need to consider the delays on pipeline registers? For example, the propagation delay, hold time, and set up time of pipeline registers are 2ns, 1ns, and 3 ns, respectively.

15. Explain what structural hazards are and how they are handled in 5-stage pipeline.

16. Calculate CPI. For example, given the frequency and CPI of different instructions, compute average CPI.

17. Calculate CPU time. For example, calculate average CPI and then compute CPU time.

18. Apply Amdahl's law.

19. Compare performance of different processors. Compute speedup.