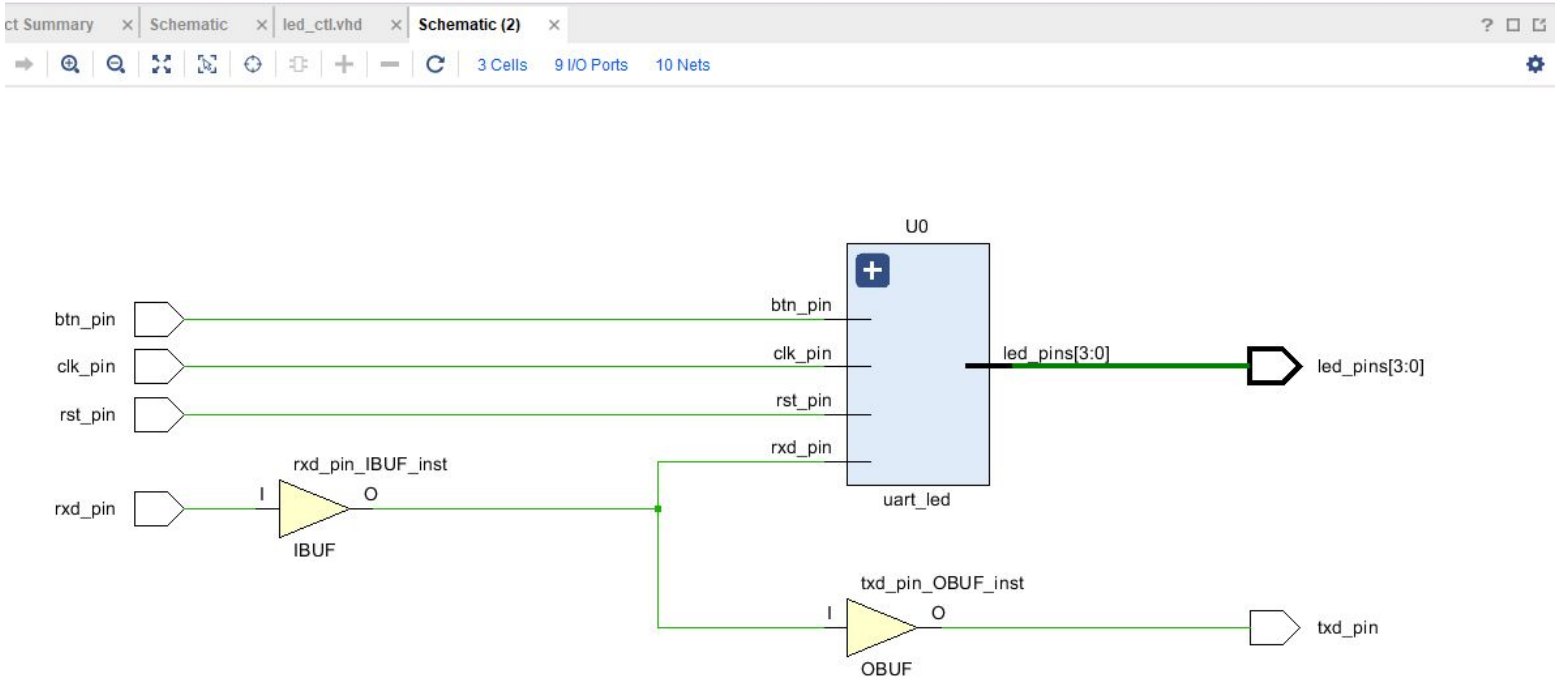
Contador ascendente y descendente por uart.


ct Summary
Schematic
led_ctl.vhd
Schematic (2)
3 Cells
9 I/O Ports
10 Nets
U0
btn_pin
clk_pin
rst_pin
rxd_pin
led_pins[3:0]
uart_led
rxd_pin_IBUF_inst
I
O
IBUF
txd_pin_OBUF_inst
OBUF
txd_pin

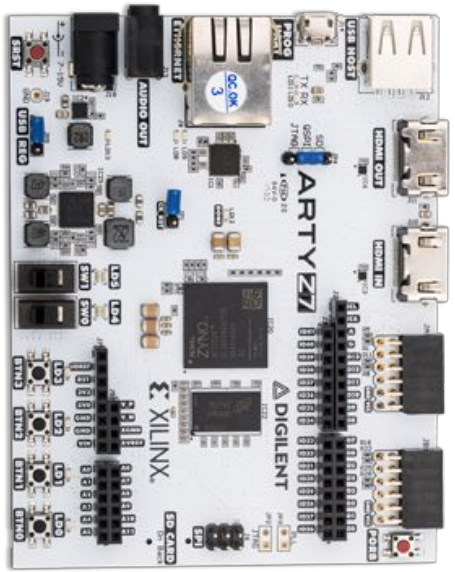
```
##############################
set_property -dict {PACKAGE_PIN R14 IOSTANDARD LVCMOS33} [get_ports {led_pins[0]}]
set_property -dict {PACKAGE_PIN P14 IOSTANDARD LVCMOS33} [get_ports {led_pins[1]}]
set_property -dict {PACKAGE_PIN N16 IOSTANDARD LVCMOS33} [get_ports {led_pins[2]}]
set_property -dict {PACKAGE_PIN M14 IOSTANDARD LVCMOS33} [get_ports {led_pins[3]}]

# CLK source 50 MHz
set_property -dict {PACKAGE_PIN H16 IOSTANDARD LVCMOS33} [get_ports clk_pin]

# Rst Btn[3]
set_property -dict {PACKAGE_PIN L19 IOSTANDARD LVCMOS33} [get_ports rst_pin]

# Nible Swap Btn[0]
set_property -dict {PACKAGE_PIN D19 IOSTANDARD LVCMOS33} [get_ports btn_pin]

# UART
set_property -dict {PACKAGE_PIN Y18 IOSTANDARD LVCMOS33} [get_ports rxd_pin]
set_property -dict {PACKAGE_PIN Y19 IOSTANDARD LVCMOS33} [get_ports txd_pin]
```



Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vr
All ports (9)										
led_pins (4)	OUT					✓	(Multiple)	LVCMOS33*	3.300	
led_pins[3]	OUT				M14	✓	35	LVCMOS33*	3.300	
led_pins[2]	OUT				N16	✓	35	LVCMOS33*	3.300	
led_pins[1]	OUT				P14	✓	34	LVCMOS33*	3.300	
led_pins[0]	OUT				R14	✓	34	LVCMOS33*	3.300	
Scalar ports (5)										
btn_pin	IN				D19	✓	35	LVCMOS33*	3.300	
clk_pin	IN				H16	✓	35	LVCMOS33*	3.300	
rst_pin	IN				L19	✓	35	LVCMOS33*	3.300	
rxd_pin	IN							default (LVCMOS18)	1.800	
txd_pin	OUT				Y19	✓	34	LVCMOS33*	3.300	


arkers View Help
From: 0 sec
To: 2 us
Marker: --
Cursor: 1835 ns
Signals
Waves
Time
btn_clk_rx_tb
clk_rx_tb
led_o_tb[3:0]
rst_clk_rx_tb
rx_data_rdy_tb
rx_data_tb[7:0]
1 us
41
42
arkers View Help
From: 0 sec
To: 2 us
Marker: --
Cursor: 1921 ns
Signals
Waves
Time
btn_clk_rx_tb
clk_rx_tb
led_o_tb[3:0]
rst_clk_rx_tb
rx_data_rdy_tb
rx_data_tb[7:0]
1 us
2 u
41