ECE 165 – Project

Progress report due: 5/25/2022 @ 11:59pm
Final report due: 6/2/2022 @ 11:59pm

Project Overview

The project this year for ECE 165 is to hand-design the schematic of **an 8-bit adder**. Specifically, the adder you design should have faster performance than the one you synthesized in Lab 4. This project is a great opportunity to design a fairly complex circuit that will solidify your Cadence Virtuoso skill set, your knowledge of arithmetic circuit design, and your ability to creatively design circuits that have better performance than vanilla designs.

Design Criteria

The adder will have inputs A<7:0>, B<7:0>, and outputs S<8:0>, where S<8> is the carry out of the last stage. Note that there is no carry-in for this adder. All inputs to the adder will arrive from the outputs of positive-edge triggered flip-flops, and the outputs of the adder will be loaded by the D input of positive-edge triggered flip-flops. A testbench called proj_tb_SP22 – it can be found in the Lab4_adder_tb library. The top location is where you will place your synthesized adder from Lab 4, while the bottom location is where you will place your custom designed adder. Note that the CLK and RST signals are only necessary in the custom design if you choose to use a dynamic logic family.

The circuit itself can be designed using **any** CMOS logic style with rail-to-rail outputs – this includes both static and dynamic logic styles. The adder architecture should **NOT** be the standard simple ripple-carry design. Projects that employ such an architecture will receive a 50% automatic deduction before the report is graded. Instead, you should try carry-lookahead, carry-skip, Kogge-Stone architectures, etc. More creative approaches will receive more points. It is strongly recommended to use a supply voltage of 1.1V, as that is what the synthesized adder will use. While you are technically permitted to use a smaller supply voltage (though we don't necessarily recommend this), you are NOT allowed to use a supply voltage higher than 1.1V.

To help with design-time, **you are permitted to the use the standard cells found in the gsclib045** for inverters, NORs, NANDs, etc. However, you are **NOT** permitted to use the ADDFX1 cell – otherwise a 25% automatic deduction will apply. Instead, you must design a **full-custom, transistor-level** full adder (or equivalent PG) cell yourself. This cell should, at minimum, have different sized transistors than the ADDFX1 gsclib045 cell. Hint: do NOT simply use NANDs/NORs/XORs to design your own FA cell – this is highly un-optimal. Instead, please review the class notes and textbook that discuss the transistor-level, single-stage complementary static CMOS implementation of a full-adder cell.

Designs that do not use a full adder cell by their very nature should instead custom design (at the transistor-level) at least one block that is found on the critical path (specifically, the largest cell found and repeated multiple times on the critical path – like the black box cell on a tree adder, for example).

Progress Reporting Requirements

Since design of your adder can take a long time, we strongly encourage submission of a brief progress report before the final report is due. This report, worth 5% of the total lab grade, should only include a picture of your *complete schematic-level* adder, with your names and student ID numbers annotated in readable test directly on the schematic. Late reports will not receive any points, and any addition details contained in the report will be ignored. Please submit this "report" to Gradescope by the due date noted above.

Final Reporting Requirements

The final project report will consist of one page of text and up to 7 figures, modeled in part after the *International Solid-State Circuits Conference* (ISSCC) format.[1] Page one of the report will contain only text, in 9-point Times New Roman font in double column format (the title will be larger). If you decide to cite any literature, please include the references in 8-point Times New Roman at the end of page one. Suggestions on topics to cover in your report are:

- Clearly introduce the design challenge and why it is important
- Briefly describe previous architectures and why they are not optimal for speed
- Describe your chosen architecture, and why you think it will be better
- Describe the most innovative aspects of your work
- If something did not work as you expected, explain why
- Provide suggestions for future iterations of your design
- Indicate who in your team did what portion of the project

Pages two through seven will have one figure per page, for a total of six figures (note: sub-figures are permitted, but should be thematically related). You are permitted to have a 7th optional figure should you require it. You should reference all figures on page one within your main body of text. *Note that writing quality matters in your grade, so make sure to think carefully about how to present your work and clearly explain your design*. A template will be provided for the report. The required figures are:

1. Schematic of the 1-bit adder used (show a screen shot within Cadence, and include your name and student ID number as a "note text" within the schematic itself – i.e., do not place it onto the schematic figure in Photoshop afterwards). If your adder does not use a 1-bit full adder (e.g., instead uses PG and AO cells), show the custom schematic of the largest cell that is repeated multiple times on the critical path.
2. Schematic of some other important circuit in your design.
3. Schematic of the 8-bit adder (include name and ID number as in Fig. 1).

[1] ISSCC is a prestigious conference held in San Francisco every February that showcases the latest and greatest in VLSI and integrated circuit research.

4. Optional for bonus points only. Layout of the 8-bit adder (include ruler-based area measurement of the core circuit). Use rulers to draw a single rectangular box around the layout, reporting this area as your "core area" of the design. Also include screen shot of LVS/DRC runs with no errors.
5. Transient simulation result showing the maximum frequency of the custom adder compared to the adder generated after PnR in Lab 4 (use sub-figures a) and b) for this). You should be able to show that the critical inputs are being used, and that the "results<8:0>" output produces the correct results at this operational frequency. The maximum frequency is set by the 'fclk' variable in the testbench (and is NOT double the propagation time). Please also include in this figure the transient current waveform, and the time over which you 'clipped' and 'averaged' power (per the description after the table).
6. Table of results.
7. (Optional) an extra figure that might help explain your design and/or results.

Please include captions for your figures describing what is shown (and explicitly mentioned any measured results, if applicable). A sample table of results is shown below. Feel free to expand if necessary.

	Place+route schematic	Custom design schematic	Place+route (optional)	Custom design extracted (optional)
	Performance for VDD = 1.1V			
f_{max}				
Power consumption @ f_{max}				
Energy per operation @ f_{max}				
	Performance for VDD = 1.1V, f_{CLK} = 1 GHz			
Power consumption @ 1 GHz				
Energy per operation @ 1 GHz				
	Other important parameters			
Adder architecture	Ripple-carry		Ripple-carry	
Core area	-	-		
Critical input pair (i.e., A=?, B=?)				
Transistor types used (e.g., VTL, VTG)				

Note that the provided testbench includes input vectors that contain the critical input for a *ripple-carry adder*. If your design has a different set of critical input vectors, please make sure to *modify the testbench (ideally by making a copy) to use the critical input vectors when characterizing frequency and power*. Power should be measured by averaging I*V over *at least* 10 cycles WITH SWITCHING EVENTS and including the power of the D flip flops! Hint: the testbench includes some initialization time – this should **NOT** be included in your power consumption – use the calculator's 'clip' function to generate power

results once the inputs start switching. Please show and clearly label a plot of the system current, showing exactly over what time interval you are averaging power.

Evaluation

Work is to be ideally completed in teams of two. Please use the piazza 'find a teammate' feature if you don't know anyone in the class to work with – it will help reduce your design load.

You will be evaluated on the on-time submission of the progress report (5%), the quality of your final report writing and design choice reasoning (30%), the clarity of your presentation of figures and results (20%), and the technical achievements of your work (45%). The technical achievements will be graded according to the following guidelines:

- Design runs correctly (post-layout) at frequencies greater than 1.8GHz (35%)
- Design creativity and innovativeness (10%)

A 10% bonus will be awarded to the group that achieves the fastest post-extracted clock speed (set by fclk in the testbench), as long as the energy/cycle is less than 700fJ/cycle. A 5% bonus will be awarded to a group that is within the top 25% of the class in terms of speed, and yet achieves the lowest energy per operation within that group. A 5% bonus will be awarded to a group within the top 50% of the class in terms of speed, and yet achieves the smallest layout area design. Finally, an additional 5% bonus will be awarded to teams who layout the entire adder and still meet all of the design specifications.

Please be very clear about how you arrive at your simulation results – if your numbers look too good to be true, we reserve the right to run your simulations ourselves, and, if it turns out you either falsely quoted numbers or set up your simulation in an unfair or incorrect manner, we will deduct (likely significant) points. Academic integrity is important.

Please submit an electronic copy of your report to Canvas before the due date.

A note on working in a team using Cadence

Normally, the best way to do this is to open up the permissions on your file system (and/or create a separate linux group) such that you and your partner work together on the same Cadence library. However, the risk of doing this (without using groups) is that other students can read and edit your files, which you may not want to have happen. The logistically-easiest way to handle this is to make a copy of your files, open up their permissions (use the 'chmod -R' command), have your partner copy over the files, then delete the copy you made (the one with the open permissions). You can also share via a USB drive. Since we are using an open-source PDK, it is possible to share like this. Note that if you are using a commercial PDK in which you've signed a non-disclosure agreement (NDA) to use, this method of sharing may not be an appropriate option.

Hints and tips

- Remember to set the 'fclk' term in your testbench.
- You need to verify *functionality* when operating at your maximum speed. For your circuit to work correctly, your RESULTS_CLOCKED<7> bit should toggle up and one cycle after the critical input arrives (under the default proj_tb setup). The maximum operation speed is just below the speed at which this condition no longer occurs. You should clearly show this in your report.
- It is recommended to set a step size of 10-100ps. The simulation run length should be such that you see at least 10 clock cycles.
- Only applicable to those who elect to layout the entire adder – You MUST use a hierarchical design approach here. Not doing so will make your life very difficult! You will want to LVS each individual block before putting your whole layout together.
- LVS for large blocks can be difficult to diagnose. You can search the web for documents that try to help. For example, this document can be useful (though doesn't strictly deal with the Calibre interface we use in this class):
    - http://www.egr.msu.edu/classes/ece410/salem/files/s14/labs/guides/guide-LVS.pdf