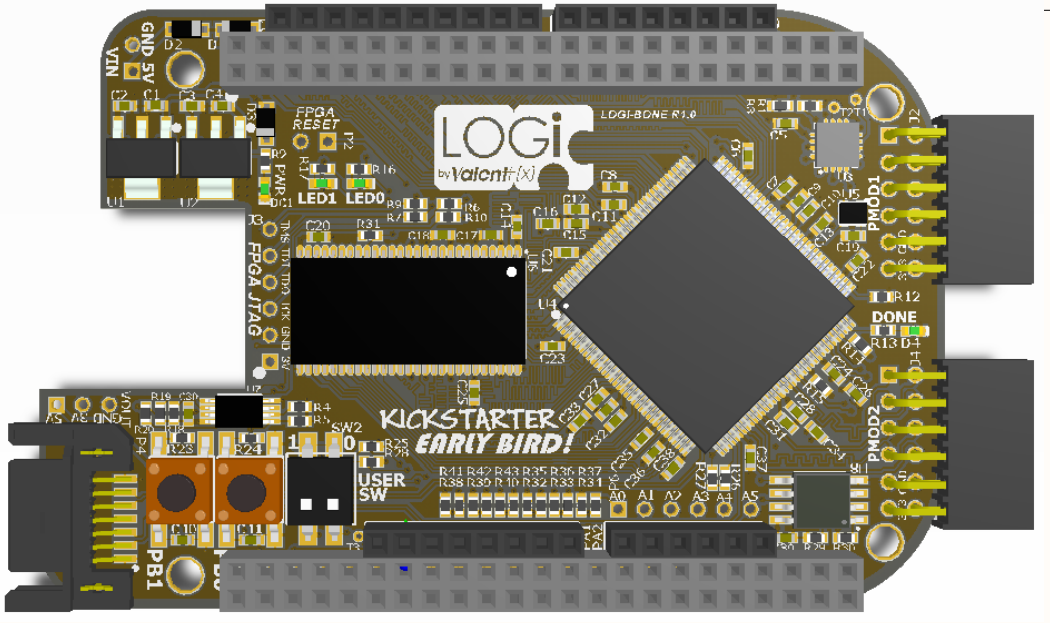

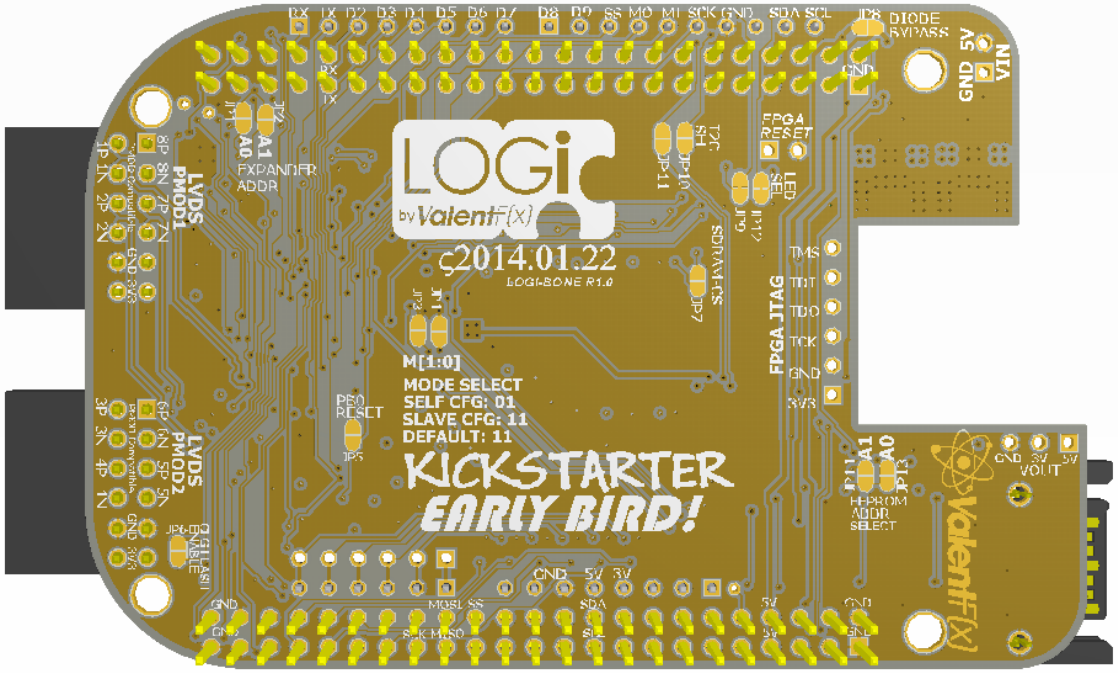

U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

LOGi-Bone Top Level			
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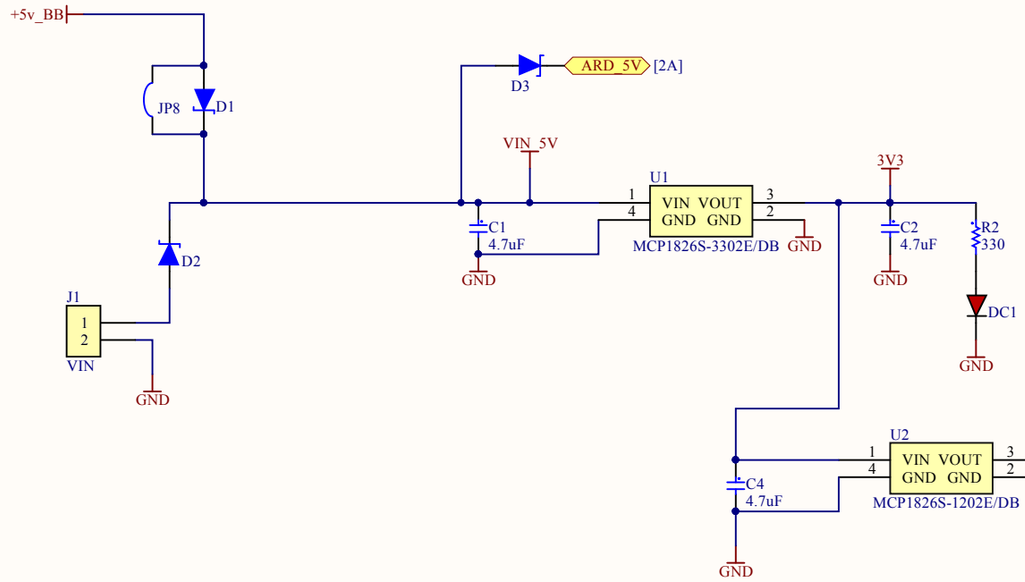
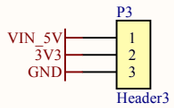
ValentF(x) ELECTRONICS INNOVATION

Power: By Default Power will be supplied by the Beaglebone.

Optionally power can be supplied through FPGA VIN header J1.



1 x Auxillary Power output Headers



LOGI-LOGO-600
LOGO3

VALENTFX-LOGO-750
Logo5

LOGI-LOGO-750
LOGO4

Title	Power Supply		
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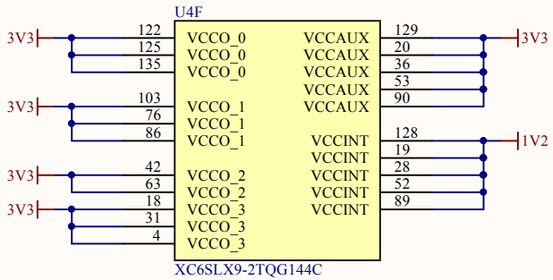
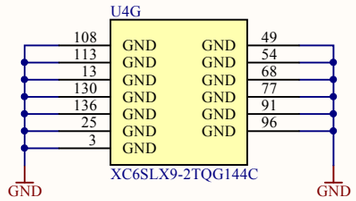
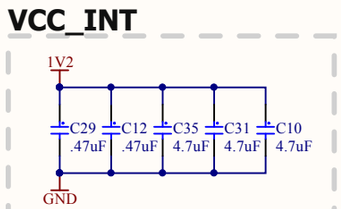
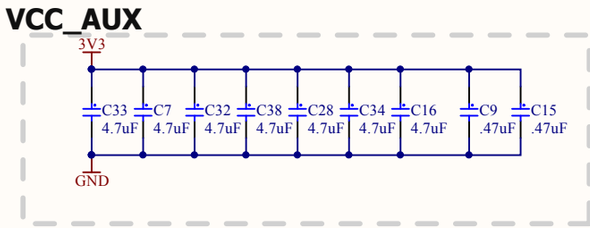
Date:	3/4/2015	Engineer:	MJones

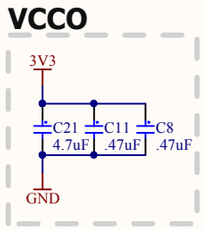
ValentF(x) ELECTRONICS INNOVATION

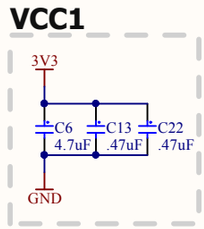


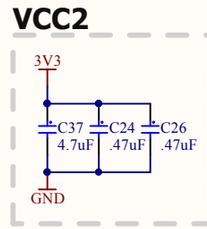


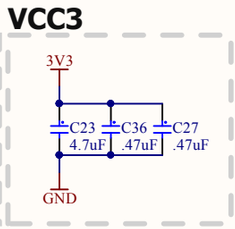




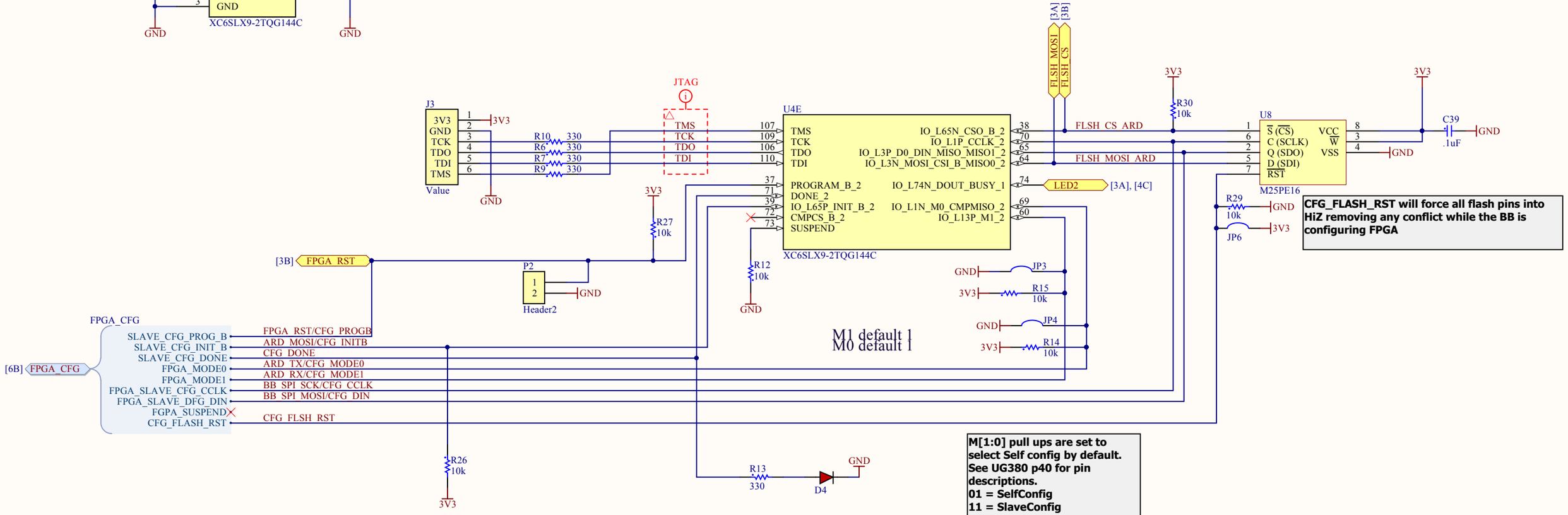








Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution



Title	FPGA Configuration		
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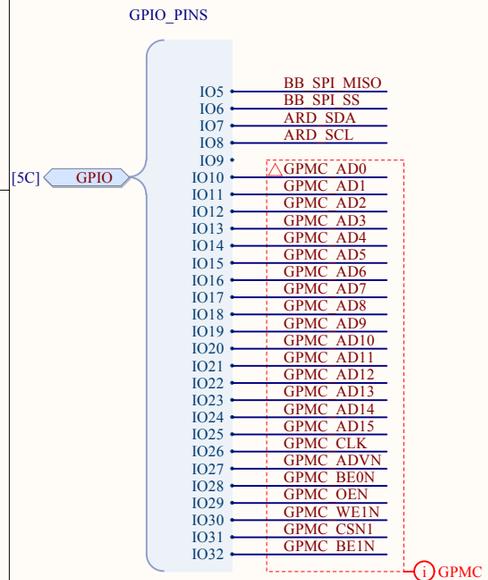
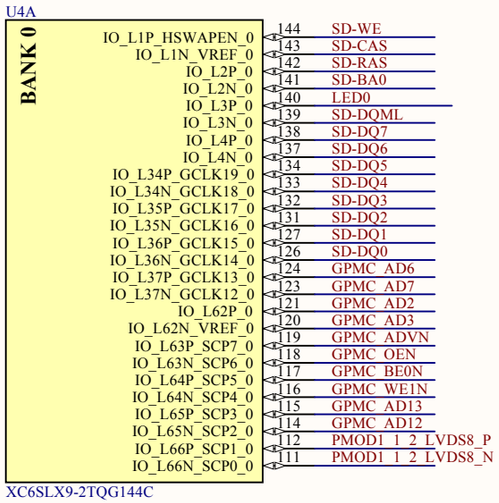
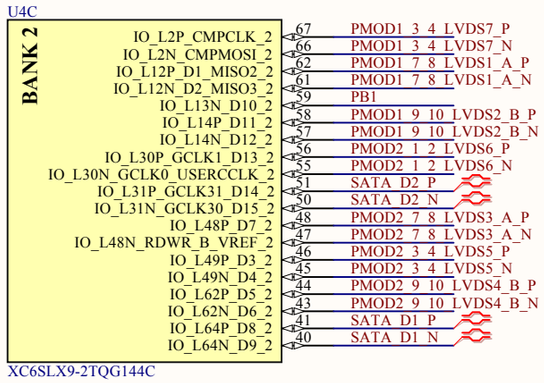
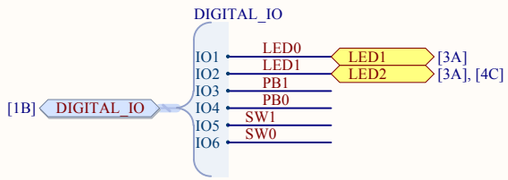
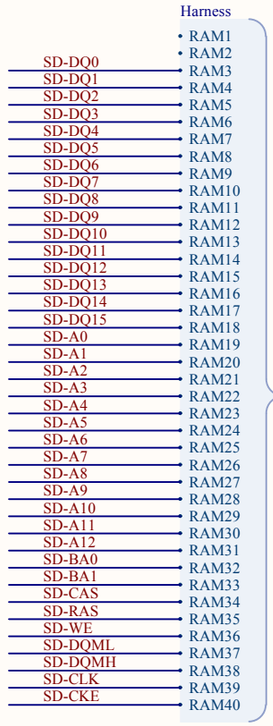
ValentF(x) ELECTRONICS INNOVATION

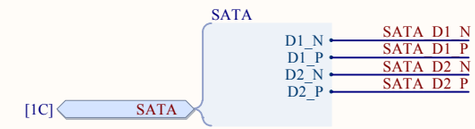


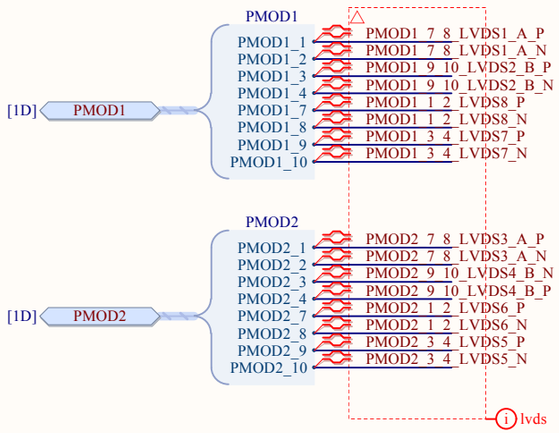


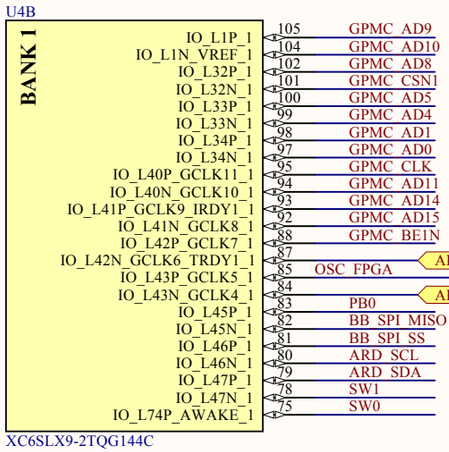


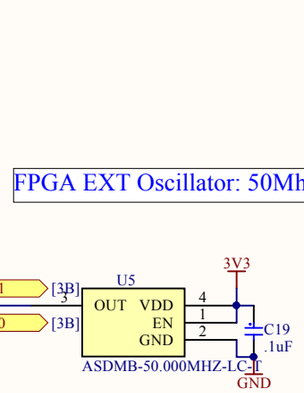


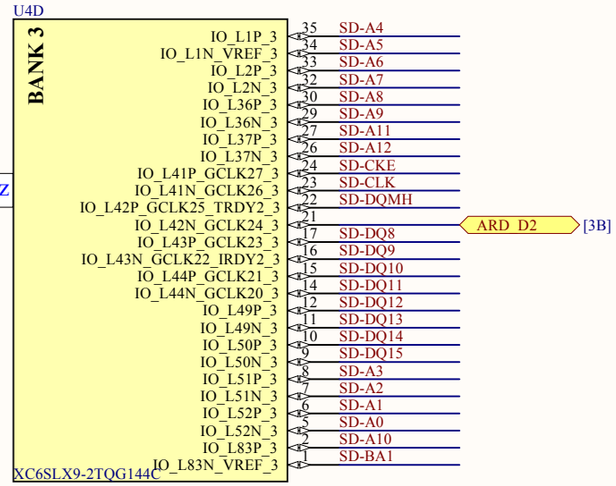












Title	FPGA Logic		
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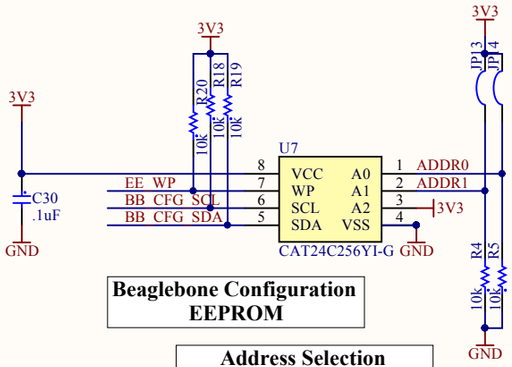
ValentF(x) ELECTRONICS INNOVATION

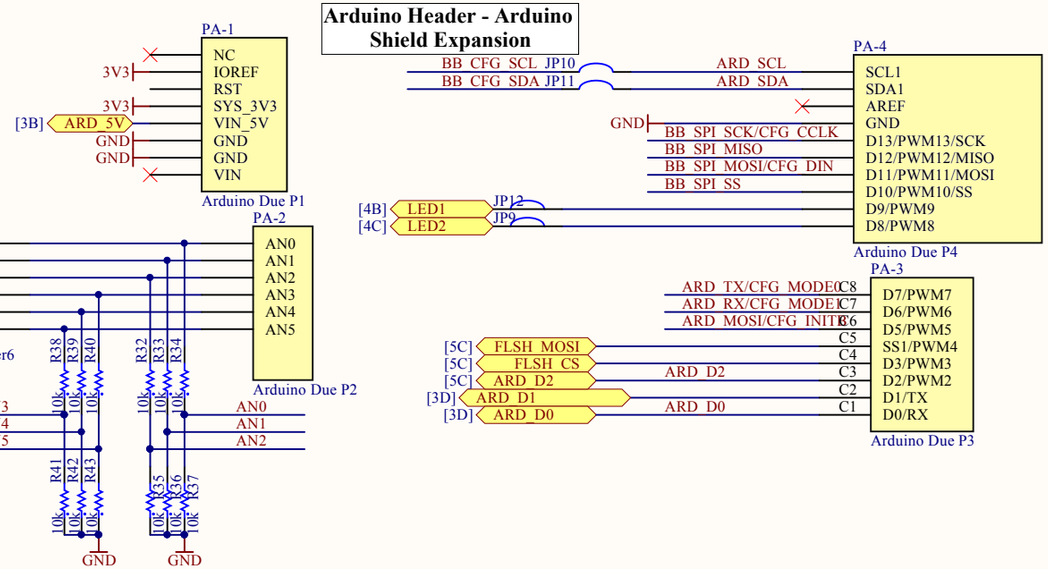
Beaglebone Configuration EEPROM



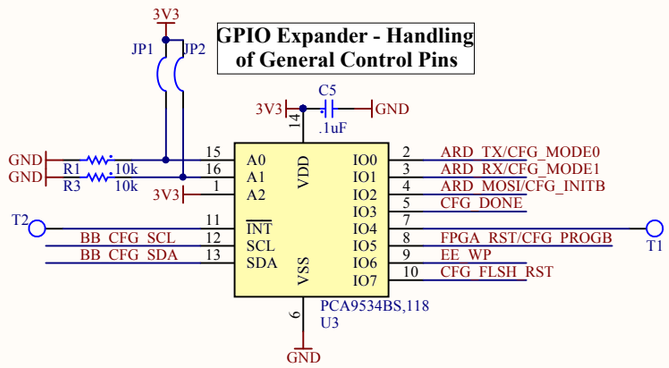
Address Selection DIP SW

If the DIP SW is NOT installed the eerpom will hold the low address 0x54 (highest priority) for capes and be used for the bone pin configuration in the case multiple installed of capes

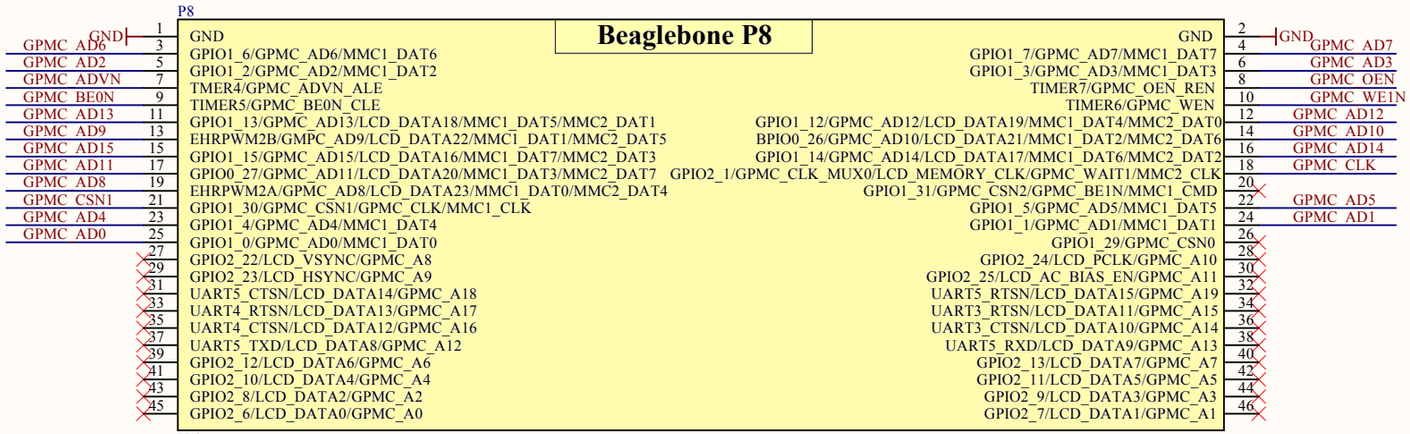
Arduino Header - Arduino Shield Expansion



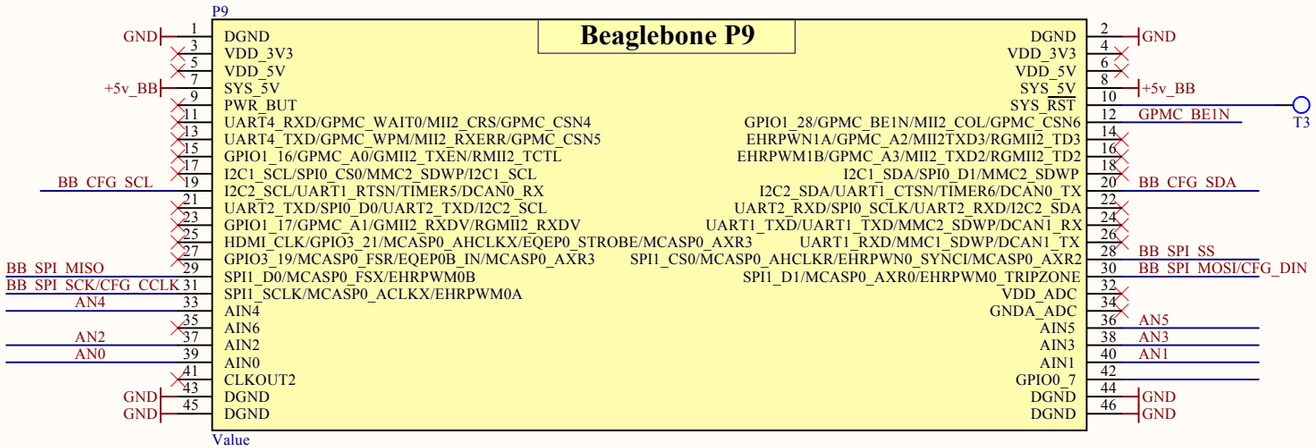
GPIO Expander - Handling of General Control Pins

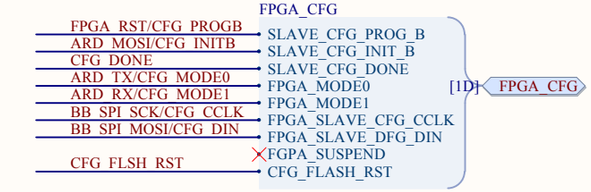


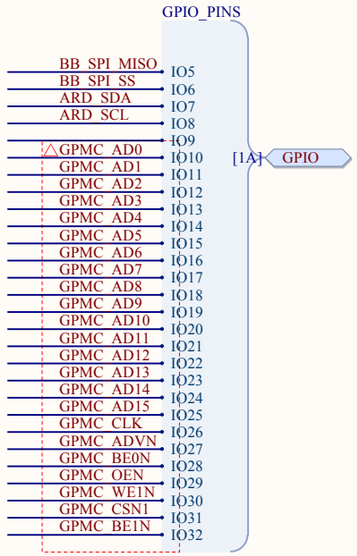
Beaglebone P8



Beaglebone P9







Title	Peripheral Port IO		
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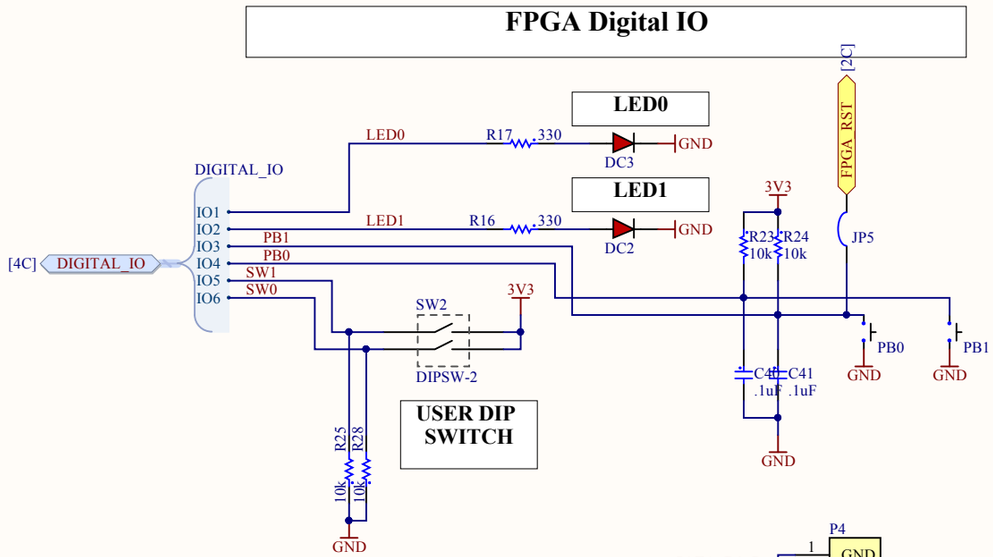
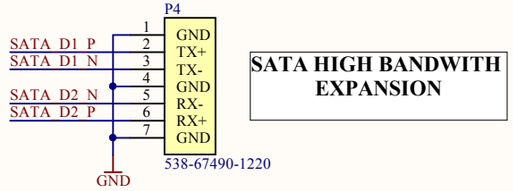
ValentF(x) ELECTRONICS INNOVATION

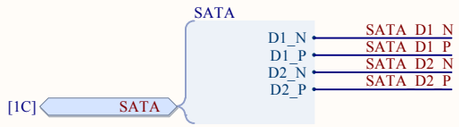
FPGA Digital IO

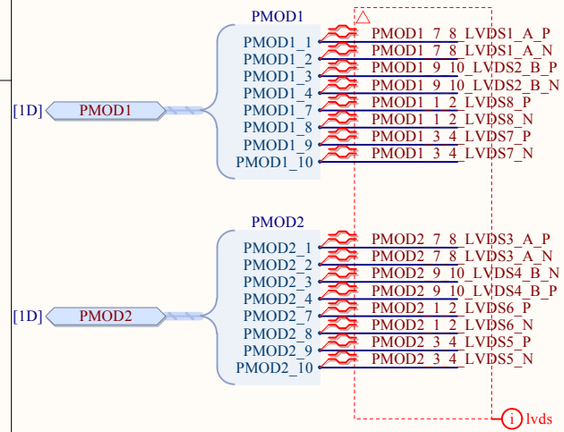


USER PUSH BUTTON

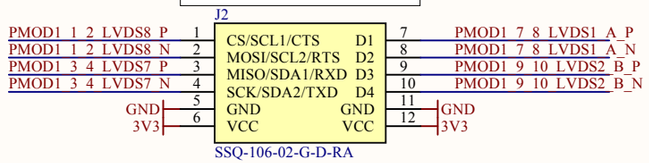


SATA HIGH BANDWITH EXPANSION

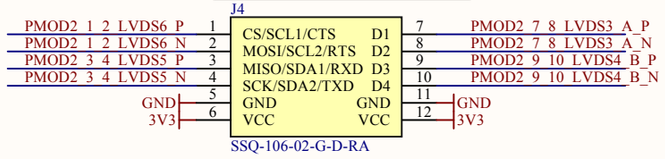




PMOD1 PORT



PMOD2 PORT



Title	Digital IO		
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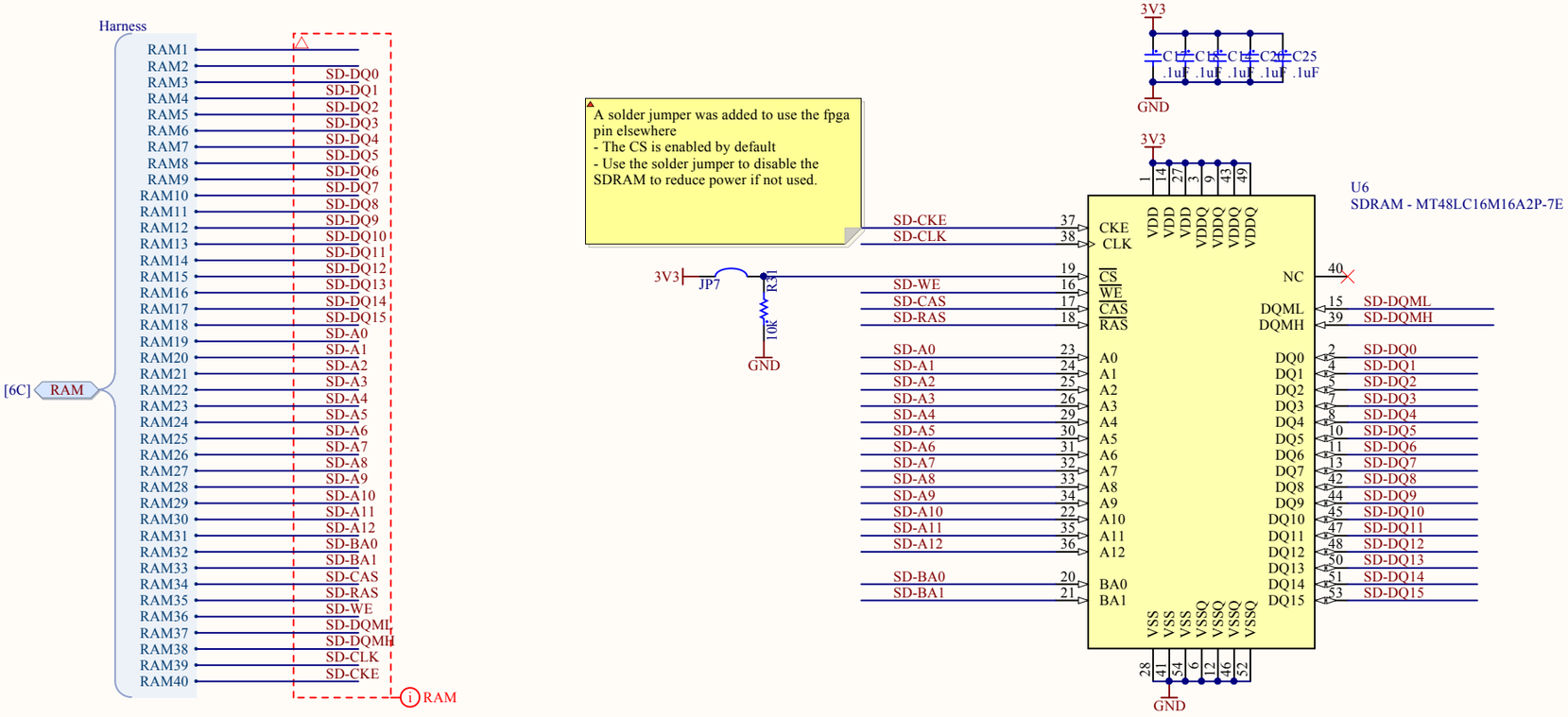
ValentF(X) ELECTRONICS INNOVATION

SDRAM



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ValentF(x) ELECTRONICS INNOVATION