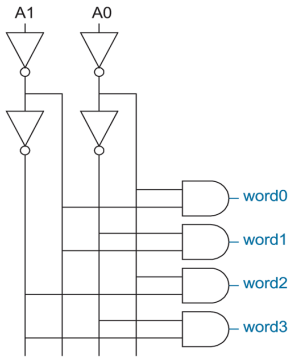
ECE 758 Week-2 Homework Due Date: February 2, 2023

No collaboration is permitted in this homework. Your work must be your own. This rule is strictly followed.

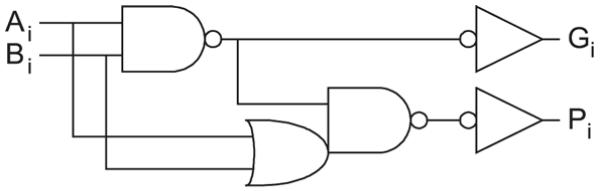
Extra credit for showing independent work

Q1. Homework questions at the end of Lecture-2A and Leacture-3A

Q2. Design a VHDL (dataflow) model for the following circuits. Declare the internal signals. Please simulate the circuits in ModelSim and show that your circuits work correctly for all possible combinations. Carryout synthesis using Leo and compare the post-synthesis circuits and ModelSim simulations. Are they identical?



(a)



(b)

Q3. Model the tollbooth controller in VHDL that works in the following way. In the *idle* (00) state, the tollbooth, with its gate lowered and its green "proceed" light off, awaits a car. When a car enters the tollbooth, a pressure sensor detects the car and passes a signal to the controller. The controller then awaits the correct toll signal and on receiving this, raises the gate and turns the green light on. When the car exits the tollbooth, the controller reenters the *idle* state (green light off and gate down). (See Weste and Eshraghian book (93 edition) for details.)

1. Define the logic expressions first after building the state transition table.
2. Do the VHDL simulations to make sure your design work.
3. Do the logic synthesis of this model.
4. Outline the gate count and plan to reduce the number of gates by remodeling.
5. Carry out the post synthesis simulation in VHDL and monitor the changes.
6. Complete the layout by using layouts of basic gates.
7. Submit an excellent report with figure numbers and figure captions.