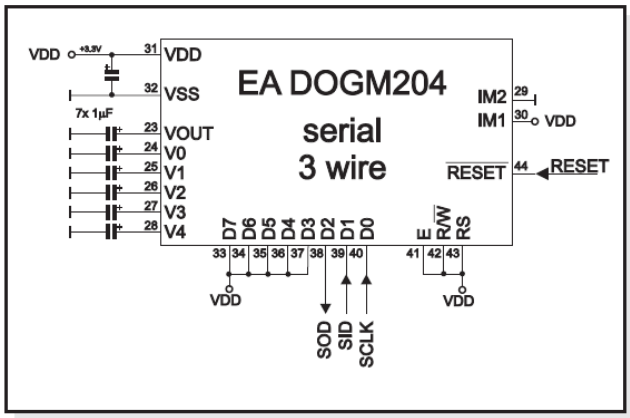
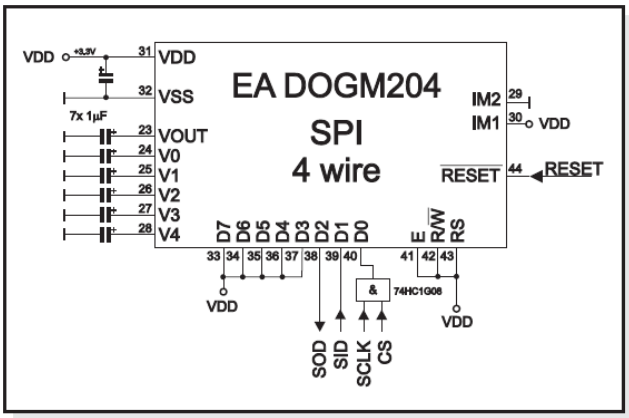
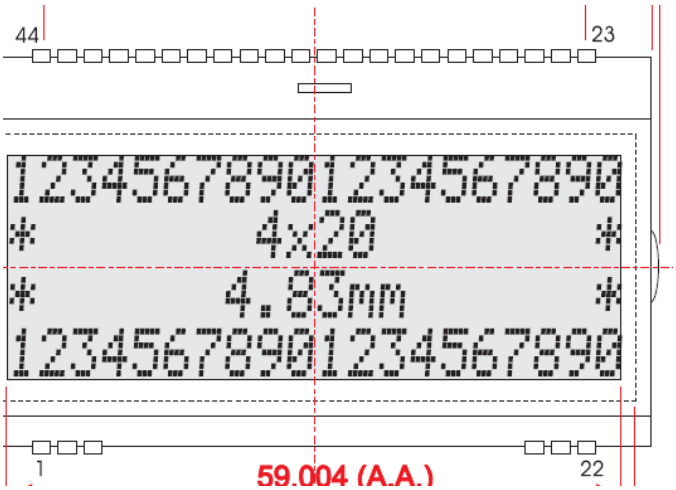
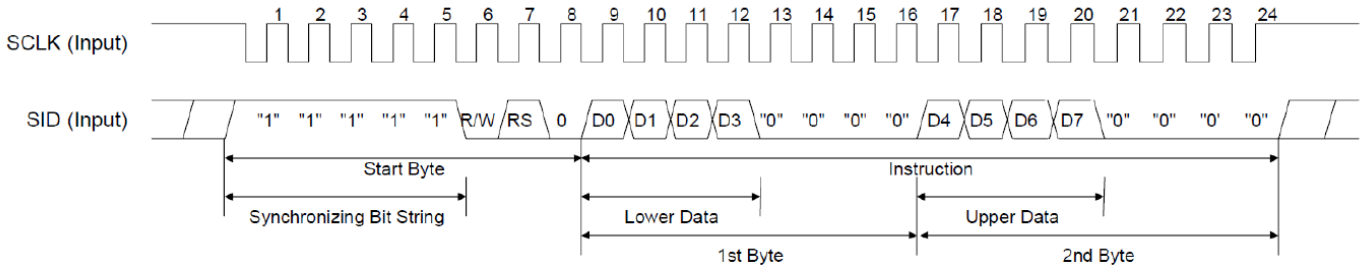




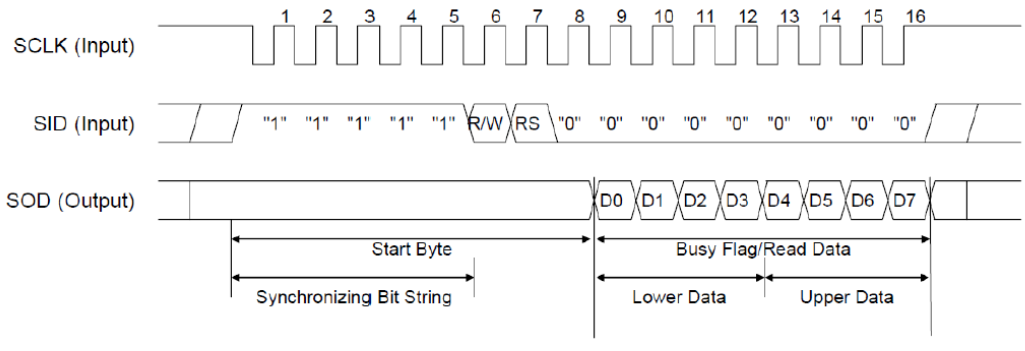


Pin	Symbol	Level	Function		Pin	Symbol	Level	Function
1	NC		(A1+: LED backlight)		23	VOUT	-	Voltage converter output
2	NC		(A2+: LED backlight)		24	V0	-	Regulated voltage output
3	NC		(A3+: LED backlight)		25	V1	-	Regulated voltage output
4					26	V2	-	Regulated voltage output
5					27	V3	-	Regulated voltage output
6					28	V4	-	Regulated voltage output
7					29	IM2	H / L	Interface mode select 2
8					30	IM1	H / L	Interface mode select 1
9					31	VDD	H	Power Supply +2.4..+3,6V
10					32	VSS	L	Power Supply 0V
11					33	D7	H / L	Data
12					34	D6	H / L	Data
13					35	D5	H / L	Data
14					36	D4	H / L	Data
15					37	D3	H / L	Data
16					38	D2	H / L	Data / SOD / SDAout
17					39	D1	H / L	Data / SID / SDAin
18					40	D0	H / L	Data / SCLK / SCL
19					41	E	H	Enable (falling edge)
20	NC		(C1-: LED backlight)		42	R/W	H / L	L= Write, H=Read
21	NC		(C2-: LED backlight)		43	RS	H / L	L=Cmd, H=Data / SA0
22	NC		(C3-: LED backlight)		44	RESET	L	Reset

Serial Write Operation



Serial Read Operation



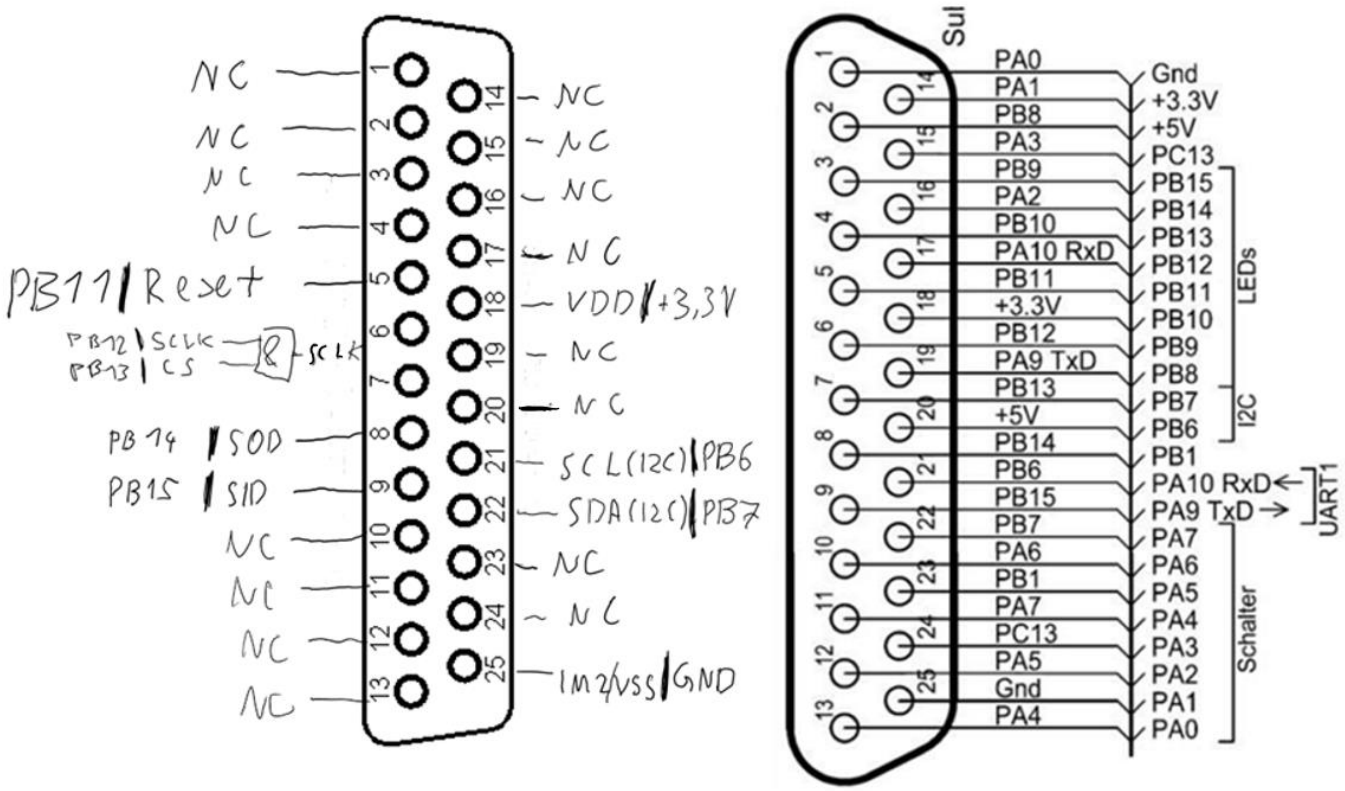


Table 17. Port bit configuration table

Configuration mode		CNF1	CNF0	MODE1	MODE0	PxODR register
General purpose output	Push-pull	0	0	01 10 11 see *Table 18*		0 or 1
	Open-drain		1			0 or 1
Alternate Function output	Push-pull	1	0			don't care
	Open-drain		1			don't care
Input	Analog input	0	0	00		don't care
	Input floating		1			don't care
	Input pull-down	1	0			0
	Input pull-up					1

MODE[1:0]	Meaning
00	Reserved
01	Max. output speed 10 MHz
10	Max. output speed 2 MHz
11	Max. output speed 50 MHz

Table 22. SPI

SPI pinout	Configuration	GPIO configuration
SPIx_SCK	Master	Alternate function push-pull
	Slave	Input floating
SPIx_MOSI	Full duplex / Master	Alternate function push-pull
	Full duplex / slave	Input floating / Input pull-up
	Simplex bidirectional data wire / Master	Alternate function push-pull
	Simplex bidirectional data wire/ Slave	Not used. Can be used as a GPIO
SPIx_MISO	Full duplex / Master	Input floating / Input pull-up
	Full Duplex / slave	Alternate function push-pull
	Simplex bidirectional data wire / Master	Not used. Can be used as a GPIO
	Simplex bidirectional data wire/ Slave	Alternate function push-pull
SPIx_NSS	Hardware Master /Slave	Input floating/ Input pull-up / Input pull-down
	Hardware Master/ NSS output enabled	Alternate function push-pull
	Software	Not used. Can be used as a GPIO

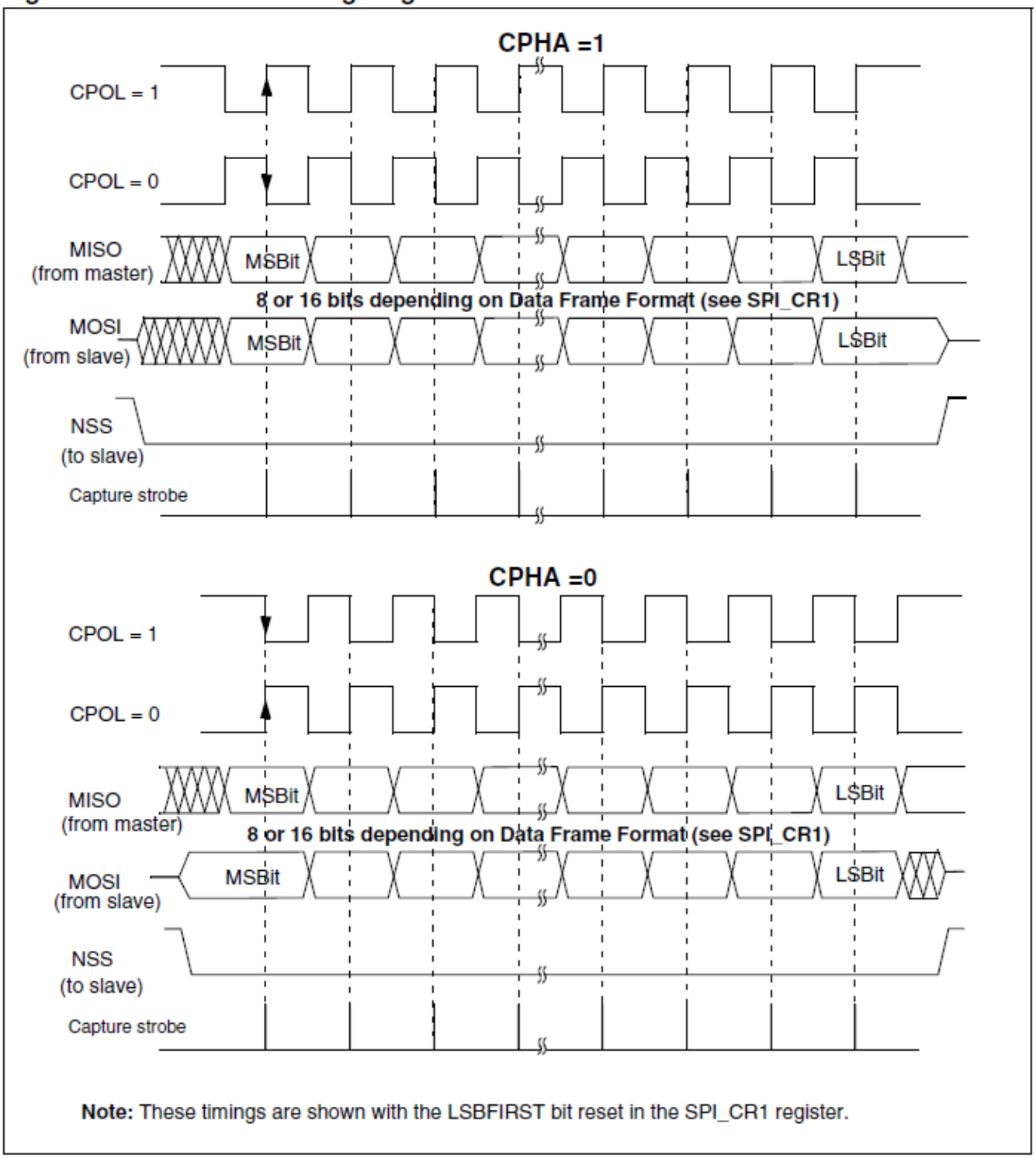
8.3.10 SPI1 alternate function remapping

Refer to *AF remap and debug I/O configuration register (AFIO_MAPR)*

Table 47. SPI1 remapping

Alternate function	SPI1_REMAP = 0	SPI1_REMAP = 1
SPI1_NSS	PA4	PA15
SPI1_SCK	PA5	PB3
SPI1_MISO	PA6	PB4
SPI1_MOSI	PA7	PB5

Figure 210. Data clock timing diagram



Note: These timings are shown with the LSBFIRST bit reset in the SPI_CR1 register.

Baudrate einstellen in SPI_CR1 (fPCLK=36MHz bzw. 72MHz):

000: fPCLK/2
001: fPCLK/4
010: fPCLK/8
011: fPCLK/16
100: fPCLK/32
101: fPCLK/64
110: fPCLK/128
111: fPCLK/256 -> gewählt: 110: fPCLK/128

23.5.1 SPI control register 1 (SPI_CR1) (not used in I²S mode)

Address offset: 0x00

Reset value: 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIDI MODE	BIDI OE	CRC EN	CRC NEXT	DFF	RX ONLY	SSM	SSI	LSB FIRST	SPE	BR [2:0]			MSTR	CPOL	CPHA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

23.5.2 SPI control register 2 (SPI_CR2)

Address offset: 0x04

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								TXEIE	RXNE IE	ERRIE	reserved		SSOE	TXDMA EN	RXDMA EN
Res.								rw	rw	rw	Res.		rw	rw	rw

23.5.3 SPI status register (SPI_SR)

Address offset: 08h

Reset value: 0x0002

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								BSY	OVR	MODF	CRC ERR	UDR	CHSID E	TXE	RXNE
Res.								r	r	r	rc_w0	r	r	r	r

23.5.4 SPI data register (SPI_DR)

Address offset: 0x0C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

23.5.5 SPI CRC polynomial register (SPI_CRCPR) (not used in I²S mode)

Address offset: 0x10

Reset value: 0x0007

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCPOLY[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

23.5.6 SPI Rx CRC register (SPI_RXCRCR) (not used in I²S mode)

Address offset: 0x14

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxCRC[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

23.5.7 SPI Tx CRC register (SPI_TXCRCR) (not used in I²S mode)

Address offset: 0x18

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TxCRC[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

23.5.8 SPI_I²S configuration register (SPI_I2SCFGR)

Address offset: 1Ch

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				I2SMOD	I2SE	I2SCFG		PCMSYNC	Reserved	I2SSTD		CKPOL	DATLEN		CHLEN
				rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw

23.5.9 SPI_I²S prescaler register (SPI_I2SPR)

Address offset: 20h

Reset value: 0000 0010 (0002h)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						MCKOE	ODD	I2SDIV							
Res.						rw	rw	rw							

Table 169. SPI register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	**SPI_CR1**	Reserved																BIDIMODE	BIDIOE	CRCEN	CRCNEXT	DFF	RXONLY	SSM	SSI	LSBFIRST	SPE	BR [2:0]			MSTR	CPOL	CPHA
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	**SPI_CR2**	Reserved																								TXEIE	RXNEIE	ERRIE	Reserved		SSOE	TXDMAEN	RXDMAEN
	Reset value																									0	0	0			0	0	0
0x08	**SPI_SR**	Reserved																								BSY	OVR	MODF	CRCERR	UDR	CHSIDE	TXE	RXNE
	Reset value																									0	0	0	0	0	0	1	0
0x0C	**SPI_DR**	Reserved																DR[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x10	**SPI_CRCPR**	Reserved																CRCPOLY[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0x14	**SPI_RXCRCR**	Reserved																RxCRC[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	**SPI_TXCRCR**	Reserved																TxCRC[15:0]															
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	**SPI_I2SCFGR**	Reserved																				I2SMOD	I2SE	I2SCFG		PCMSYNC	Reserved	I2SSTD		CKPOL	DATLEN		CHLEN
	Reset value																					0	0	0	0	0		0	0	0	0	0	0
0x20	**SPI_I2SPR**	Reserved																						MCKOE	ODD	I2SDIV							
	Reset value																							0	0	0	0	0	0	0	0	1	0