1. Description

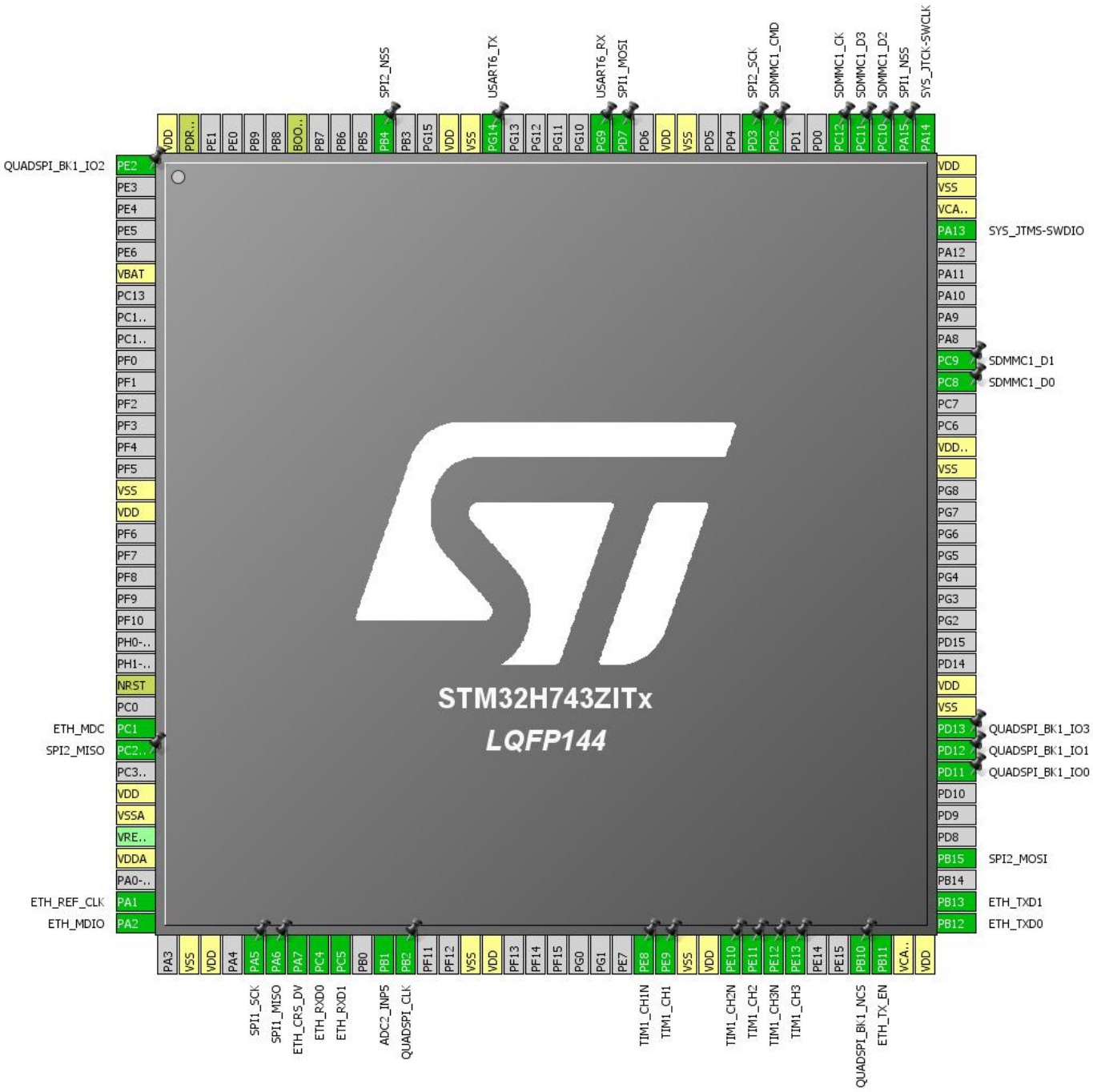
1.1. Project

Project Name	STM32Cube_pin_assignment_
Board Name	No information
Generated with:	STM32CubeMX 4.23.0
Date	11/22/2017

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7x3
MCU name	STM32H743ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration

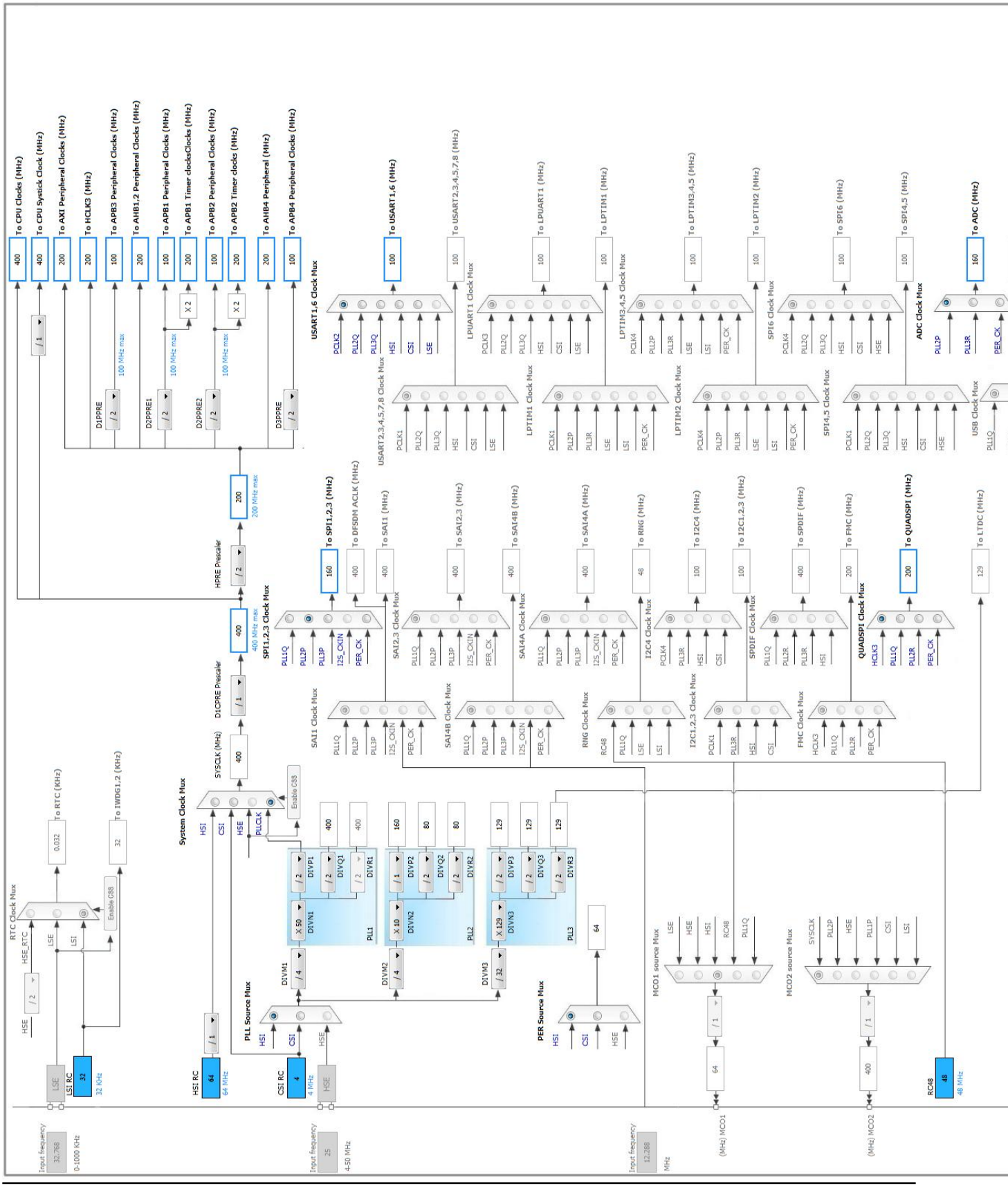


3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
6	VBAT	Power		
16	VSS	Power		
17	VDD	Power		
25	NRST	Reset		
27	PC1	I/O	ETH_MDC	
28	PC2_C	I/O	SPI2_MISO	
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
35	PA1	I/O	ETH_REF_CLK	
36	PA2	I/O	ETH_MDIO	
38	VSS	Power		
39	VDD	Power		
41	PA5	I/O	SPI1_SCK	
42	PA6	I/O	SPI1_MISO	
43	PA7	I/O	ETH_CRS_DV	
44	PC4	I/O	ETH_RXD0	
45	PC5	I/O	ETH_RXD1	
47	PB1	I/O	ADC2_INP5	
48	PB2	I/O	QUADSPI_CLK	
51	VSS	Power		
52	VDD	Power		
59	PE8	I/O	TIM1_CH1N	
60	PE9	I/O	TIM1_CH1	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	TIM1_CH2N	
64	PE11	I/O	TIM1_CH2	
65	PE12	I/O	TIM1_CH3N	
66	PE13	I/O	TIM1_CH3	
69	PB10	I/O	QUADSPI_BK1_NCS	
70	PB11	I/O	ETH_TX_EN	
71	VCAP1	Power		
72	VDD	Power		
73	PB12	I/O	ETH_TXD0	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
74	PB13	I/O	ETH_TXD1	
76	PB15	I/O	SPI2_MOSI	
80	PD11	I/O	QUADSPI_BK1_IO0	
81	PD12	I/O	QUADSPI_BK1_IO1	
82	PD13	I/O	QUADSPI_BK1_IO3	
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDD33_USB	Power		
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
105	PA13	I/O	SYS_JTMS-SWDIO	
106	VCAP2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14	I/O	SYS_JTCK-SWCLK	
110	PA15	I/O	SPI1_NSS	
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
116	PD2	I/O	SDMMC1_CMD	
117	PD3	I/O	SPI2_SCK	
120	VSS	Power		
121	VDD	Power		
123	PD7	I/O	SPI1_MOSI	
124	PG9	I/O	USART6_RX	
129	PG14	I/O	USART6_TX	
130	VSS	Power		
131	VDD	Power		
134	PB4	I/O	SPI2_NSS	
138	BOOT0	Boot		
143	PDR_ON	Reset		
144	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC2

IN5: IN5 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 6
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Boost Mode	Enabled
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ETH

Mode: RMII

5.2.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

5.3. QUADSPI

QuadSPI Mode: Bank1 with Quad SPI Lines

5.3.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 1
Dual Flash	Disabled

5.4. SDMMC1

Mode: SD 4 bits Wide bus

5.4.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMCCLK clock divide factor	0

5.5. SPI1

Mode: Full-Duplex Master
Hardware NSS Signal: Hardware NSS Output Signal

5.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**5.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	00 Cycle
Master Keep IO State	0
IO Swap	Disabled

5.6. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

5.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**5.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	00 Cycle
Master Keep IO State	0
IO Swap	Disabled

5.7. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.8. TIM1

Clock Source : Internal Clock
Channel1: PWM Generation CH1 CH1N
Channel2: PWM Generation CH2 CH2N
Channel3: Output Compare CH3 CH3N

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Dead Time	0

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1 and 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

PWM Generation Channel 2 and 2N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

Output Compare Channel 3 and 3N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.9. USART6

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit

Over Sampling	16 Samples
Single Sample	Disable
Prescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PB1	ADC2_INP5	Analog mode	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA15	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE8	TIM1_CH1N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE10	TIM1_CH2N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE12	TIM1_CH3N	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PG9	USART6_RX	Alternate Function Push Pull	Pull-up	Low	
	PG14	USART6_TX	Alternate Function Push Pull	Pull-up	Low	

6.2. DMA configuration

nothing configured in DMA service

6.3. BDMA configuration

nothing configured in DMA service

6.4. MDMA configuration

nothing configured in DMA service

6.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
SDMMC1 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
USART6 global interrupt	unused		
FPU global interrupt	unused		
QUADSPI global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7x3
MCU	STM32H743ZITx
Datasheet	030538_Rev1

7.2. Parameter Selection

Temperature	25
Vdd	3.0