

1 Overview. The objective of this test procedure is to test the BMS PCB for use in light electric vehicles. This procedure tests basic elements of the power, instrumentation, and digital logic subsystems of the BMS PCB. This procedure is limited to initial testing of the BMS PCB, and additional test procedure documentation should be developed and executed upon in order to fully validate the design and operation of the complete system.

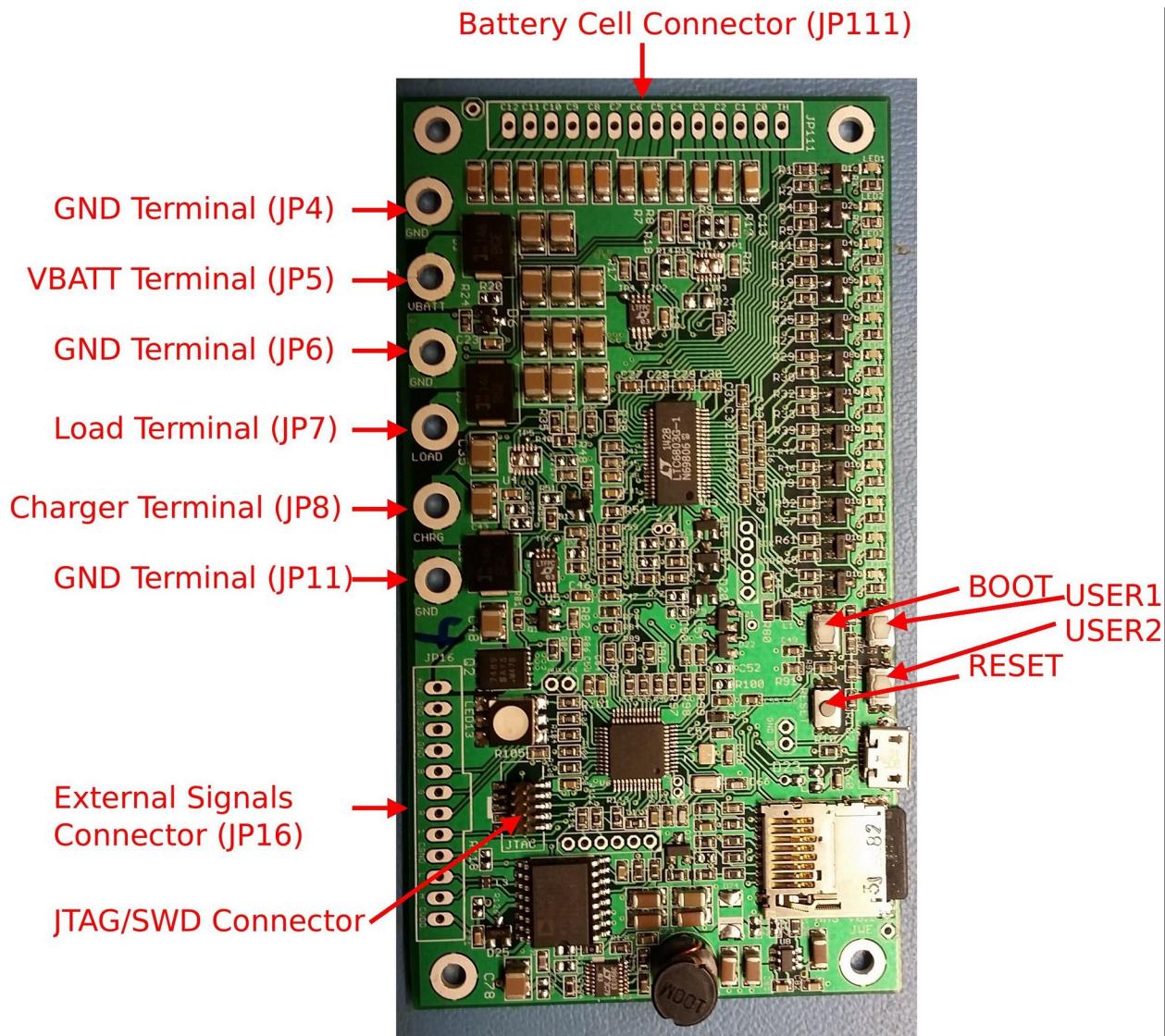


Figure 1: BMS PCB (front side)

This document assumes that the technician has practical experience and training working with power electronics. DC voltages of up to 100V may be present in the system.

Functional Test Procedure

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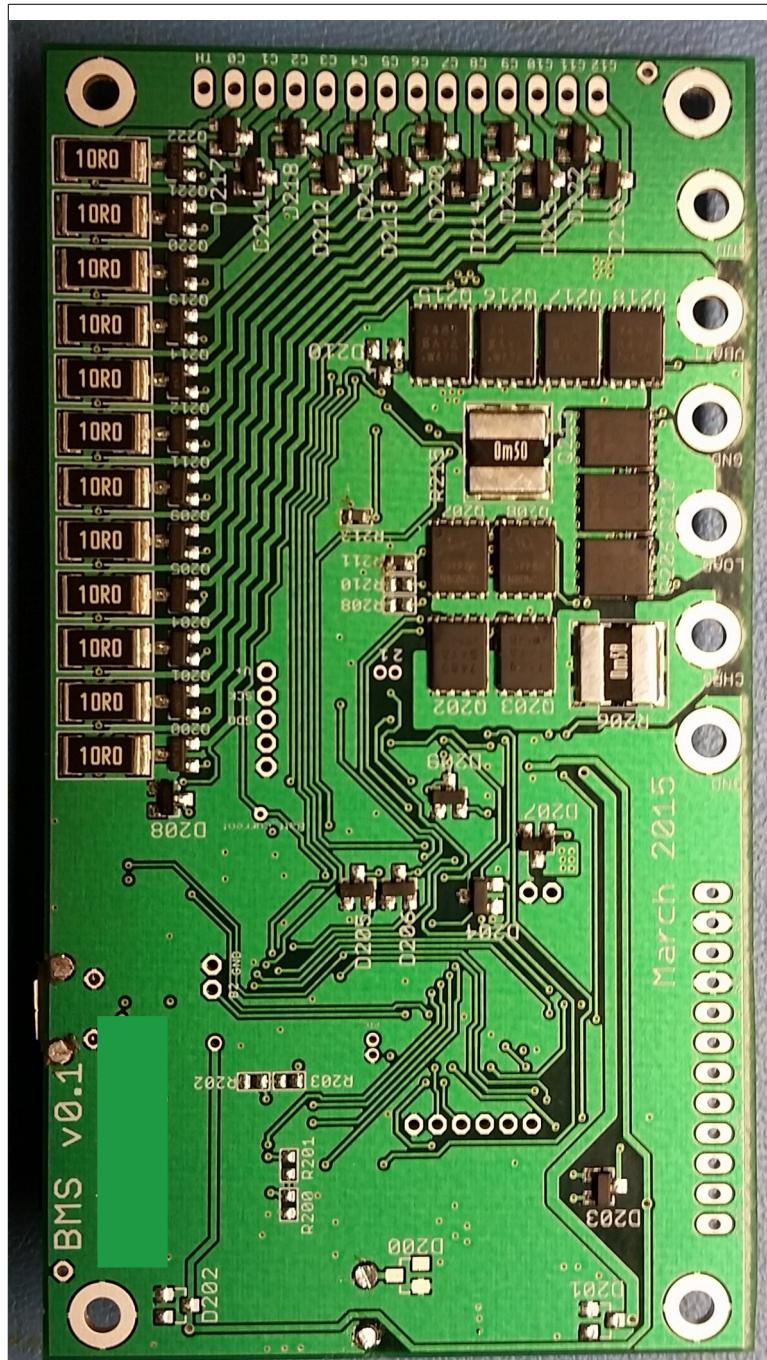


Figure 2: BMS PCB (back side)

Functional Test Procedure

5 Preparation

- 5.1 **Test Form.** Test_step_table.xlsx spreadsheet
- 5.2 **Test Purpose.** The purpose of these tests is to validate requirements provided in the file, "requirements_bms," stored in the ecen/systems git repository file system. The series of tests listed in this document test the PCB's functionality, including voltage, current, and temperature instrumentation, power-path control, and digital logic subsystems. This set of tests provides a broadly focused initial systems-level bring-up protocol for each assembled BMS PCB. It is not a comprehensive test suite for each subsystem, and further testing is required to fully verify all features of the system.
- 5.3 **Instructions.** Testing will be conducted in the Boulder Engineering Studio electronics test lab. Any technicians involved in the test are required to have a background in high power embedded electronics systems.

5.4 Required Equipment.

- DC power supply
 - 60V, 5A capable
- Oscilloscope
 - 100Mhz bandwidth or greater
- Signal analyzer
 - Saleae 8-channel V2 (100Msample/second)
- Multimeter
 - Single channel Agilent bench multimeter
 - Voltage measurement (100V tolerant)
 - Current measurement (5A capable)
- JTAG/SWD programmer
 - Stlink-V2, Segger programmer, or equivalent
- Load bank
 - Keysight 60503B
- Linux workstation
 - GCC compiler
 - GDB server
 - JTAG/SWD interface (qstlink)
- Electronics lab
 - Fire-safe high-power test area
 - Fire extinguisher

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- Non-flammable anti-static mat
- Microscope
- BNC, banana, Molex SL, Anderson Powerpole test cables, crimping tool

5.5

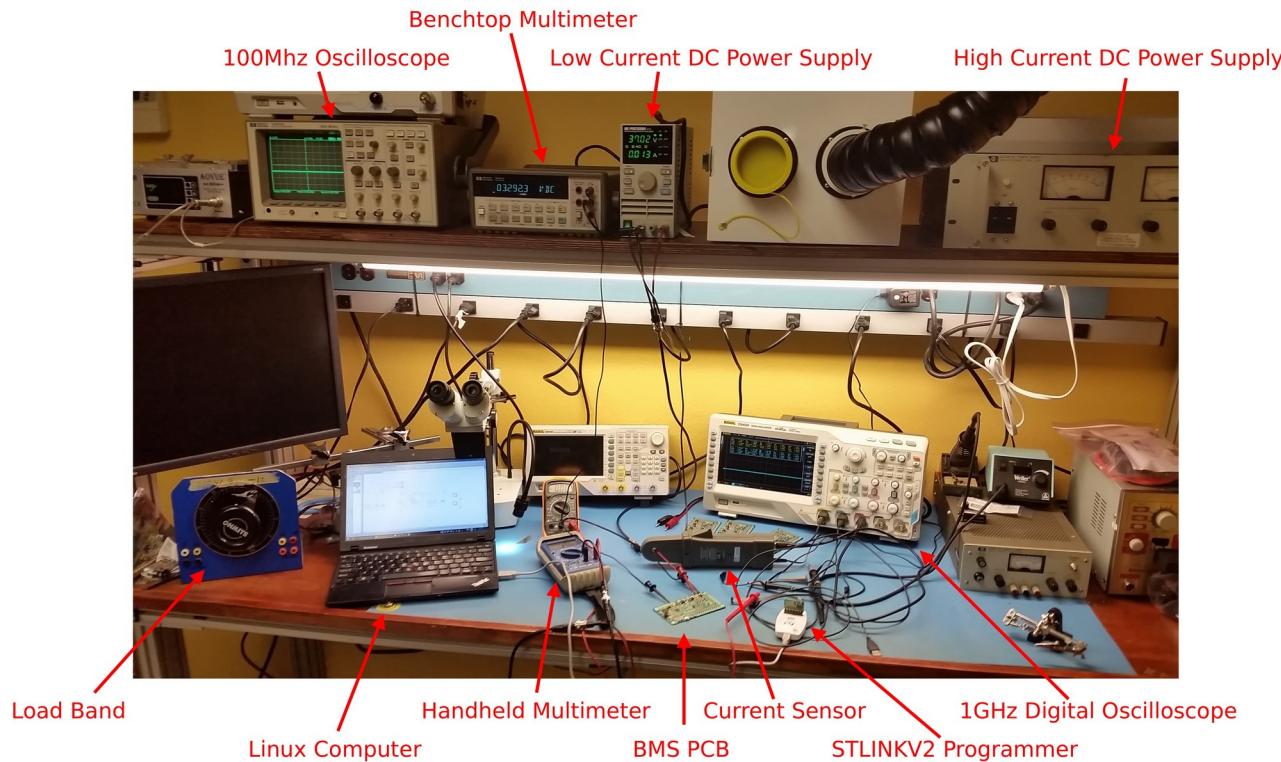


Figure 3: Required Equipment and Test Apparatus

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5.6 Precautions.

- The battery pack, the charger, the load, and the BMS are each subject to voltages as high as 60V. All personnel are advised to exercise caution and appropriate procedures in handling the the test hardware.

5.7 References

- LT1999 datasheet:<http://cds.linear.com/docs/en/datasheet/1999fc.pdf>
- LT3456 datasheet: <http://cds.linear.com/docs/en/datasheet/3456fa.pdf>
- LTC6803 datasheet: <http://www.linear.com/product/LTC6803-1>
- STM32F407 datasheet:
<http://www.st.com/web/en/resource/technical/document/datasheet/DM00037051.pdf>

Functional Test Procedure

5.8 Participants and roles/responsibilities.

Personnel	Role/Responsibility
Jone Lay	All roles

5.9 Prerequisites.

- BMS PCB is fully assembled according to bms_v0.1_assembly_bom.ods bill of materials spreadsheet
- BMS has been visually inspected for solder-jumps and other assembly defects
- Ambient temperature is 25C, +-5C

5.10 Test Completion Sign-Off. At the end of each test in Section 3, personnel involved in execution of the test or approval of test completion shall complete the sign-off block on the test form. The sign-off block shall contain the following information:

- Name of the test operator, date of the test, high-level comments

5.11 Comments and Notes. Minor changes to the test procedure shall be red lined, initialed, and dated within the test procedure hard copy. This hard copy will become the “as-run” test procedure and shall be archived. Major changes to the test procedure shall be captured in a corrective plan found in document “testing_vms_v01.ods”

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6 Conducting Test

6.1 **3.1 Test Forms.** Test steps in each test section shall be completed in the order they appear. The test operator shall mark in the left-hand column of the test form after completion of each test step. Test sections shall be reviewed at the end of each test, at the end of the complete test protocol, and as needed by individual testing processes.

Requirement 0.01

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
thermistor_pcbl	The thermistor voltage tracks the temperature of the PCB	V	The thermistor voltage follows the defined look-up table across a temperature range of -5C to 60C
INITIALS	DATA OR FILE NAME	TEST STEP	PROCEDURE
		1	Configure test freezer for -5C
		2	Disconnect all external connections from the BMS PCB
		3	Place BMS PCB in freezer
		4	Configure DC Power Supply output voltage to 50V
		5	Configure DC Power Supply current limit to 200mA
		6	Disable power supply output
		7	Connect DC power supply GND terminal to PCB GND terminal (JP4)
		8	Connect DC Power Supply output to PCB VBATT+ terminal (JP5)
		9	Connect thermocouple probe to PCB area nearby R78 with kapton tape
		10	Connect oscilloscope probe 2 to 3V3 net (JP16)
		11	Verify that freezer temperature has reached -5C
		12	Enable DC Power Supply
		13	Record voltage on pcb_temp and 3V3 nets
		14	Disable power supply output
		15	Configure test oven for 50C
		16	Place BMS PCB test apparatus in test oven
		17	Enable oven
		18	Verify that oven temperature has reached 50C
		19	Enable DC Power Supply
		20	Record voltage on pcb_temp and 3V3 nets
		21	Review results and verify that the voltage on the pcb_temp net tracks the provided look-up table +-2%

Functional Test Procedure

Requirement 0.07

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
vbatt_sense	The voltage on the chrg_sense net tracks the voltage on the charger net	D	V_chrg_sense = 0.04 V_chrg

COMPLETED	TEST STEP	PROCEDURE
	1	Disconnect all external connections from the BMS PCB
	2	Configure DC Power Supply output voltage to 50V
	3	Configure DC Power Supply current limit to 200mA
	4	Disable Power Supply output
	5	Connect DC power supply GND terminal to PCB GND terminal (JP4)
	7	Connect Power Supply output to PCB VBATT+ terminal (JP5)
	10	Connect oscilloscope probe 1 to the vbatt_sense net
	11	Connect oscilloscope probe 2 to vbatt net
	13	Enable DC Power Supply output
	15	Record voltages measured on oscilloscope probes 1 and 2
	18	Configure DC Power Supply output voltage to 35V
	19	Record voltages measured on oscilloscope probes 1 and 2
	21	Calculate transfer function from Vbatt net to Vbatt_sense net
	22	Verify that V_batt_sense = 0.04 Vbatt



Figure 4: Example Vbatt_sense tracking

Functional Test Procedure

Requirement 0.09

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
load_aout	Voltage on load_aout net linearly tracks current across sense resistor R215	D	voltage on batt_current net = 0.0166 * amps across sense resistor R215

COMPLETED	TEST STEP	PROCEDURE
	1	Disconnect all external connections from the BMS PCB
	2	Configure DC Power Supply output voltage to 50V
	3	Configure DC Power Supply current limit to 200mA
	4	Disable Power Supply output
	5	Connect DC power supply GND terminal to PCB GND terminal (JP4)
	6	Connect DC Power Supply positive output lead to current sensor
	7	Connect Current Sensor to oscilloscope channel 4
	5	Connect DC power supply GND terminal to PCB GND terminal (JP4)
	6	Connect Current Sensor output to PCB VBATT+ terminal (JP5)
	7	Configure Load Bank to dissipate zero power
	8	Connect Load Bank to Load Terminals (JP6, JP7)
	9	Connect oscilloscope probe 1 to external connector side of R215
	10	Connect oscilloscope probe 2 to downstream side of R215
	11	Connect oscilloscope probe 3 to load_aout net (JP12)
	12	Enable DC Power Supply output
	13	Apply 3.3V to Test Point 5
	14	Record voltages measured on oscilloscope probes 1 and 2
	15	Calculate current across R215
	16	Record current measured on Current Sensor
	17	Configure Load Bank to 10A
	18	Record voltages measured on oscilloscope probes 1 and 2
	19	Calculate current across R215
	20	Calculate transfer function from current across R215 to voltage on load_aout net
	21	Verify that voltage on batt_current net = 0.0166 * amps across sense resistor R215

Functional Test Procedure

Requirement 1.01

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
quiescent_current	Total PCB quiescent current is less than 1.2mA in low power mode	I	Current from V_batt, current per cell < 1.2mA
COMPLETED	TEST STEP	PROCEDURE	
	1 Disconnect all external connections from the BMS PCB 2 Configure DC Power Supply output voltage to 50V 3 Configure DC Power Supply current limit to 200mA 4 Disable power supply output 5 Connect DC power supply GND terminal to PCB GND terminal (JP4) 6 Connect DC power supply positive output lead to current sensor 7 Connect current sensor to oscilloscope 8 Connect Current Sensor output to PCB VBATT+ terminal (JP5) 9 Connect voltage meter to 3V3 net and GND (JP16) 10 Enable DC power supply output 11 Verify 3.0V < 3V3 net < 3.4V 12 Verify DC RMS current measured by the current sensor is less than 1.2mA		

Functional Test Procedure

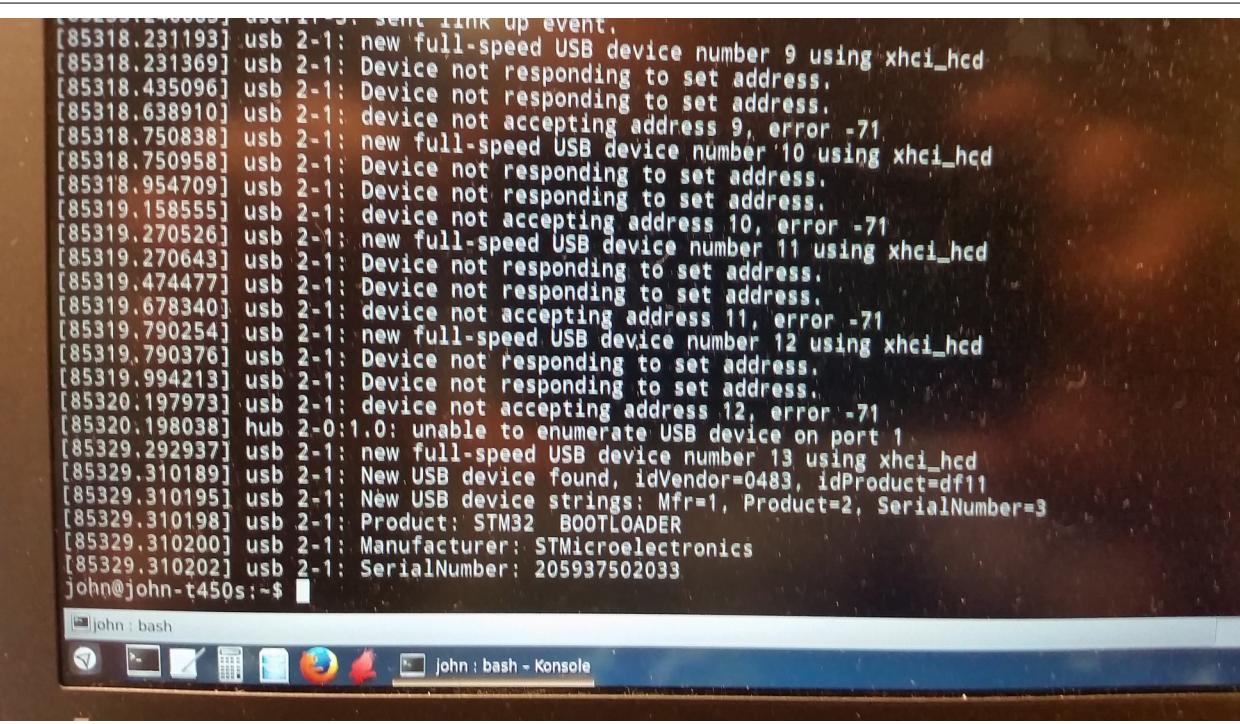
Requirement 2.03

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
aux_enable	Auxiliary power output is controlled by 0 – 3.3V signal on the aux_en net	A	Conduction between Vbatt_sense and AUX_OUT when the voltage on the aux_en net > 3V
COMPLETED	TEST STEP	PROCEDURE	
	1 Disconnect all external connections from the BMS PCB 2 Configure DC Power Supply output voltage to 50V 3 Configure DC Power Supply current limit to 200mA 4 Disable Power Supply output 5 Connect DC power supply GND terminal to PCB GND terminal (JP4) 6 Connect DC Power Supply positive output lead to current sensor 7 Connect Current Sensor to oscilloscope channel 4 8 Connect Current Sensor output to PCB VBATT+ terminal (JP5) 9 Configure Load Bank to dissipate zero power 10 Connect Load Bank to aux_out Terminals (JP16) 11 Connect oscilloscope probe 1 to Aux_out net (JP16) 12 Connect oscilloscope probe 2 to Vbatt terminal (JP5) 13 Connect oscilloscope probe 3 to Aux_enable net 14 Enable DC Power Supply output 15 Record voltages measured on oscilloscope probes 1, 2, and 3 16 Apply 3.3V to aux_enable net 17 Record voltages measured on oscilloscope probes 1, 2, and 3 18 Apply 0V to aux_enable net 19 Record voltages measured on oscilloscope probes 1, 2, and 3 20 Apply 2A to Load Bank 21 Review data and verify that the aux_out net is switched to conduct from the vbat_net when the aux_en net = 3.3V		

Functional Test Procedure

Requirement 2.06

REQ ID	REQUIREMENT		TEST METHOD	P/F CRITERIA
usb_dfu	The STM32 enumerates as a DFU device with a Linux		T	Host computer DMESG terminal output
COMPLETED	TEST STEP	PROCEDURE		
	1	Disconnect all external connections from the BMS PCB		
	2	Configure DC Power Supply output voltage to 50V		
	3	Configure DC Power Supply current limit to 200mA		
	4	Disable power supply output		
	5	Connect DC power supply GND terminal to PCB GND terminal (JP4)		
	6	Connect DC Power Supply output to PCB VBATT+ terminal (JP5)		
	7	Connect Current Sensor output to PCB VBATT+ terminal (JP5)		
	8	Connect USB cable (micro-A side) to USB micro port (JP15)		
	9	Connect USB cable (B side) to host Linux computer		
	10	Press and hold "BOOT" button		
	11	Enable DC Power Supply		
	12	Release "BOOT" button		
	13	Check DMESG output on host Linux computer		
	14	Verify that STM32 microcontroller enumerates as a USB DFU device		
	15	Disable DC Power Supply		
	16	Check DMESG output on host Linux computer		
	17	Verify that STM32 microcontroller does not enumerate as a USB DFU device		



```
[85318.231193] usb 2-1: new full-speed USB device number 9 using xhci_hcd
[85318.231369] usb 2-1: Device not responding to set address.
[85318.435096] usb 2-1: Device not responding to set address.
[85318.638910] usb 2-1: device not accepting address 9, error -71
[85318.750838] usb 2-1: new full-speed USB device number 10 using xhci_hcd
[85318.750958] usb 2-1: Device not responding to set address.
[85318.954709] usb 2-1: Device not responding to set address.
[85319.158555] usb 2-1: device not accepting address 10, error -71
[85319.270526] usb 2-1: new full-speed USB device number 11 using xhci_hcd
[85319.270643] usb 2-1: Device not responding to set address.
[85319.474477] usb 2-1: Device not responding to set address.
[85319.678340] usb 2-1: device not accepting address 11, error -71
[85319.790254] usb 2-1: new full-speed USB device number 12 using xhci_hcd
[85319.790376] usb 2-1: Device not responding to set address.
[85319.994213] usb 2-1: Device not responding to set address.
[85320.197973] usb 2-1: device not accepting address 12, error -71
[85320.198038] hub 2-0:1.0: unable to enumerate USB device on port 1
[85329.292937] usb 2-1: new full-speed USB device number 13 using xhci_hcd
[85329.310189] usb 2-1: New USB device found, idVendor=0483, idProduct=df11
[85329.310195] usb 2-1: New USB device strings: Mfr=1, Product=2, SerialNumber=3
[85329.310198] usb 2-1: Product: STM32 BOOTLOADER
[85329.310200] usb 2-1: Manufacturer: STMicroelectronics
[85329.310202] usb 2-1: SerialNumber: 205937502033
john@john-t450s:~$ 
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Figure 5: Example USB DFU enumeration

Functional Test Procedure

Requirement 2.07

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
jtag_id	The STM32 communicates its device ID over JTAG	T	Microcontroller device ID is correctly reported to a host computer
COMPLETED	TEST STEP	PROCEDURE	
	1 Disconnect all external connections from the BMS PCB 2 Configure DC Power Supply output voltage to 50V 3 Configure DC Power Supply current limit to 200mA 4 Disable power supply output 5 Connect DC power supply GND terminal to PCB GND terminal (JP4) 6 Connect DC Power Supply output to PCB VBATT+ terminal (JP5) 7 Connect Current Sensor output to PCB VBATT+ terminal (JP5) 8 Connect USB cable to STLINKV2 programmer 9 Connect USB cable (B side) to host Linux computer 10 Execute qstlink program on host Linux computer 11 Configure qstlink for JTAG mode 12 Enable DC Power Supply 13 "Connect" qstlink link via the GUI or command line 14 Verify that STM32 microcontroller reports its correct device ID through the qstlink program 15 Disable DC Power Supply		

Functional Test Procedure

Requirement 2.08

REQ ID	REQUIREMENT	TEST METHOD	P/F CRITERIA
swd_id	The STM32 communicates its device ID over SWD	D	Microcontroller device ID is correctly reported to a host computer
COMPLETED	TEST STEP	PROCEDURE	
	1 Disconnect all external connections from the BMS PCB 2 Configure DC Power Supply output voltage to 50V 3 Configure DC Power Supply current limit to 200mA 4 Disable power supply output 5 Connect DC power supply GND terminal to PCB GND terminal (JP4) 6 Connect DC Power Supply output to PCB VBATT+ terminal (JP5) 7 Connect Current Sensor output to PCB VBATT+ terminal (JP5) 8 Connect USB cable to STLINKV2 programmer 9 Connect USB cable (B side) to host Linux computer 10 Execute qstlink program on host Linux computer 11 Configure qstlink for SWD mode 12 Enable DC Power Supply 13 "Connect" qstlink link via the GUI or command line 14 Verify that STM32 microcontroller reports its correct device ID through the qstlink program 15 Disable DC Power Supply		

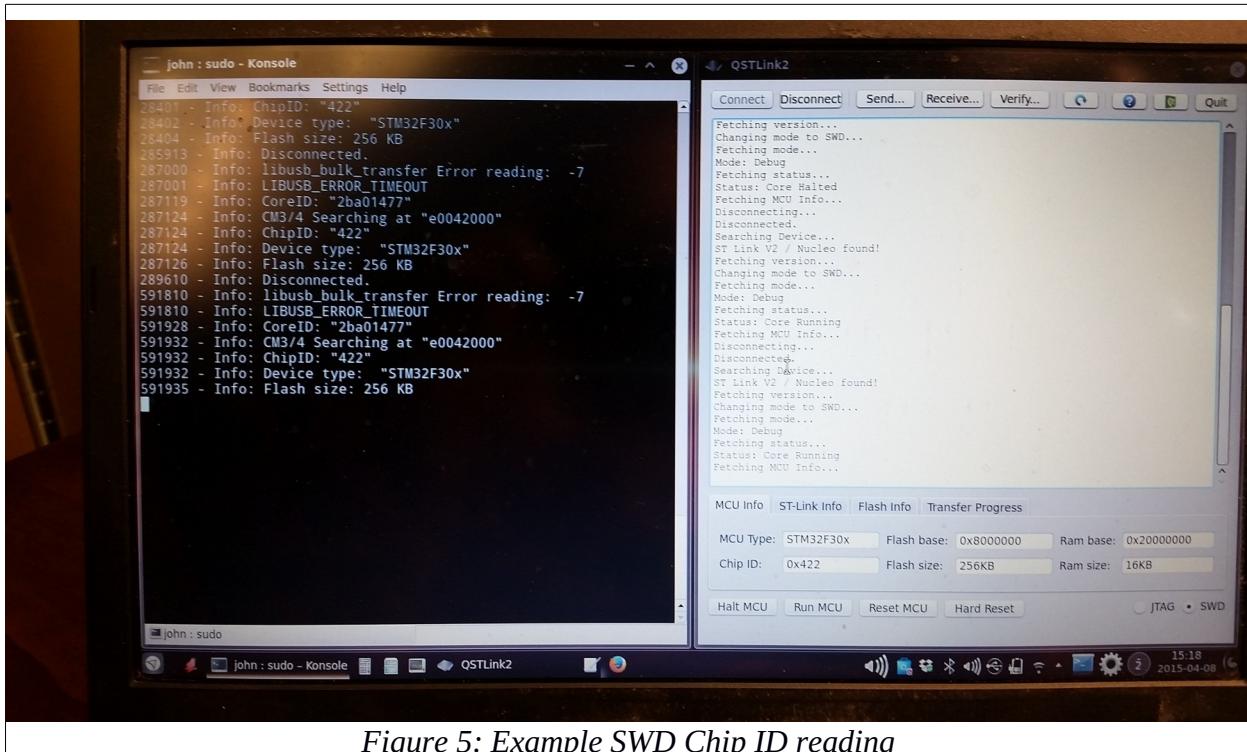


Figure 5: Example SWD Chip ID reading

Functional Test Procedure

Requirement 2.09

reset	The STM32 enters the reset state when the reset button is pressed	D	The STM32 enters the reset state when the reset button is pressed
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COMPLETED	TEST STEP	PROCEDURE	
	1	Disconnect all external connections from the BMS PCB	
	2	Configure DC Power Supply output voltage to 50V	
	3	Configure DC Power Supply current limit to 200mA	
	4	Disable power supply output	
	5	Connect DC power supply GND terminal to PCB GND terminal (JP4)	
	6	Connect DC Power Supply output to PCB VBATT+ terminal (JP5)	
	7	Connect Current Sensor output to PCB VBATT+ terminal (JP5)	
	8	Connect oscilloscope probe 1 nrst net (jtag connector)	
	9	Enable DC Power Supply	
	10	Record voltage on nrst net	
	11	Press "RESET" momentary button	
	12	Record voltage on nrst net	
	13	Verify that STM32 microcontroller reset pin is brought to <0.1V when the reset button is pressed	
	14	Verify that STM32 microcontroller reset pin is brought to >3.0V when the reset button is released	
	15	Disable DC Power Supply	