ECS 154A Homework 7

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1. The advantage of write back cache is that main memory does not have to be written to immediately. The main memory can be lazily written to when there are free cycles.

   Two disadvantages are that it is more complex. If there is a cache miss and the location to store the new data is ready to be written, it will be written at that time. Then memory will be read into the cache. This makes for two memory access instead of just one.

2. L1 cache should use virtual addresses. Since the cache is so close to the processor, speed is the main concern. A translation from virtual addresses to physical addresses would slow down L1 access. So, it's best to keep L1 addressed virtually.

3. If we take average access time to be:

   $$AverageAccessTime = HitRate \cdot UpperAccessTime + MissRate \cdot LowerAccessTime$$

   We should be able to compute this relatively easily. We need some numbers first.

   $$\begin{aligned} L1\ AccessTime &= 1\ cycle \\ L1\ HitRate &= 0.90 \\ L1\ MissRate &= 0.10 \\ L2\ AccessTime &= 10\ cycle \\ L2\ HitRate &= 0.95 \\ L2\ MissRate &= 0.05 \\ MemoryAccessTime &= 1000\ cycle \end{aligned}$$

   So we want to compute:

   $$\begin{aligned} AverageAccessTime = {} & L1\ HitRate \cdot L1\ AccessTime \\ & + L1\ MissRate(L2\ HitRate \cdot L2\ AccessTime \\ & + L2\ MissRate(MemoryAccessTime)) \end{aligned}$$

   Now we just plug and chug the numbers.

$$
\begin{aligned}
AverageAccessTime &= 0.90 \cdot 1\ cycle + 0.10(0.95 \cdot 10\ cycle + 0.05(1000\ cycle)) \\
&= 0.90 \cdot 1\ cycle + 0.10(0.95 \cdot 10\ cycle + 50\ cycle) \\
&= 0.90 \cdot 1\ cycle + 0.10(9.5\ cycle + 50\ cycle) \\
&= 0.90 \cdot 1\ cycle + 0.10(59.5\ cycle) \\
&= 0.90 \cdot 1\ cycle + 5.95\ cycle \\
&= 0.90\ cycle + 5.95\ cycle \\
&= 6.85\ cycle
\end{aligned}
$$

So the average access time is 6.85 cycles.

4. ...