# 1. Description

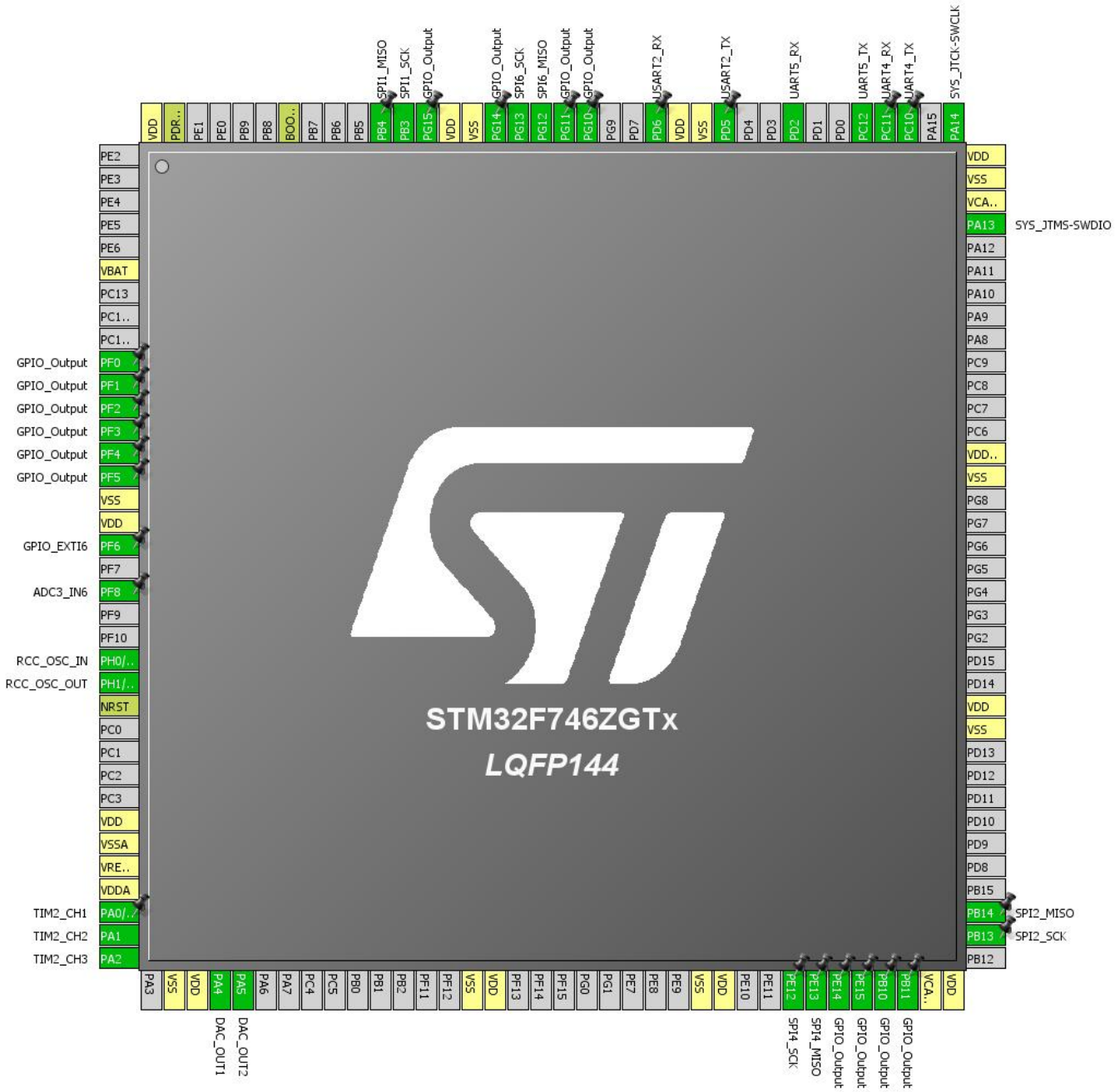
## 1.1. Project

| | |
|---|---|
| Project Name | ADCS2 |
| Board Name | No information |
| Generated with: | STM32CubeMX 4.20.1 |
| Date | 06/06/2017 |

## 1.2. MCU

| | |
|---|---|
| MCU Series | STM32F7 |
| MCU Line | STM32F7x6 |
| MCU name | STM32F746ZGTx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

# 2. Pinout Configuration



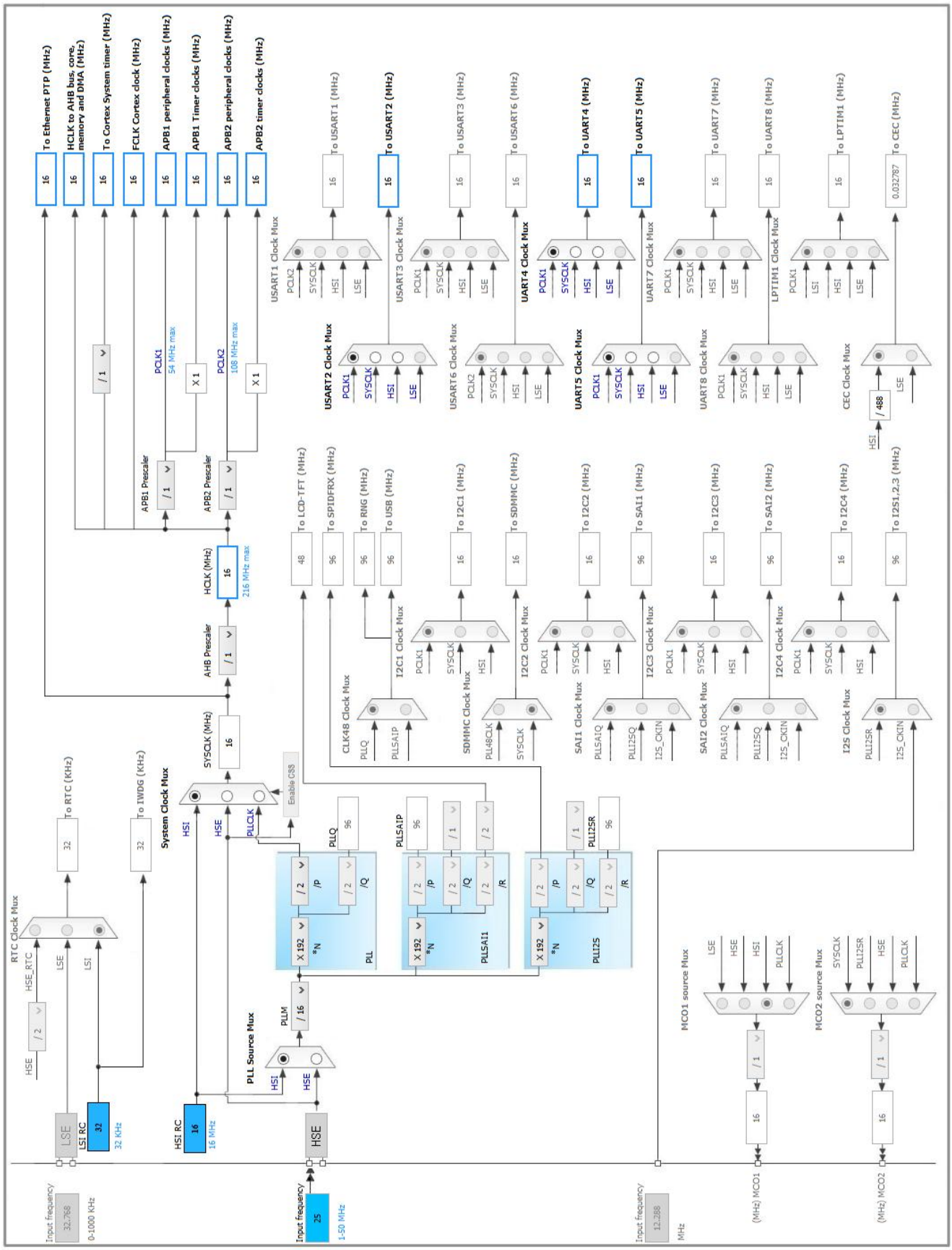
# 3. Pins Configuration

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 6 | VBAT | Power | | |
| 10 | PF0 * | I/O | GPIO_Output | |
| 11 | PF1 * | I/O | GPIO_Output | |
| 12 | PF2 * | I/O | GPIO_Output | |
| 13 | PF3 * | I/O | GPIO_Output | |
| 14 | PF4 * | I/O | GPIO_Output | |
| 15 | PF5 * | I/O | GPIO_Output | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | PF6 | I/O | GPIO_EXTI6 | |
| 20 | PF8 | I/O | ADC3_IN6 | |
| 23 | PH0/OSC_IN | I/O | RCC_OSC_IN | |
| 24 | PH1/OSC_OUT | I/O | RCC_OSC_OUT | |
| 25 | NRST | Reset | | |
| 30 | VDD | Power | | |
| 31 | VSSA | Power | | |
| 32 | VREF+ | Power | | |
| 33 | VDDA | Power | | |
| 34 | PA0/WKUP | I/O | TIM2_CH1 | |
| 35 | PA1 | I/O | TIM2_CH2 | |
| 36 | PA2 | I/O | TIM2_CH3 | |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 40 | PA4 | I/O | DAC_OUT1 | |
| 41 | PA5 | I/O | DAC_OUT2 | |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 65 | PE12 | I/O | SPI4_SCK | |
| 66 | PE13 | I/O | SPI4_MISO | |
| 67 | PE14 * | I/O | GPIO_Output | |
| 68 | PE15 * | I/O | GPIO_Output | |
| 69 | PB10 * | I/O | GPIO_Output | |
| 70 | PB11 * | I/O | GPIO_Output | |
| 71 | VCAP_1 | Power | | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|---|---|---|---|---|
| 72 | VDD | Power | | |
| 74 | PB13 | I/O | SPI2_SCK | |
| 75 | PB14 | I/O | SPI2_MISO | |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 94 | VSS | Power | | |
| 95 | VDDUSB | Power | | |
| 105 | PA13 | I/O | SYS_JTMS-SWDIO | |
| 106 | VCAP_2 | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |
| 109 | PA14 | I/O | SYS_JTCK-SWCLK | |
| 111 | PC10 | I/O | UART4_TX | |
| 112 | PC11 | I/O | UART4_RX | |
| 113 | PC12 | I/O | UART5_TX | |
| 116 | PD2 | I/O | UART5_RX | |
| 119 | PD5 | I/O | USART2_TX | |
| 120 | VSS | Power | | |
| 121 | VDD | Power | | |
| 122 | PD6 | I/O | USART2_RX | |
| 125 | PG10 * | I/O | GPIO_Output | |
| 126 | PG11 * | I/O | GPIO_Output | |
| 127 | PG12 | I/O | SPI6_MISO | |
| 128 | PG13 | I/O | SPI6_SCK | |
| 129 | PG14 * | I/O | GPIO_Output | |
| 130 | VSS | Power | | |
| 131 | VDD | Power | | |
| 132 | PG15 * | I/O | GPIO_Output | |
| 133 | PB3 | I/O | SPI1_SCK | |
| 134 | PB4 | I/O | SPI1_MISO | |
| 138 | BOOT0 | Boot | | |
| 143 | PDR_ON | Reset | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

# 4. Clock Tree Configuration



# 5. IPs and Middleware Configuration

## 5.1. ADC3

**mode: IN6**

### 5.1.1. Parameter Settings:

**ADCs_Common_Settings:**

| | |
|---|---|
| Mode | Independent mode |

**ADC_Settings:**

| | |
|---|---|
| Clock Prescaler | PCLK2 divided by 2 |
| Resolution | 12 bits (15 ADC Clock cycles) |
| Data Alignment | Right alignment |
| Scan Conversion Mode | Disabled |
| Continuous Conversion Mode | Disabled |
| Discontinuous Conversion Mode | Disabled |
| DMA Continuous Requests | Disabled |
| End Of Conversion Selection | EOC flag at the end of single channel conversion |

**ADC_Regular_ConversionMode:**

| | |
|---|---|
| Number Of Conversion | 1 |
| External Trigger Conversion Source | Regular Conversion launched by software |
| External Trigger Conversion Edge | None |
| Rank | 1 |
| Channel | Channel 6 |
| Sampling Time | 3 Cycles |

**ADC_Injected_ConversionMode:**

| | |
|---|---|
| Number Of Conversions | 0 |

**WatchDog:**

| | |
|---|---|
| Enable Analog WatchDog Mode | false |

## 5.2. DAC

**mode: OUT1 Configuration**

**mode: OUT2 Configuration**

### 5.2.1. Parameter Settings:

**DAC Out1 Settings:**

| | |
|---|---|
| Output Buffer | Enable |
| Trigger | None |

**DAC Out2 Settings:**

| | |
|---|---|
| Output Buffer | Enable |
| Trigger | None |

## *5.3. RCC*

### High Speed Clock (HSE): BYPASS Clock Source

### 5.3.1. Parameter Settings:

**System Parameters:**

| | |
|---|---|
| VDD voltage (V) | 3.3 |
| Flash Latency(WS) | 0 WS (1 CPU cycle) |

**RCC Parameters:**

| | |
|---|---|
| HSI Calibration Value | 16 |
| TIM Prescaler Selection | Disabled |
| HSE Startup Timout Value (ms) | 100 |
| LSE Startup Timout Value (ms) | 5000 |

**Power Parameters:**

| | |
|---|---|
| Power Over Drive | Disabled |
| Power Regulatror Voltage Scale | Power Regulator Voltage Scale 3 |

## *5.4. SPI1*

### Mode: Receive Only Master

### 5.4.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |

| | |
|---|---|
| Baud Rate | **8.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## *5.5. SPI2*

### Mode: Receive Only Master

### 5.5.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **8.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## *5.6. SPI4*

### Mode: Receive Only Master

### 5.6.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **8.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## *5.7. SPI6*

**Mode: Receive Only Master**

### 5.7.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Frame Format | Motorola |
| Data Size | 4 Bits |
| First Bit | MSB First |

**Clock Parameters:**

| | |
|---|---|
| Prescaler (for Baud Rate) | 2 |
| Baud Rate | **8.0 MBits/s *** |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

**Advanced Parameters:**

| | |
|---|---|
| CRC Calculation | Disabled |
| NSSP Mode | Enabled |
| NSS Signal Type | Software |

## *5.8. SYS*

**Debug: Serial Wire**

**Timebase Source: SysTick**

## *5.9. TIM2*

**Clock Source : Internal Clock**
**Channel1: Input Capture direct mode**
**Channel2: Input Capture direct mode**
**Channel3: Input Capture direct mode**

### 5.9.1. Parameter Settings:

**Counter Settings:**

| | |
|---|---|
| Prescaler (PSC - 16 bits value) | 0 |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 32 bits value ) | 0 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

**Trigger Output (TRGO) Parameters:**

| | |
|---|---|
| Master/Slave Mode | Disable (no sync between this TIM (Master) and its Slaves |
| Trigger Event Selection TRGO | Reset (UG bit from TIMx_EGR) |

**Input Capture Channel 1:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

**Input Capture Channel 2:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

**Input Capture Channel 3:**

| | |
|---|---|
| Polarity Selection | Rising Edge |
| IC Selection | Direct |
| Prescaler Division Ratio | No division |
| Input Filter (4 bits value) | 0 |

## *5.10. UART4*

**Mode: Asynchronous**

### 5.10.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 7 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

## *5.11. UART5*

**Mode: Asynchronous**

### 5.11.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 7 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |

| | |
|---|---|
| DMA on RX Error | Enable |
| MSB First | Disable |

## *5.12. USART2*

### Mode: Asynchronous

### 5.12.1. Parameter Settings:

**Basic Parameters:**

| | |
|---|---|
| Baud Rate | 115200 |
| Word Length | 7 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

**Advanced Parameters:**

| | |
|---|---|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |
| Single Sample | Disable |

**Advanced Features:**

| | |
|---|---|
| Auto Baudrate | Disable |
| TX Pin Active Level Inversion | Disable |
| RX Pin Active Level Inversion | Disable |
| Data Inversion | Disable |
| TX and RX Pins Swapping | Disable |
| Overrun | Enable |
| DMA on RX Error | Enable |
| MSB First | Disable |

*** User modified value**

# 6. System Configuration

## 6.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| ADC3 | PF8 | ADC3_IN6 | Analog mode | No pull-up and no pull-down | n/a | |
| DAC | PA4 | DAC_OUT1 | Analog mode | No pull-up and no pull-down | n/a | |
| | PA5 | DAC_OUT2 | Analog mode | No pull-up and no pull-down | n/a | |
| RCC | PH0/OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | |
| | PH1/OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| SPI1 | PB3 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB4 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SPI2 | PB13 | SPI2_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PB14 | SPI2_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SPI4 | PE12 | SPI4_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PE13 | SPI4_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SPI6 | PG12 | SPI6_MISO | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| | PG13 | SPI6_SCK | Alternate Function Push Pull | No pull-up and no pull-down | **Very High *** | |
| SYS | PA13 | SYS_JTMS-SWDIO | n/a | n/a | n/a | |
| | PA14 | SYS_JTCK-SWCLK | n/a | n/a | n/a | |
| TIM2 | PA0/WKUP | TIM2_CH1 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA1 | TIM2_CH2 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| | PA2 | TIM2_CH3 | Alternate Function Push Pull | No pull-up and no pull-down | Low | |
| UART4 | PC10 | UART4_TX | Alternate Function Push Pull | Pull-up | **Very High *** | |
| | PC11 | UART4_RX | Alternate Function Push Pull | Pull-up | **Very High** | |

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|---|---|---|---|---|---|---|
| | | | | | * | |
| UART5 | PC12 | UART5_TX | Alternate Function Push Pull | Pull-up | **Very High** * | |
| | PD2 | UART5_RX | Alternate Function Push Pull | Pull-up | **Very High** * | |
| USART2 | PD5 | USART2_TX | Alternate Function Push Pull | Pull-up | **Very High** * | |
| | PD6 | USART2_RX | Alternate Function Push Pull | Pull-up | **Very High** * | |
| GPIO | PF0 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF1 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF2 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF3 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF4 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF5 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PF6 | GPIO_EXTI6 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | |
| | PE14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PE15 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PB10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PB11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PG10 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PG11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PG14 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |
| | PG15 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Low | |

## *6.2. DMA configuration*

nothing configured in DMA service

## 6.3. NVIC configuration

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|---|---|---|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| ADC1, ADC2 and ADC3 global interrupts | unused | | |
| EXTI line[9:5] interrupts | unused | | |
| TIM2 global interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| SPI2 global interrupt | unused | | |
| USART2 global interrupt | unused | | |
| UART4 global interrupt | unused | | |
| UART5 global interrupt | unused | | |
| TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts | unused | | |
| FPU global interrupt | unused | | |
| SPI4 global interrupt | unused | | |
| SPI6 global interrupt | unused | | |

*** User modified value**

# 7. Power Consumption Calculator report

## 7.1. Microcontroller Selection

| | |
|---|---|
| Series | STM32F7 |
| Line | STM32F7x6 |
| MCU | STM32F746ZGTx |
| Datasheet | 027590_Rev4 |

## 7.2. Parameter Selection

| | |
|---|---|
| Temperature | 25 |
| Vdd | 3.3 |