

Real-Time Operating System (Day 4 Lab)

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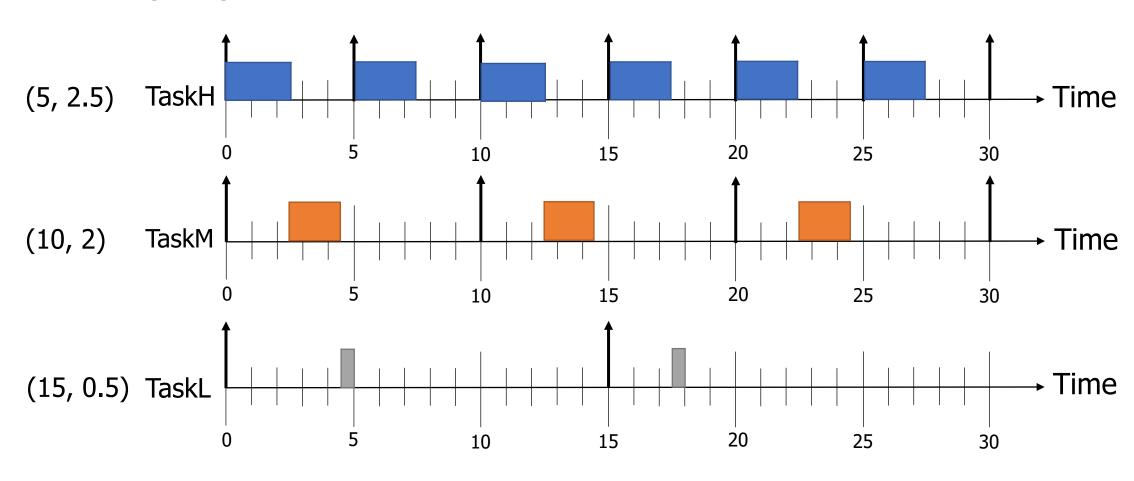


22. Schedule Table

```
SCHEDULETABLE SchedTab1 {
    COUNTER = counter1;
                              Cycle Time
    DURATION = 10; -
    REPEATING = TRUE;
   AUTOSTART = TRUE {
                              Start Offset
        START VALUE = 5;
                                                        Task Activation
    EXPIRE POINT = ACTION {
        EXPIRE VALUE = 0;
        ACTION = ACTIVATETASK { TASK = TaskH; };
        ACTION = ACTIVATETASK { TASK = TaskL; };
    EXPIRE POINT = ACTION {
                                                                Event Setting
        EXPIRE VALUE = 5;
        ACTION = ACTIVATETASK { TASK = TaskH; };
        ACTION = SETEVENT { TASK = TaskL; EVENT = Event1; };
    };
};
```

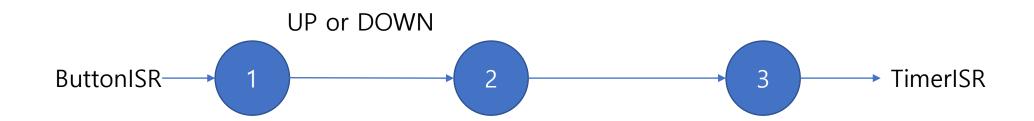
22. Schedule Table

- 3개 Task 생성 및 Scheduling 실험
- Timing diagram



23. End-to-End Delay

- AUTOSAR 기반 DAG (Directed Acyclic Graph) SW 구조
- Sensor에서 Actuator까지 End-to-End Delay 관찰



23. End-to-End Delay

• 아래 복잡한 DAG 구조를 정의하고 Delay 측정 세 입력이 모두 UP 혹은 DOWN이면 반응 UP or DOWN ButtonISR⁻ **TimerISR** UP or DOWN

Questions

